Overvoltage Protection for 2-Series and 3-Series Cell Li-Ion Batteries

Check for Samples: bq294502, bq294504, bq294512, bq294515, bq294522, bq294524, bq294532, bq294562, bq294572, bq294582, bq294592

FEATURES

- 2-Series and 3-Series Cell Monitor for Secondary Protection
- Fixed Programmable Delay Timer
- Fixed OVP Threshold:
  - bq294502 = 4.35 V with 4-s Delay Timer
  - bq294504 = 4.35 V with 6.5-s Delay Timer
  - bq294512 = 4.40 V with 4-s Delay Timer
  - bq294515 = 4.425 V with 4-s Delay Timer
  - bq294522 = 4.45 V with 4-s Delay Timer
  - bq294524 = 4.45 V with 6.5-s Delay Timer
  - bq294532 = 4.50 V with 4-s Delay Timer
  - bq294562 = 4.25 V with 4-s Delay Timer
  - bq294572 = 4.00 V with 4-s Delay Timer
  - bq294582 = 4.225 V with 4-s Delay Timer
  - bq294584 = 4.225 V with 6.5-s Delay Timer
  - bq294592 = 4.30 V with 4-s Delay Timer
- High-Accuracy Overvoltage Protection: ± 10 mV
- Low Power Consumption I_{CC} ≈ 1 µA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- Low leakage current per cell input < 100 nA
- Small package footprint
  - 6-pin SON

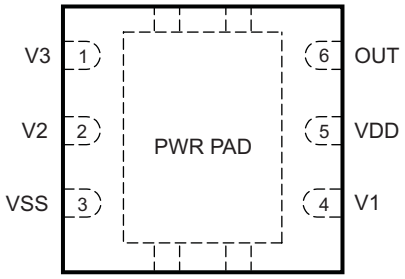
APPLICATIONS

- 2nd-Level Protection in Li-Ion Battery Packs in:
  - Tablets
  - Slates
  - Power Tools
  - Notebook Computers
  - Portable Equipment and Instrumentation

DESCRIPTION

The bq2945xy family of products is a secondary level voltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. Based on the configuration, an output is triggered after a fixed delay if any one of the two or three cells has an overvoltage condition. This output will be triggered into a high state after an overvoltage condition has satisfied the specified delay timer.

DRV Package
(Top View)



PIN FUNCTIONS

bq2945xy	Pin Name	Type I/O	Description
1	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
2	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack
3	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
4	V1	IA	Sense input for positive voltage of the lowest cell in the stack
5	VDD	P	Power supply
6	OUT	OA	Output drive for external N-Channel FET
Thermal Pad	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed circuit board for proper operation

PIN DETAILS

Description

The voltage sensing for each cell is done independently using a multiplexer. The method of overvoltage detection is comparing the voltage to an overvoltage protection voltage V_{OV}. Once the voltage exceeds the programmed fixed value, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for either a 4-s or 6.5-s delay. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if *all* of the cell inputs (Vx) are below the OVP threshold minus the Vhys.

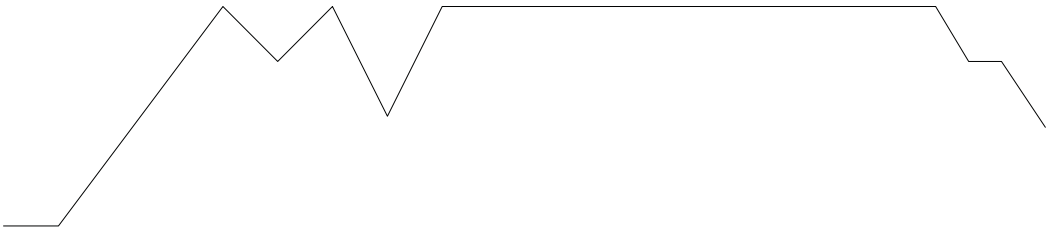


Figure 1. Timing for Overvoltage Sensing

Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

The gate of an external N-Channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. The out will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

DC CHARACTERISTICS (continued)

Typical values stated where T_A = 25°C and VDD = 10.8 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 15 V (unless otherwise noted).

	Symbol	Parameter	Condition	Min	Typ	Max	Unit
Voltage Protection Threshold VCx							
1.24	t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode	Fixed delay (Internal settings)		15		ms

TYPICAL CHARACTERISTICS

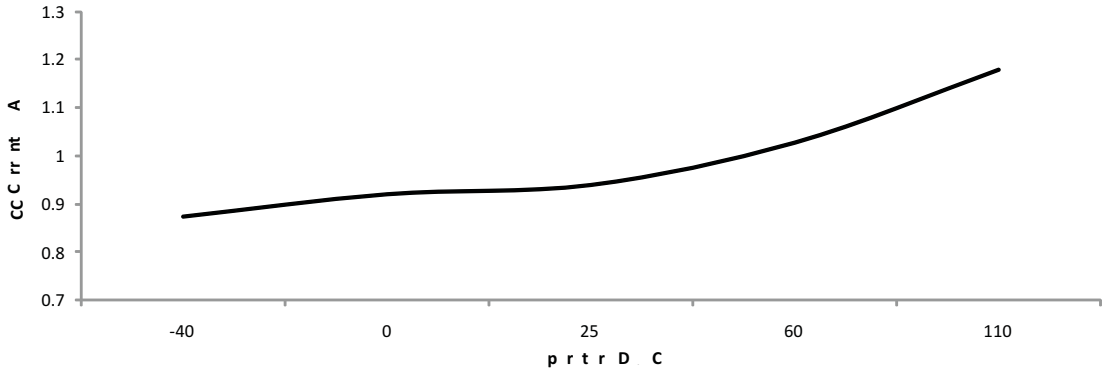


Figure 2. I_{CC} Current Consumption Versus Temperature

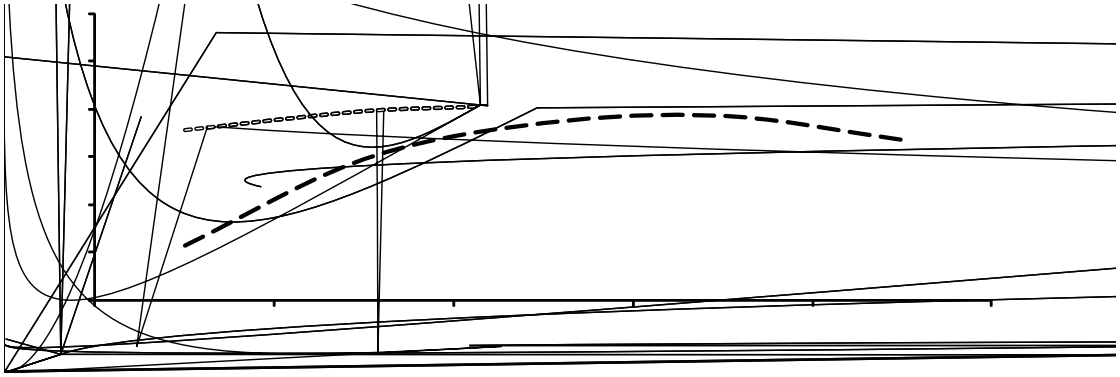


Figure 3. bq294502 Overvoltage Threshold (OVT) vs. Temp

Figure 4. Hysteresis V_{HYS} Versus Temperature

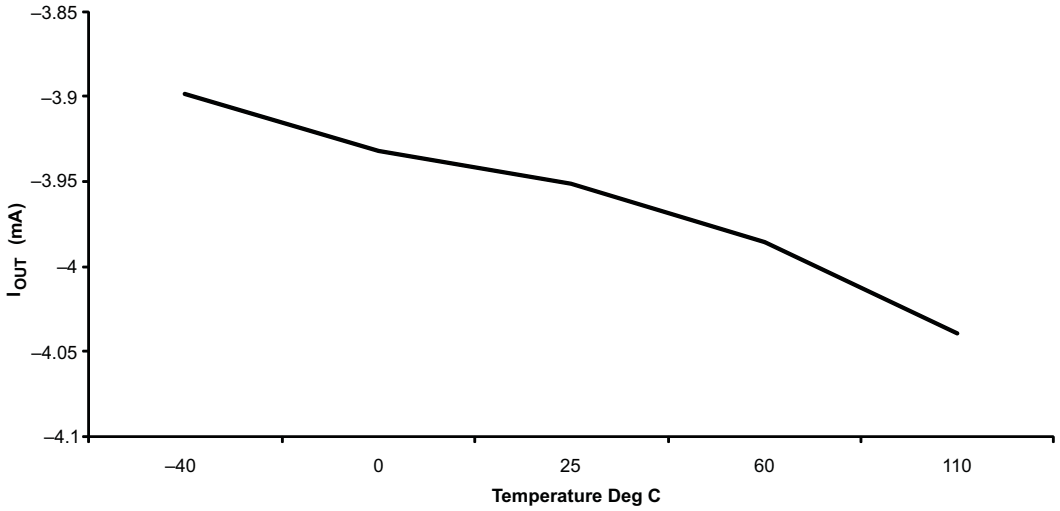


Figure 5. Output Current I_{OUT} Versus Temperature

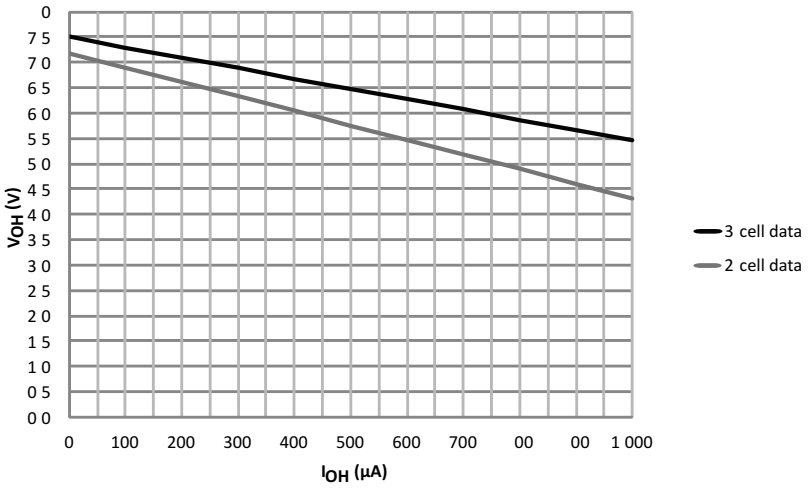


Figure 6. Output Voltage Versus Output Current

APPLICATION INFORMATION

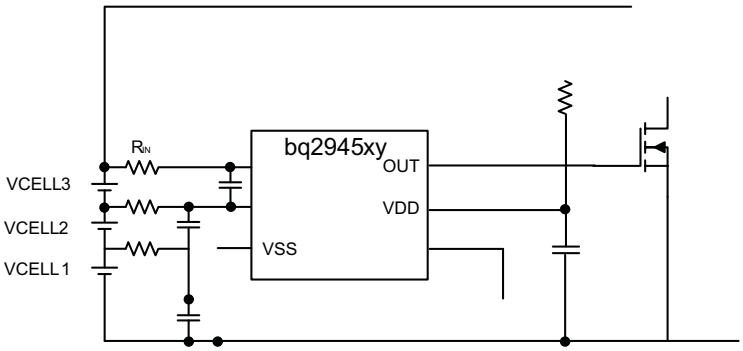


Figure 7. Application Configuration

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 7 shows each external component.

Table 1. Parameters

PARAMETER	External Component	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01		0.1	µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

APPLICATION SCHEMATIC

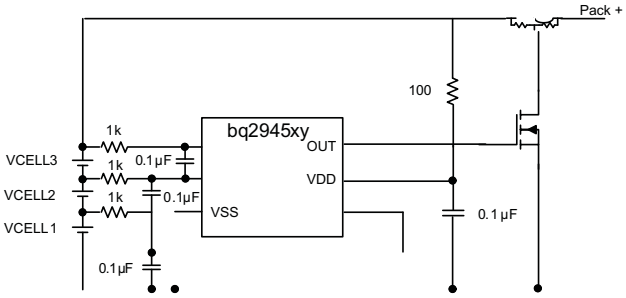


Figure 8. 3-Series Cell Configuration with Fixed Delay

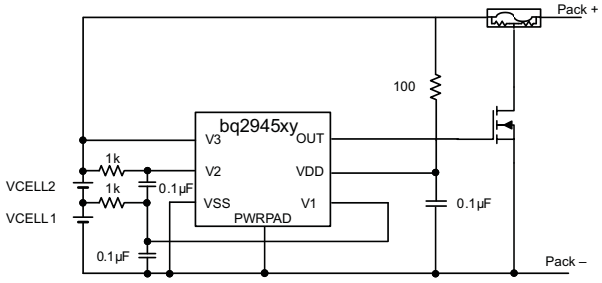


Figure 9. 2-Series Cell Configuration with Internal Fixed Delay

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V3 (see Figure 10). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to VC3 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 10 shows the timing for the Customer Test Mode.

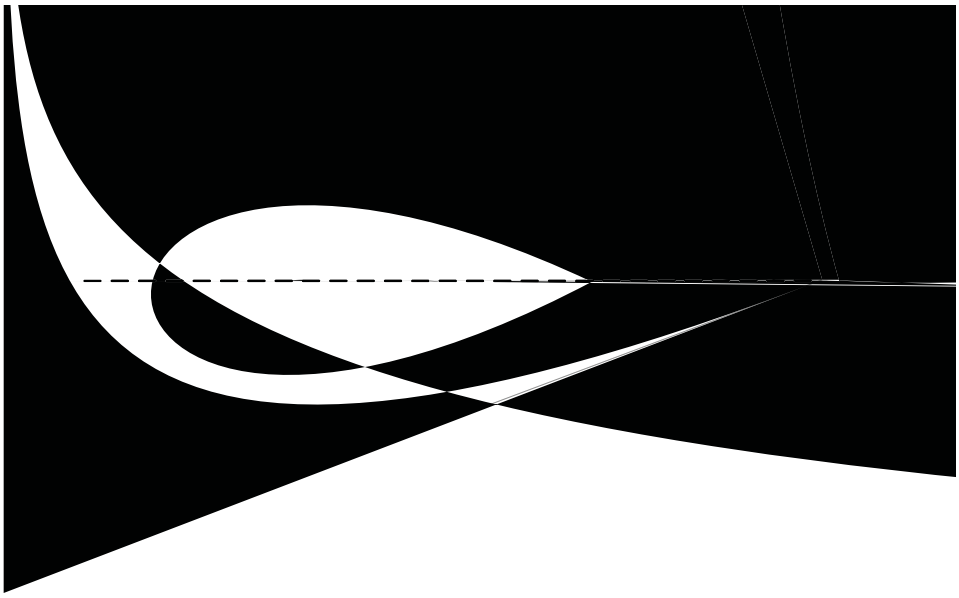


Figure 10. Timing for Customer Test Mode

Figure 11 shows the measurement for current consumption for the product for both VDD and Vx.

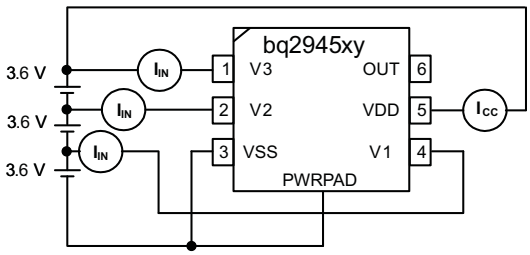


Figure 11. Configuration for IC Current Consumption Test

REVISION HISTORY

Changes from Original (September 2011) to Revision A **Page**

- Added the bq294582 Device to Production Data 2

Changes from Revision A (November 2011) to Revision B **Page**

- Changed the bq294504 Device to Production Data 1
- Added the bq294512 Device 1
- Added the bq294592 Device 1
- Added a second I_{CC} Test Condition 5
- Changed Fault Detection Delay Time in bq2945x4 Test Mode Specifications 5

Changes from Revision B (February 2012) to Revision C **Page**

- Added the bq294515 Device to Production Data 2
- Added the bq294524 Device to Production Data 2
- Added the bq294532 Device to Production Data 2
- Added the bq294572 Device to Production Data 2
- Changed Overvoltage Detection Hysteresis 5
- Added Output Voltage Versus Output Current graphic 7
- Changed Timing for Customer Test Mode figure 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ294502DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Top-Side Markings

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ294592DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

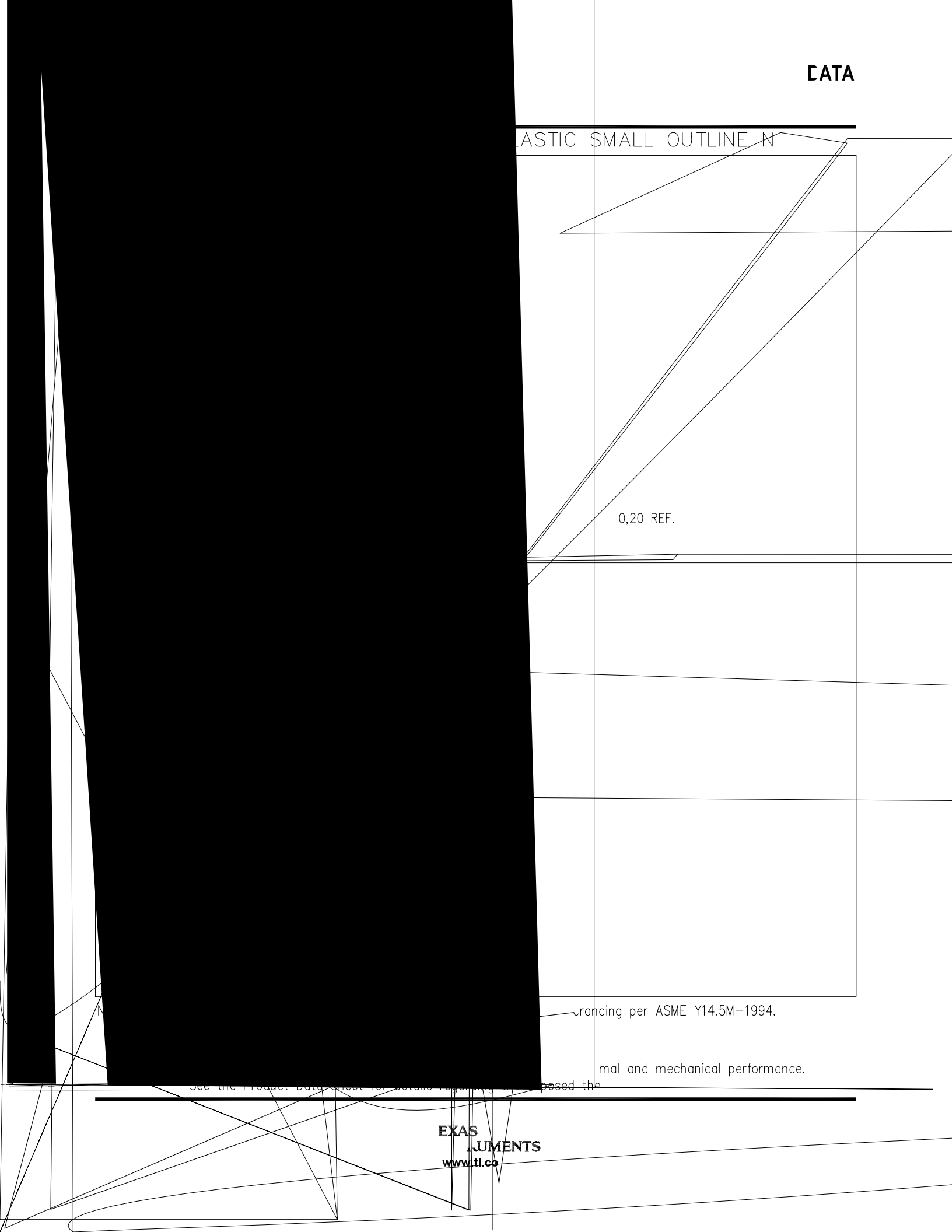
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294502DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294502DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294504DRVR	SON	DRV	6	0	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294504DRVT	SON	DRV	6	0	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294512DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294512DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294522DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294522DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294524DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294524DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294532DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294532DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294582DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294582DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294592DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294592DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294502DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294502DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVR	SON	DRV	6	0	367.0	367.0	35.0
BQ294504DRVT	SON	DRV	6	0	210.0	185.0	35.0
BQ294512DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294512DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294522DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294522DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294524DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294532DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294582DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294592DRVT	SON	DRV	6	250	210.0	185.0	35.0

ASTIC SMALL OUTLINE N



rancing per ASME Y14.5M–1994.

mal and mechanical performance.

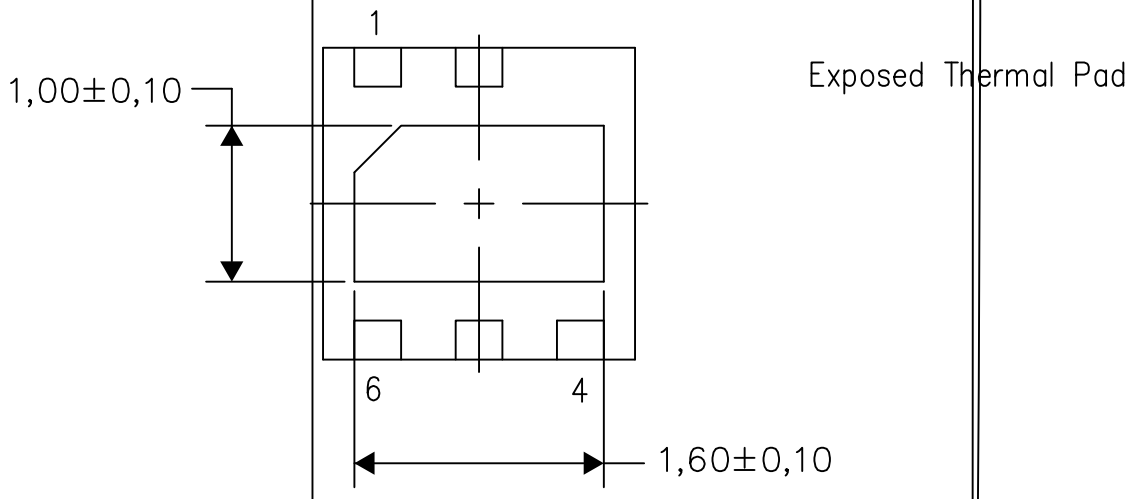
PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached

pecial heatsink structure designed into the PCB. This design optimizes the heat transfer from the

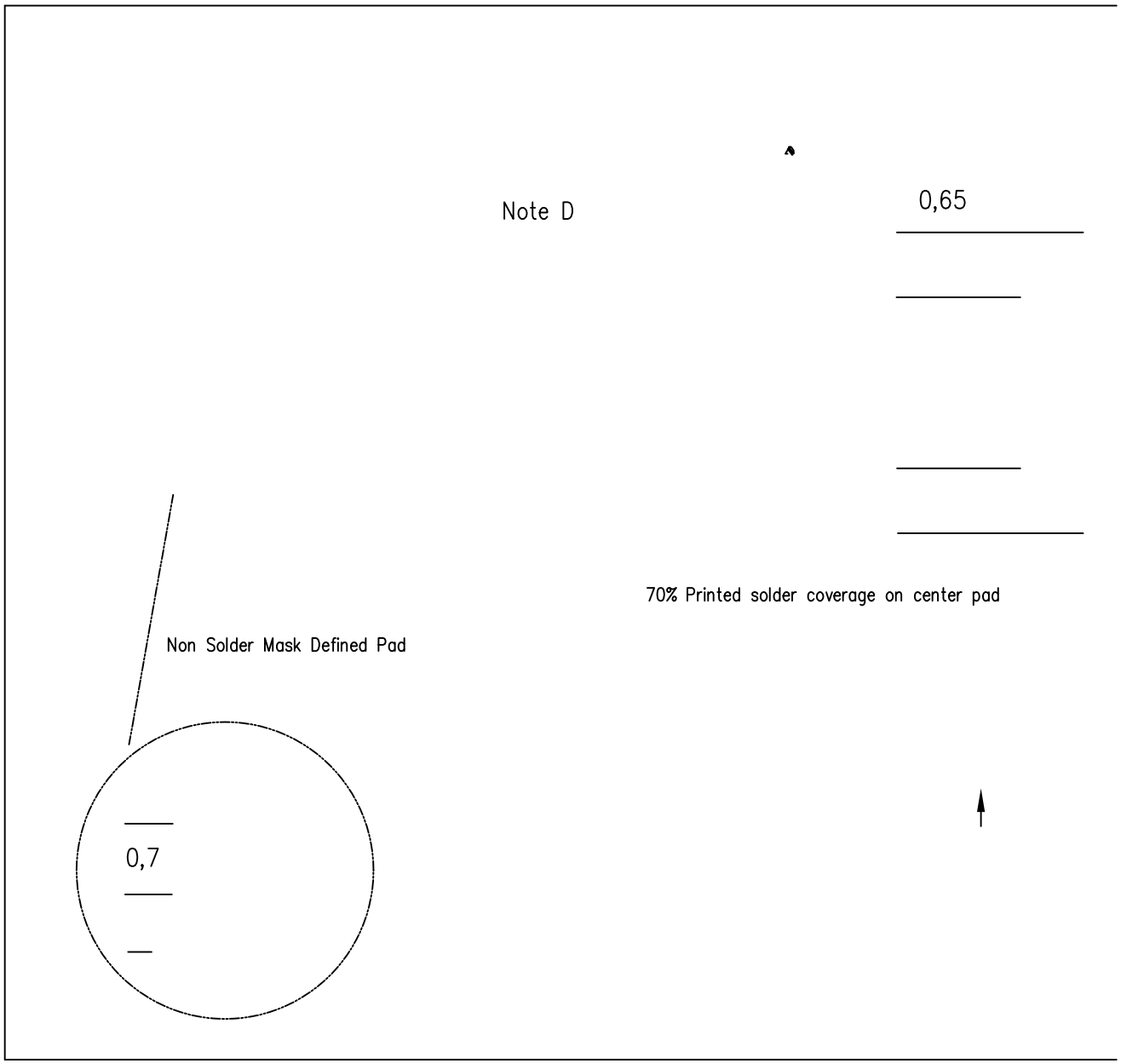
For information on the Quad Flatpack No–Lead (QFN) rcuit (IC).



Bottom View

Exposed Thermal Pad Dimensions

NOTE: All linear dimensions are in millimeters



C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout.
T
Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. Customers should contact their board fabrication site for solder mask tolerances.

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