

## Overvoltage Protection for 2-Series and 3-Series Cell Li-Ion Batteries

Check for

 Samples: [bq294502](#), [bq294504](#), [bq294512](#), [bq294515](#), [bq294522](#), [bq294524](#), [bq294532](#), [bq294562](#), [bq294572](#), [bq294582](#), [bq294592](#)

### FEATURES

- 2-Series and 3-Series Cell Monitor for Secondary Protection
- Fixed Programmable Delay Timer
- Fixed OVP Threshold:
  - bq294502 = 4.35 V with 4-s Delay Timer
  - bq294504 = 4.35 V with 6.5-s Delay Timer
  - bq294512 = 4.40 V with 4-s Delay Timer
  - bq294515 = 4.425 V with 4-s Delay Timer
  - bq294522 = 4.45 V with 4-s Delay Timer
  - bq294524 = 4.45 V with 6.5-s Delay Timer
  - bq294532 = 4.50 V with 4-s Delay Timer
  - bq294562 = 4.25 V with 4-s Delay Timer
  - bq294572 = 4.00 V with 4-s Delay Timer
  - bq294582 = 4.225 V with 4-s Delay Timer
  - bq294584 = 4.225 V with 6.5-s Delay Timer
  - bq294592 = 4.30 V with 4-s Delay Timer
- High-Accuracy Overvoltage Protection:
  - ± 10 mV

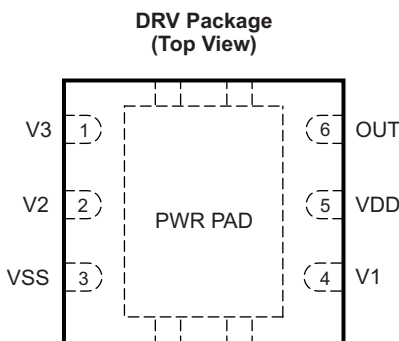
- Low Power Consumption  $I_{CC} = 1 \mu A$   
( $V_{CELL(ALL)} < V_{PROTECT}$ )
- Low leakage current per cell input < 100 nA
- Small package footprint
  - 6-pin SON

### APPLICATIONS

- 2<sup>nd</sup>-Level Protection in Li-Ion Battery Packs in:
  - Tablets
  - Slates
  - Power Tools
  - Notebook Computers
  - Portable Equipment and Instrumentation

### DESCRIPTION

The bq2945xy family of products is a secondary level voltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. Based on the configuration, an output is triggered after a fixed delay if any one of the two or three cells has an overvoltage condition. This output will be triggered into a high state after an overvoltage condition has satisfied the specified delay timer.



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## PIN FUNCTIONS

bq2945xy	Pin Name	Type I/O	Description
1	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
2	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack
3	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
4	V1	IA	Sense input for positive voltage of the lowest cell in the stack
5	VDD	P	Power supply
6	OUT	OA	Output drive for external N-Channel FET
Thermal Pad	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed circuit board for proper operation

## PIN DETAILS

### Description

The voltage sensing for each cell is done independently using a multiplexer. The method of overvoltage detection is comparing the voltage to an overvoltage protection voltage  $V_{OV}$ . Once the voltage exceeds the programmed fixed value, the delay timer circuit is activated. This delay ( $t_{DELAY}$ ) is fixed for either a 4-s or 6.5-s delay. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if *all* of the cell inputs ( $V_x$ ) are below the OVP threshold minus the  $V_{phys}$ .

**Figure 1. Timing for Overvoltage Sensing**

### Sense Positive Input for $V_x$

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

### Output Drive, OUT

The gate of an external N-Channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. The out will reset to a low level if the cell voltage falls below the  $V_{OV}$  threshold before the fixed delay timer expires.

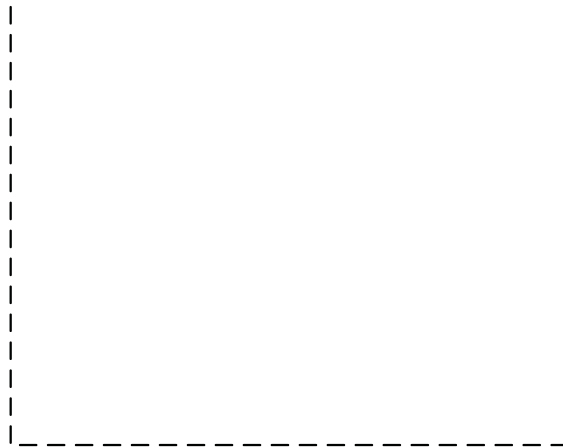
### Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

**Thermal Pad, PWRPAD**

For correct operation, the power pad (PWRPAD) is connected to the  $V_{SS}$  terminal on the printed circuit board.

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V1–VSS or V2–VSS or V3–VSS	–0.3 to 30 V
	V3–V2 or V2–V1	–0.3 to 8 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, $P_{TOT}$		See package dissipation rating.
Functional temperature		–65 to 110°C
Storage temperature range, $T_{STG}$		–65 to 150°C
Lead temperature (soldering, 10 s), $T_{SOLDER}$		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These stresses are for absolute maximum ratings only. (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These stresses are for absolute maximum ratings only.


## DC CHARACTERISTICS

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 10.8\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$  to  $15\text{ V}$  (unless otherwise noted).

	Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Voltage Protection Threshold VCx</b>							
1.0	$V_{OV}$	$V_{(PROTECT)} - \text{Overvoltage Detection}$	bq294502, fixed delay 4 s		4.35		V
1.1			bq294504, fixed delay 6.5 s		4.35		V
1.2			bq294512, fixed delay 4 s		4.40		V
1.3			bq294515, fixed delay 4 s		4.425		V
1.4			bq294522, fixed delay 4 s		4.45		V
1.5			bq294524, fixed delay 6.5 s		4.45		V
1.6			bq294532, fixed delay 4 s		4.50		V
1.7			bq294562, fixed delay 4 s		4.25		V
1.8			bq294572, fixed delay 4 s		4.00		V
1.9			bq294582, fixed delay 4 s		4.225		V
1.10			bq294584, fixed delay 6.5 s <sup>(1)</sup>		4.225		V
1.11	bq294592, fixed delay 4 s		4.30		V		
1.12	$V_{HYS}$	Overvoltage Detection Hysteresis		250	300	400	mV
1.13	$V_{OA}$	OV Detection Accuracy	$T_A = 25^\circ\text{C}$	-10		10	mV
1.14	$V_{OA-DRIFT}$	OV Detection Accuracy due to Temperature	$T_A = -40^\circ\text{C}$ $T_A = 0^\circ\text{C}$ $T_A = 60^\circ\text{C}$ $T_A = 110^\circ\text{C}$	-40 -20 -24 -54		44 20 24 54	mV mV mV mV
<b>Supply and Leakage Current</b>							
1.15	$I_{CC}$	Supply Current	$(V3-V2) = (V2-V1) = (V1-VSS) = 4.0\text{ V}$ (See Figure 11 for reference) $(V3-V2) = (V2-V1) = (V1-VSS) = 2.8\text{ V}$ with $T_A = -40^\circ\text{C}$ to $60^\circ\text{C}$		1	2	$\mu\text{A}$
1.16	$I_{IN}$	Input Current at Vx Pins	Measured at V3, V2, and V1 = 4.0 V $(V2-V1) = (V1-VSS) = 4.0\text{ V}$ $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$ (See Figure 11 for reference.)	-0.1		0.1	$\mu\text{A}$
<b>Output Drive OUT</b>							
1.17	$V_{OUT}$	Output Drive Voltage	$(V3-V2)$ or $(V2-V1)$ or $(V1-VSS) > V_{OV}$ $V_{DD} = 7.2\text{ V}$ , $I_{OH} = 100\text{ }\mu\text{A}$ , $T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	6			V
1.18			Two of the three cells are short circuit and only one cell is powered $(V3-V2)$ or $(V2-V1)$ or $(V1-VSS) > V_{OV}$ $V_{DD} = V_x$ (Cell voltage), $I_{OH} = 100\text{ }\mu\text{A}$ , $T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$		$V_{DD} - 0.2$		V
1.19			$(V3-V2)$ , $(V2-V1)$ , and $(V1-VSS) < V_{OV}$ , $I_{OL} = 100\text{ }\mu\text{A}$ , $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$		250	400	
1.20	$I_{OUT(Short)}$	OUT Short Circuit Current	OUT = 0 V ( $V3-V2$ ) or $(V2-V1)$ or $(V1-VSS) > V_{OV}$			4.5	mA
1.21	$t_R$	Output Rise Time	CL = 1 nF, $V_{OH(OUT)} = 0\text{ V}$ to $5\text{ V}$ <sup>(2)</sup>		5		$\mu\text{s}$
1.22	$Z_O$	Output Impedance			2	5	k $\Omega$
<b>Fixed Delay Timer</b>							
1.23	$t_{DELAY}$	Fault Detection Delay Time	Fixed Delay, bq2945x2 Fixed Delay, bq2945x4	3.2 5.2	4 6.5	4.8 7.8	s

(1) Product Preview only

(2) Specified by design. Not 100% tested in production.

## DC CHARACTERISTICS (continued)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 10.8\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$  and  $V_{DD} = 3\text{ V}$  to  $15\text{ V}$  (unless otherwise noted).

	Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Voltage Protection Threshold VCx</b>							
1.24	$t_{\text{DELAY\_CTM}}$	Fault Detection Delay Time in Test Mode	Fixed delay (Internal settings)		15		ms

## TYPICAL CHARACTERISTICS

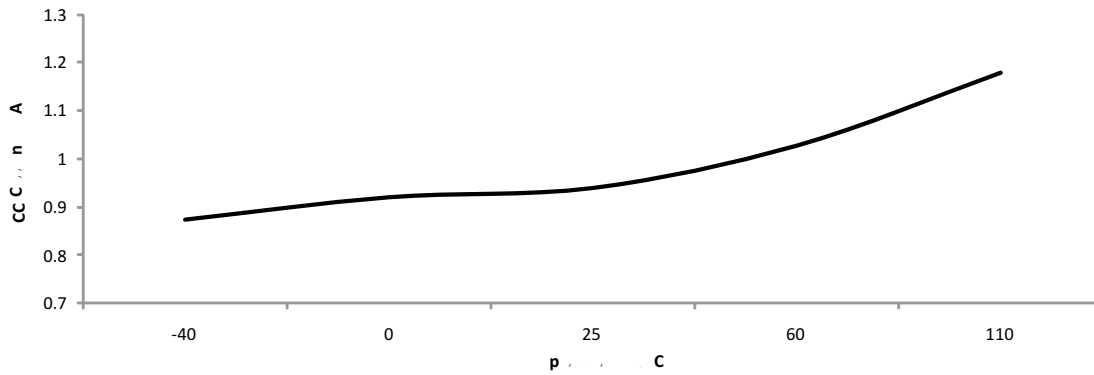


Figure 2.  $I_{CC}$  Current Consumption Versus Temperature

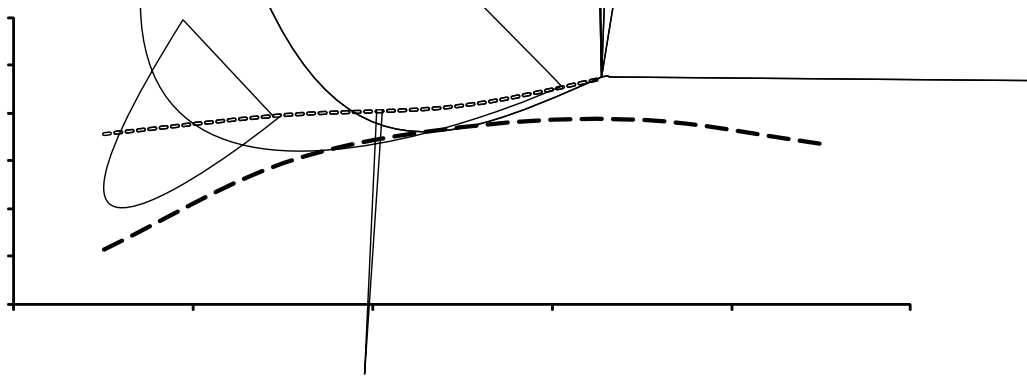


Figure 3. bq294502 Overvoltage Threshold (OVT) vs. Temp

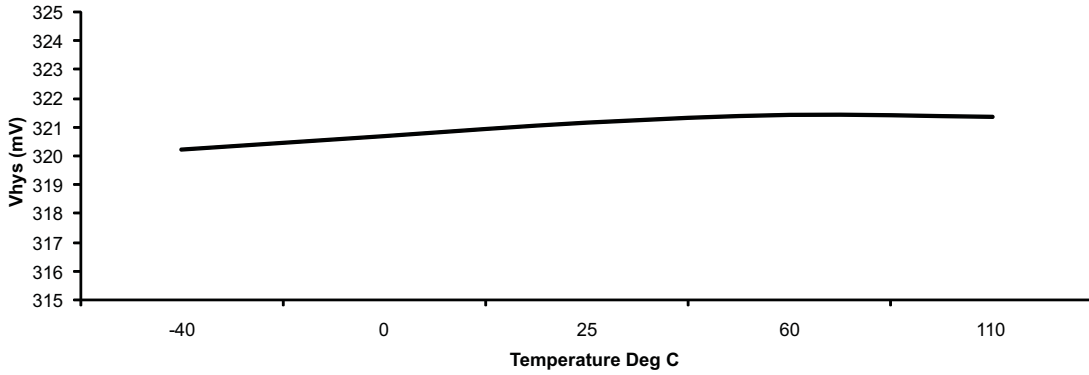


Figure 4. Hysteresis  $V_{HYS}$  Versus Temperature

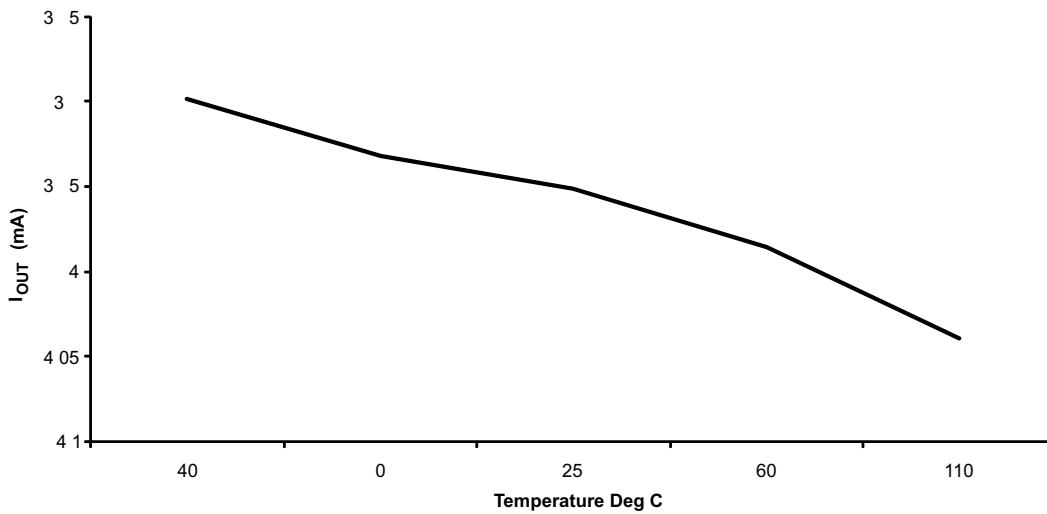


Figure 5. Output Current  $I_{OUT}$  Versus Temperature

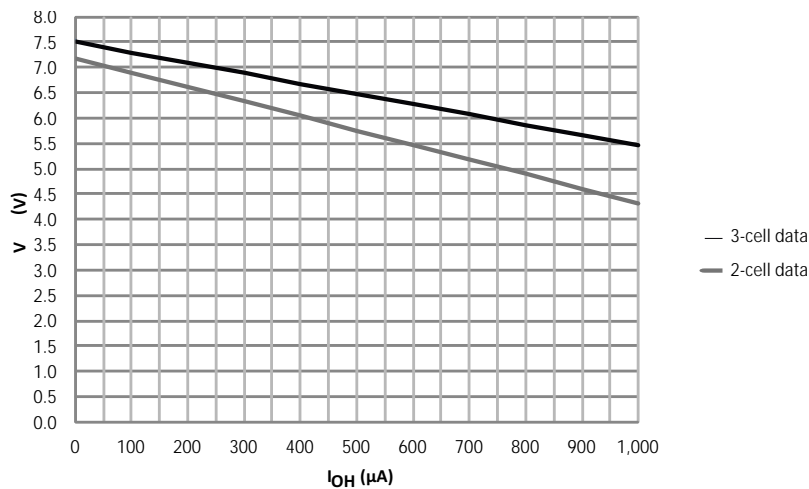


Figure 6. Output Voltage Versus Output Current

## APPLICATION INFORMATION

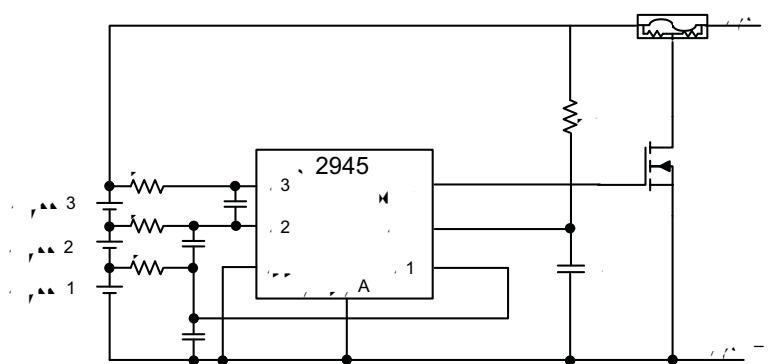


Figure 7. Application Configuration

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 7 shows each external component.

Table 1. Parameters

PARAMETER	External Component	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	$\Omega$
Voltage monitor filter capacitance	CIN	0.01		0.1	$\mu\text{F}$
Supply voltage filter resistance	RVD	100		1K	$\Omega$
Supply voltage filter capacitance	CVD		0.1		$\mu\text{F}$

## APPLICATION SCHEMATIC

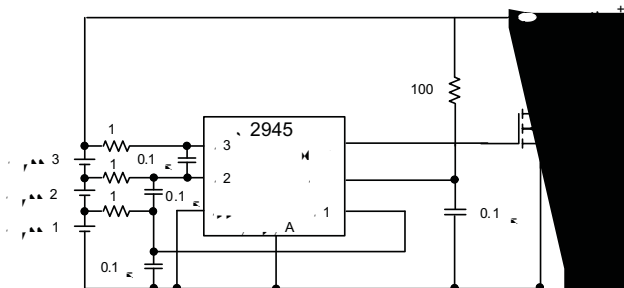


Figure 8. 3-Series Cell Configuration with Fixed Delay

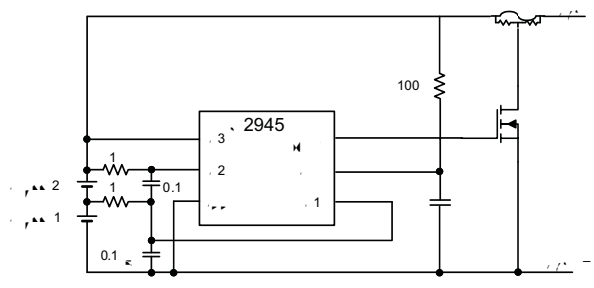


Figure 9. 2-Series Cell Configuration with Internal Fixed Delay

## CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V3 (see Figure 10). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to VC3 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

### CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

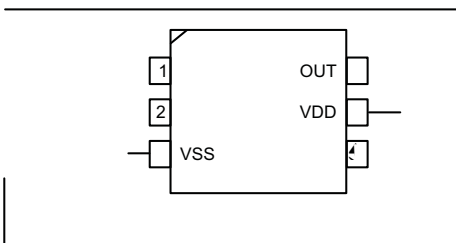


Figure 10 shows the timing for the Customer Test Mode.

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**Figure 10. Timing for Customer Test Mode**

Figure 11 shows the measurement for current consumption for the product for both VDD and Vx.



**Figure 11. Configuration for IC Current Consumption Test**

## REVISION HISTORY

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### Changes from Original (September 2011) to Revision A Page

- Added the bq294582 Device to Production Data ..... 2
- 

### Changes from Revision A (November 2011) to Revision B Page

- Changed the bq294504 Device to Production Data ..... 1
  - Added the bq294512 Device ..... 1
  - Added the bq294592 Device ..... 1
  - Added a second I<sub>CC</sub> Test Condition ..... 5
  - Changed Fault Detection Delay Time in bq2945x4 Test Mode Specifications ..... 5
- 

### Changes from Revision B (February 2012) to Revision C Page

- Added the bq294515 Device to Production Data ..... 2
  - Added the bq294524 Device to Production Data ..... 2
  - Added the bq294532 Device to Production Data ..... 2
  - Added the bq294572 Device to Production Data ..... 2
  - Changed Overvoltage Detection Hysteresis ..... 5
  - Added Output Voltage Versus Output Current graphic ..... 7
  - Changed Timing for Customer Test Mode figure ..... 9
-

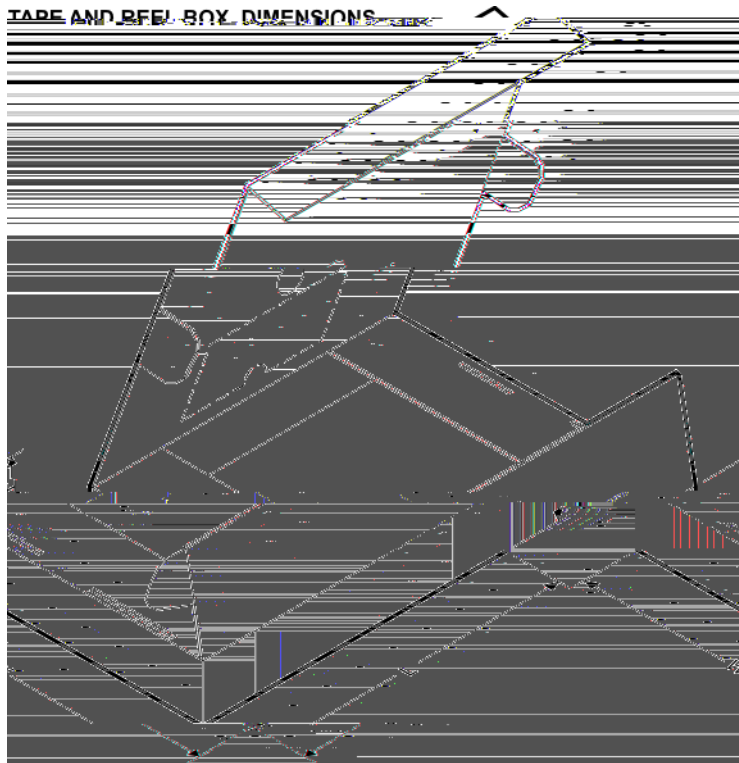




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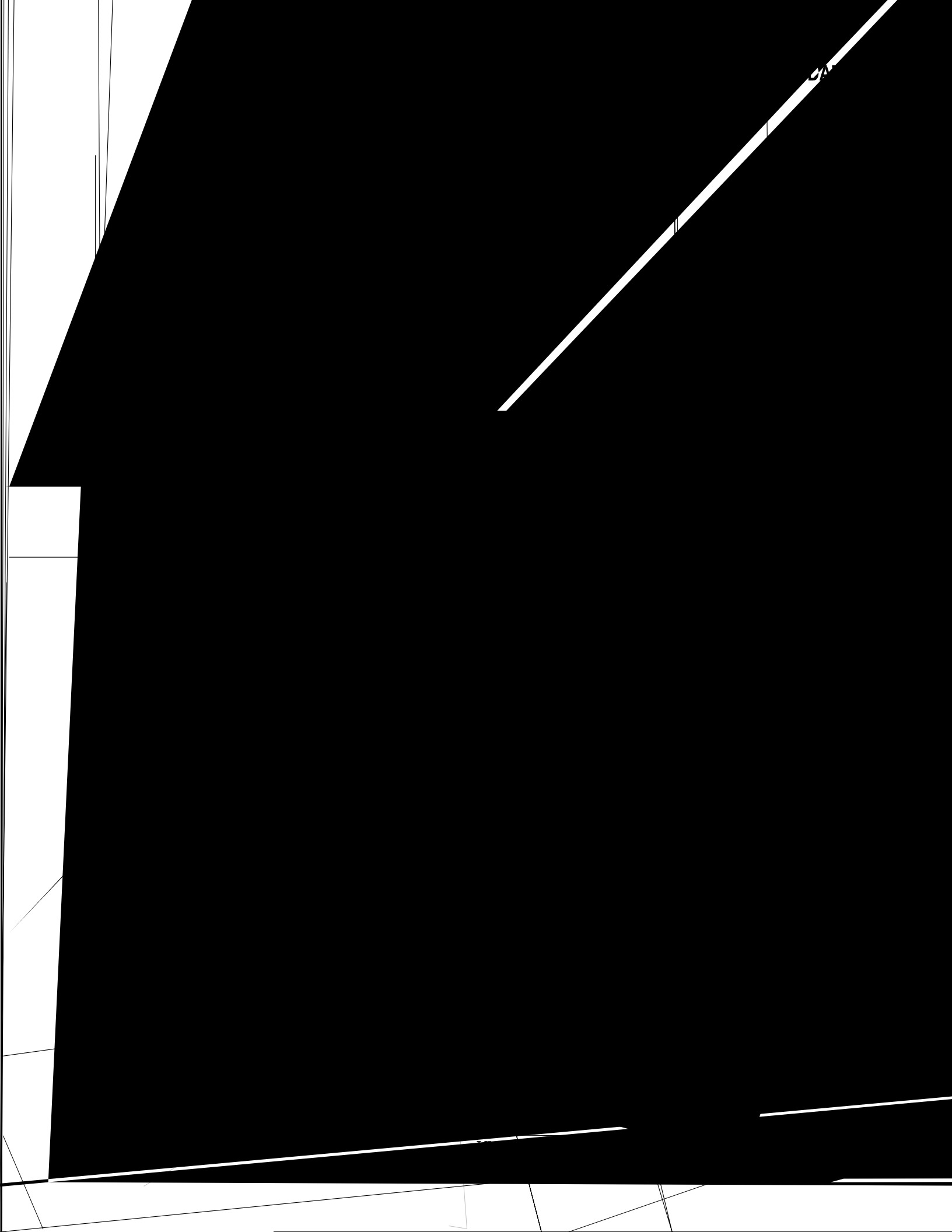
## PACKAGE OPTION ADDENDUM





\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294502DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294502DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVR	SON	DRV	6	0	367.0	367.0	35.0
BQ294504DRVT	SON	DRV	6	0	210.0	185.0	35.0
BQ294512DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294512DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294522DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294522DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294524DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294532DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294582DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294592DRVT	SON	DRV	6	250	210.0	185.0	35.0

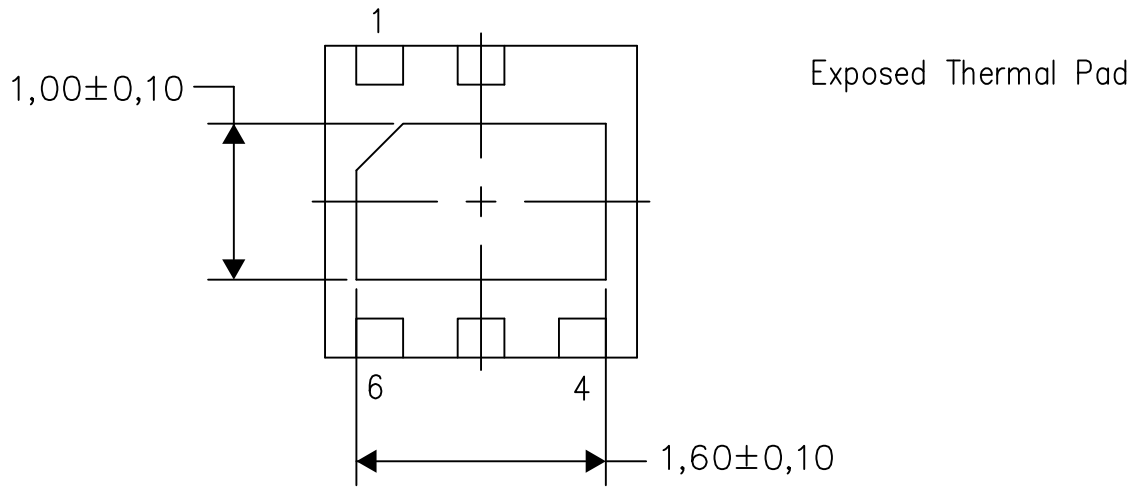


# PLASTI

s package incorporates an exposed thermal pad that is designed to be attached directly to an external

pecial heatsink structure designed into the PC

For information on the Quad Flatpack No-Lead (QFN) package and its advantages

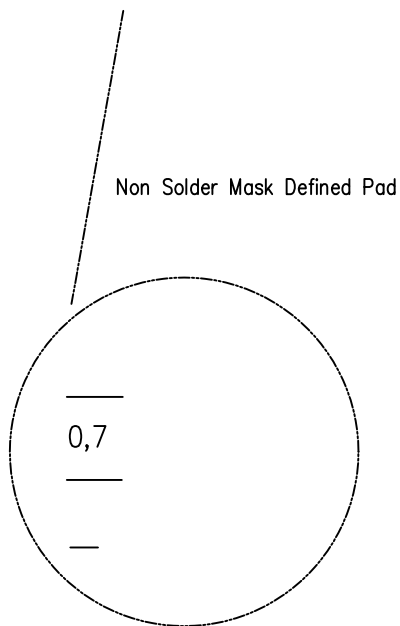


Bottom View

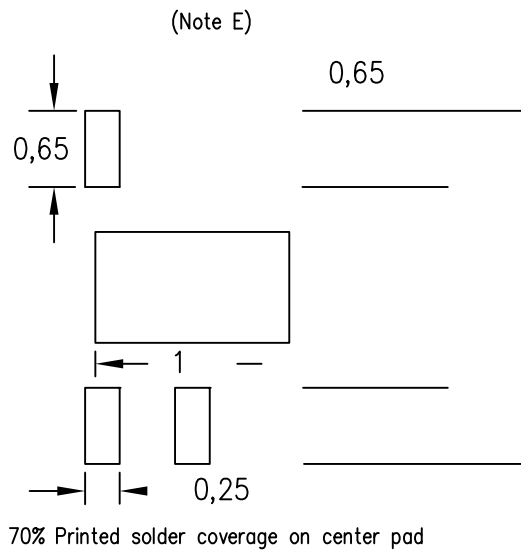
Exposed Thermal Pad Dimensions

NOTE: All linear dimensions are in millimeters





Note D



C. Publication IPC-7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These

Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations and board fabrication site for solder mask tolerances.

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### Applications

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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