Super Capacitor Manager

Check for Samples: bq33100

FEATURES

- **Fully Integrated 2, 3, 4 and 5 Series Super Capacitor Manager**
- **Can Be Used With Up To 9 Series Capacitors Without Individual Integrated Capacitor Monitoring & Balancing**
- **Active Capacitor Voltage Balancing**
  - **Prevents Super Capacitor Overvoltage during Charging**
- **and Capacitor Health Monitoring**
  - **Capacitance Learning**
  - **ESR Measurement**
  - **Operation Status**
  - **State of Charge**
  - **State of Health**
  - **Charging Voltage and Current Reports**
  - **Safety Alerts with Optional Pin Indication**
- **Integrated Protection Monitoring and Control**
  - **Over Voltage**
  - **Short Circuit**
  - **Excessive Temperature**
  - **Excessive Capacitor Leakage**
- **2 Wire SMBus Serial Communications**
- **High-Accuracy 16-Bit Delta-Sigma ADC With a 16-Channel Multiplexer for Measurement**
  - **Used for Voltage, Current and Temperature**
- **Low Power Consumption**
  - **<450uA in Normal Operating Mode**
  - **<1uA in Shutdown Mode**
- **Wide Operating Temperature: -40°C to +85°C**

APPLICATIONS

- **Battery Backup Replacement**
- **Cache Controllers**
- **RAID Systems**
- **Server Blade Cards**
- **UPS**
- **Medical and Test Equipment**
- **Portable Instruments**

DESCRIPTION

The Texas Instruments bq33100 Super Capacitor Manager is a fully integrated, single-chip, solution that provides a rich array of features for managing, charge control, monitoring, and protection, for either 2, 3, 4 or 5 series Super Capacitors with individual capacitor monitoring and balancing or up to 9 series capacitors with only the stack voltage being measured. With a small footprint of 7.8 x 6.4 mm in a compact 24-pin TSSOP package, the bq33100 maximizes functionality and safety while dramatically increasing ease of use and cutting the solution cost and size for Super Capacitor applications.

Using its integrated high-performance analog peripherals, the bq33100 measures and maintains an accurate record of available capacitance, state-of-health, voltage, current, temperature, and other critical parameters in Super Capacitors, and reports the information to the system host controller over a 2-wire SMBus 1.1 compatible interface.

The bq33100 provides firmware controlled protection on overvoltage, overtemperature, and overcharge along with hardware controlled protection for overcurrent in discharge and short circuit protection during charge and discharge.

ORDERING INFORMATION

T_A	AGE	
	24 PIN TSSOP (PW) Tube	24 PIN TSSOP (PW) Tape & Reel
–40°C to 85°C	bq33100PW(1)	bq33100PWR(2)

(1) A single tube quantity is 60 units.
(2) A single reel quantity is 2000 units

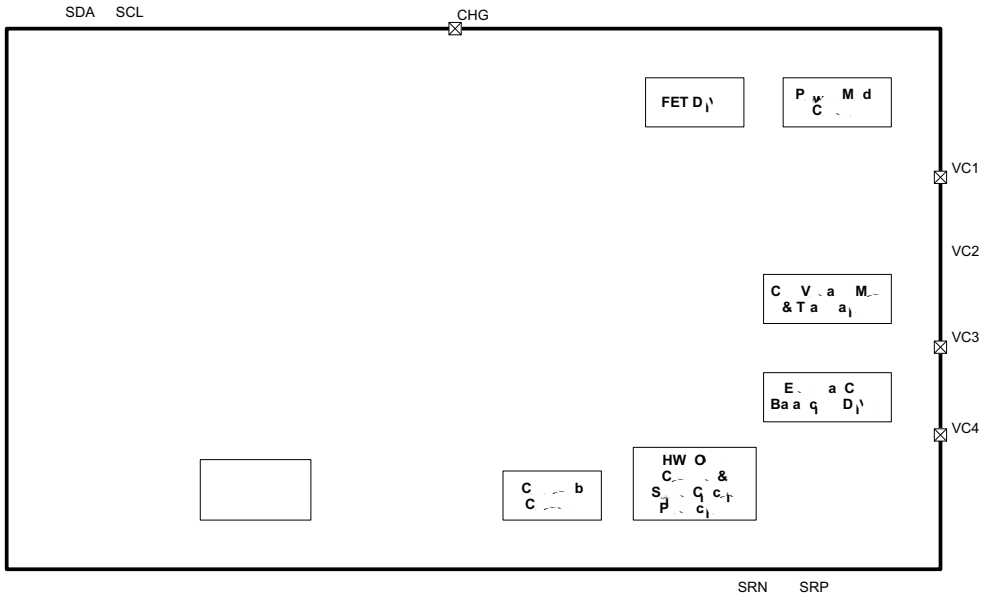
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small paral(failmay.)Tj 26.51 0 Td (Prec4s)Tj 27.39uits

Table 1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	22	-	No connect, leave pin floating
CHG	23	O	P-Channel FET drive for controlling charge
VCC	24	P	Positive input from power supply

SYSTEM PARTITIONING DIAGRAM



ELECTRICAL CHARACTERISTICS

GENERAL PURPOSE I/O

Typical values stated where T_A = 25°C and VCC = VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85°C and VCC = VCC = 3.8V to 25V (unless otherwise noted)

PARAMETER T BT /F1 8 Tf 100 Tz 0 0 0 rg 111.8z 0 0 f 0 rg 4 660.4g 111.8z 0 0 f 009 0 Td l			

LOW FREQUENCY OSCILLATOR

Typical values stated where T_A = 25°C and VCC = VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85°C and VCC = VCC = 3.8V to 25V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		MHz
$f_{(LEIO)}$	Frequency error(1)	T_A = –20°C to 70°C	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time(2)	T_A = –25°C to 85°C			100	ms

(1) The frequency drift is included and measured from the trimmed frequency at VCC = VCC = 14.4 V, T_A = 25°C.
(2) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

RAM BACKUP

Typical values stated where T_A = 25°C and VCC = VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85°C and VCC = VCC = 3.8V to 25V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	$V_{RBI} > V_{(RBI)MIN}$, $V_{REG27} < V_{REG27IT-}$, T_A = 70°C to 110°C		20	1500	nA
		$V_{RBI} > V_{(RBI)MIN}$, $V_{REG27} < V_{REG27IT-}$, T_A = –40°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage(1)		1			V

(1) Specified by design. Not production tested.

FLASH

Typical values stated where T_A = 25°C and VCC = VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85°C and VCC = VCC = 3.8V to 25V (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention		10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				250	ms
$t_{(PAGEERASE)}$	Page-erase time				25	ms
$I_{CC(PROG)}$	Flash-write supply current			4	6	mA
$I_{CC(ERASE)}$	Flash-erase supply current	T_A = –40°C to 0°C		8	22	mA
		T_A = 0°C to 85°C		3	15	

(1) Specified by design. Not production tested

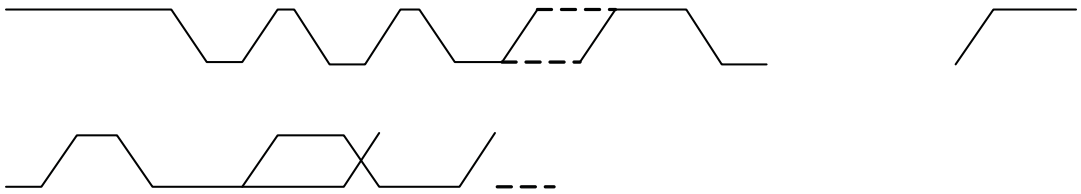
CURRENT PROTECTION THRESHOLDS

Typical values stated where T_A = 25°C and VCC = VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85 25°

SMBus

Typical values stated where T_A = 25°C and VCC = VCC = 14.4V, Min/Max values stated where T_A = -40°C to 85°C and VCC = VCC = 3.8V to 25V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus operating frequency	Slave mode, SCL 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4.0			µs
$t_{SU:STA}$	Repeated start setup time					



OVERVIEW

Note: The CC0...CC2 bits in Operation Cfg should be programmed to match the corresponding configuration.

When in Stack mode (Operation Cfg [STACK] =1) VC1 should be connected to VC2 and VC3 connected to VC4. Additionally a 'divide by 2' resistor divider should be connected between the top and bottom of the capacitor array with VC1,2 being the top and VC3,4 being the middle and VSS being the bottom. In this configuration pins VC5 and VC5BAL are not used and should be connected to VSS.

Charge Control Features

The bq33100 charge control features can report the appropriate charging voltage and charging current via communications bus if host or charge controller requires. The bq33100 can also report charging status and faults through status registers and, optionally, the FAULT pin.

CHG Over Ride Control

The CHG output of the bq33100 is typically controlled automatically but can be over ridden through the CHGOR pin (pin 21). On a low -to-high transition the CHG output is released turning off the external CHG FET and on a high-to-low transition the CHG output is pulled low after a programmable delay.

Note: The CHG FET will remain OFF until *OperationStatus [LTE]* is set or through control via the SMBus command *FETControl*. Once *[LTE]* is set then CHG will be controlled automatically.

Capacitor Voltage Balance Control

During charging and when in Normal mode, this feature reduces the voltage difference of the Super Capacitors gradually using a voltage-based balancing algorithm. This prevents fully charged capacitors from overcharging and causing excessive degradation and also increases the usable energy by preventing premature charge termination.

If voltage balancing is required a voltage threshold can be set up for voltage balancing to be active. When balancing the bq33100 control allows a weak, internal pull-down for VC1 to VC4 pin. The purpose of this weak pull-down is to enable an external FET for current bypass. Series resistors placed between the input VC1 to VC4 pins and the positive Super Capacitor terminals, control the V_{GS} of the external FET. The lowest capacitor is slightly different and uses the VC5BAL output to enable the capacitor bypass

Lifetime Data Logging Features

The bq33100 offers limited lifetime data logging for the following critical Super Capacitor parameters for analysis purposes:

- Lifetimlifetimfer3 /F2 10 Tf **Lifetime Datafor** Tf 10Lifetime

Td (SLUS987A)Tj /F3 7 Tf 36.2 0397509.8)

SMBus On and Off State

The bq33100 detects a SMBus off state when SCL and SDA are logic-low for ≥ 2 seconds. Clearing this state requires either SCL or SDA to transition high. Within 1 ms, the communication bus is available.

Power Modes

The bq33100 supports 2 different power modes:

- In Normal Mode, the bq33100 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq33100 is in a reduced power mode.
- In Shutdown mode the bq33100 is powered down with only a voltage based wake function operating

NOTATIONAL CONVENTIONS

The following notation is used in this document, if SBS commands and Data Flash values are mentioned within a text block:

- SBS commands are set in italic, e.g., *Voltage*
- SBS bits and flags are capitalized, set in italic and enclosed with square brackets, e.g., *[SS]*
- Data Flash values are set in bold italic e.g., ***OV Threshold***
- All Data Flash bits and flags are capitalized, set in bold italic and enclosed with square brackets, e.g., ***[OV]***

All SBS commands, Data Flash values and flags mentioned in a chapter are listed at the beginning of that chapter.

Figure 1. Voltage as Current During Learning

Where:

$$C = I \times \left(t[D] - t[C]\right) / \left(V[C] - V[D]\right) \quad (1)$$

and

$$ESR = \left(V[A] - V[B]\right) / I \quad (2)$$

Main Monitoring Registers

Capacitance represents the total capacitance in the . The bq33100 computes capacitance in units of F (Farads).

On initialization, the bq33100 sets *Capacitance* to the data flash value stored in ***Initial Capacitance***. During subsequent learning cycles, the bq33100 updates *Capacitance* with the last measured capacitance of the . Once updated, the bq33100 writes the new *Capacitance* value to data flash to ***Capacitance***. *Capacitance* represents the full Super Capacitor reference for relative state of charge calculations.

InitialCapacitance — The first updated value of Super Capacitor capacitance and represented in units of F.

RelativeStateOfCharge (RSOC) represents the % of available energy and is calculated by:

Capacitance * (*Voltage* - ***Vmin***) / (Vcharging - ***Vmin***)

Learning Frequency — The Learning Frequency register sets the time between automatic learning cycles of the Super Capacitor which can also be manually executed by issuing a *ManufacturerAccess Learn* command. The bq33100 uses the learning cycles to measure the Super Capacitor capacitance and update the Capacitance register accordingly.

Initial Capacitance at Device Reset

The bq33100 estimates the initial capacitance of a at device reset, which is the case when the capacitors are first attached to the application circuit. This gives a reasonably accurate Capacitance and RSOC value, however, Super Capacitor capacitance learning is required in order to improve the accuracy of Capacitance and RSOC.

Qualified Capacitance Learning

The bq33100 updates Capacitance with an amount based on the value learned during a qualified learning cycle. Once updated, the bq33100 writes the new *Capacitance* value to data flash to ***Capacitance***.

The bq33100 sets *[CL]* = 1 and clears *[LPASS]* in *Operation Status* when a qualified capacitance learning cycle begins. The period of time that the learning takes is set by ***CL Time*** although the first learning cycle after a device reset will not occur until after an elapsed time of ***Learning Frequency***. When a qualified learn has occurred *[LPASS]* in *Operation Status* is set.

During the learning process there are specific timeouts to protect from over charge or over discharge of the super capacitor array. At the beginning of each phase of charge and discharge a timer is started. If the timer exceeds ***Max Discharge Timeout*** during the discharging phase then *Operation Status [LDTO]* is set if the timer exceeds ***Max Charge Timeout*** for the charging phase then *Operation Status [LCTO]* is set. the flags are cleared upon the beginning of the next learning cycle.

During capacitance learning both capacitor voltage balancing operations and overvoltage detection are suspended.

Health Determination

The bq33100 uses the following method to determine the relative health of the capacitor.

Health = (*Capacitance* / *InitialCapacitance*)

The bq33100 will determine a new *ChargingVoltage* at end of the learning cycle based on the newly learned *Capacitance*. The following warnings will be set based on the changes in *ChargingVoltage* and the capacitors ability to provide the minimum power needs.

ChargingVoltage = ***V Chg Nominal*** then *SafetyStatus[HLOW]*, *[HWARN]* and *[HFAIL]* are cleared.

If *ChargingVoltage* is set to ***V Chg A*** or ***V Chg B*** then *SafetyStatus[HLOW]* is set.

If *ChargingVoltage* is set to ***V Chg Max*** then *SafetyStatus [HWARN]* is set.

If *ChargingVoltage* is set to ***V Chg Max*** and the bq33100 determines that the newly learned *Capacitance* cannot provide the minimum power requirements then *SafetyStatus [HFAIL]* is set.

The minimum ill

Capacitor Voltage Balancing

Capacitor voltage balancing in the bq33100 is accomplished by connecting an external parallel bypass load to each capacitor, and enabling the bypass load depending on each individual capacitors voltage level. The bypass load is typically formed by a P-ch MOSFET and a resistor connected in series across each capacitor. The filter resistors that connect the capacitor tabs to VC1~VC4 pins of the bq33100 are required to be 1k ohms to support this function on all capacitors other than the lowest. The lowest capacitor bypass is enabled via the VC5BAL pin. Capacitor Voltage Balancing is only operational after the *ManufacturerAccess* Lifetime & Capacitor Balancing Enable (0x21) command is sent to the bq33100.

Using this circuit, the bq33100 balances the capacitors during charge and after charge termination by discharging those capacitors with voltage above the threshold set in ***CB Threshold*** and if the ΔV in capacitor voltages exceeds the value programmed in ***CB Min***. During capacitor voltage balancing, the bq33100 measures the capacitor voltages periodically (during which time the voltage balancing circuit is turned off) and based on the capacitor voltages, the bq33100 selects the appropriate capacitor to discharge. When ΔV of *CapacitorVoltage5...1* < ***CB Min*** then capacitor voltage balancing stops. Capacitor voltage balancing restarts when ΔV of *CapacitorVoltage5...1* ≥ ***CB Restart*** to avoid balancing start-stop oscillations.

Capacitor voltage balancing only occurs when:

- Charging current is detected (*Current* > ***Chg Current Threshold*** OR
- The *[FC]* flag in *OperationStatus* has been set AND
- Δ*CapacitorVoltage5...1* ≥ ***CB Restart***

Capacitor voltage balancing stops when:

- Δ*CapacitorVoltage5...1* < ***CB Min***
- Discharging current detected (*Current* > ***Dsg Current Threshold***)

This feature is disabled when in Stack mode, when ***Operation Cfg [STACK]*** =1.

Charge Control

The bq33100 supports two main charge control architectures, discrete control and smart control. In a discrete charge control implementation the CHGLVL0 and CHGLVL1 pins can be used to adjust the charging voltage of an external supply (see reference schematic for example).

As the super capacitors age a higher charging voltage can be configured to offset the deteriorating super capacitor ESR and Capacitance due to aging. With the discrete control method there are 4 levels of charging voltages that can be chosen, ***V Chg Nominal***, ***V Chg A***, ***V Chg B*** and ***V Chg Max***. The setting of the charging voltage is determined by the value of the latest determined required *Charging Voltage*.

The CHGLVL0 and CHGLVL1 pin states are defined by the V Chg X parameters selected per the following table:

ChargingVoltage	CHGLVL1 (pin 12)	CHGLVL0 (pin11)
V Chg Nominal	0	0
V Chg A	0	1
V Chg B	1	0
V Chg Max	1	1

In a smart control architecture the bq33100 makes the appropriate maximum charging current and charging voltage per the charging algorithm available via the *ChargingCurrent* and *ChargingVoltage* SMBus commands respectively. This enables either an SMBus master or smart charger to manage the charging of the super capacitor pack.

Primary Charge Termination

The bq33100 determines charge termination if:

- The average charge current < ***Taper Current*** during 2 consecutive ***Current Taper Window*** time periods, AND
- *Voltage* + ***Taper Voltage*** ≥ *ChargingVoltage*

NOTE: To make sure that the charge terminates properly, it is recommend that ***Taper Current*** be set to a value greater than the maximum charger voltage inaccuracy

The bq33100 sets the *[FC]* flag in *Operation Status* when a valid charge termination occurs and cleared when *RelativeStateOfCharge* is less than 98%.

CHG Over Ride Control

During the normal operation of the bq33100 the CHG output of the bq33100 is typically controlled automatically but can be over ridden through the CHGOR pin (pin 21). On a low -to-high transition the CHG output is released turning off the external CHG FET and on a high-to-low transition the CHG output is pulled low after a programmable delay ***CHG Enable Delay***. If ***CHG Enable Delay*** is programmed to 0 the delay is a maximum of 250ms. If the CHG over ride function is not needed then the CHGOR pin should be connected to VSS.

Lifetime Data Gathering

Lifetime Maximum Temperature

During the operation lifetime of the bq33100 it gathers temperature data. During this time the bq33100 can be enabled to record the Maximum value that the measured temperature reached. If the [*LTE*] flag is set in *OperationStatus*, ***Lifetime Max Temp*** value is updated if one of the following conditions are met:

- internal measurement temperature - ***Lifetime Max Temp*** > 1 °C.
- internal measurement temperature > ***Lifetime Max Temp*** for a period > 60 seconds
- internal measurement temperature > ***Lifetime Max Temp*** AND any other lifetime value is updated.

Table 3. Lifetime Maximum Temperature

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
59	Lifetime Data	0	Lifetime Max Temp	Integer	2	0	1400	350	0.1 degC

Lifetime Minimum Temperature

During the operation lifetime of the bq33100 it gathers temperature data. During this time the bq33100 can be enabled to record the Minimum value that the measured temperature reached. If the [*LTE*] flag is set, ***Lifetime Min Temp*** is updated if one of the following conditions are met:

- ***Lifetime Min Temp*** - internal measurement temperature > 1 °C.
- ***Lifetime Min Temp*** > internal measurement temperature for a period > 60 seconds
- ***Lifetime Min Temp*** > internal measurement temperature > AND any other lifetime value is updated.

Table 4. Lifetime Minimum Temperature

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
59	Lifetime Data	2	Lifetime Min Temp	Integer	2	-600	1400	50	0.1 degC

Lifetime Maximum Capacitor Voltage

During the operation lifetime of the bq33100 it gathers voltage data and if in Single mode (***Operation Cfg [STACK]*** =0). During this time the bq33100 can be enabled to record the Maximum value that the measured voltage reached. If the [*LTE*] flag is set, ***Lifetime Max Capacitor Voltage*** is updated if one of the following conditions are met:

- any internally measured capacitor voltage - ***Lifetime Max Capacitor Voltage*** > 25 mV
- any internally measured capacitor voltage > ***Lifetime Max Capacitor Voltage*** for a period > 60 seconds
- any internally measured capacitor voltage ***Lifetime Max Capacitor Voltage*** AND any other lifetime value is updated.

Table 5. Lifetime Max Capacitor Voltage

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
59	Lifetime Data	4	Lifetime Max Capacitor Voltage	Integer	2	0	32767	0	mV

Safety Detection Features

The bq33100 supports a wide range of Super Capacitor and system safety detection and protection features that are easily configured or enabled via the integrated data flash. These features are intended, through various configuration options, to provide a level of safety from external influences causing damage to components with the power path, eg: limiting the period of time the CHG FET is exposed to high current pulse charge conditions

Capacitor Overvoltage (OV)

The bq33100 can detect capacitor overvoltage condition and protect capacitors from damage.

When any *CapacitorVoltage5...1* exceeds (*ChargingVoltage* / number of capacitors (see ***Operation Cfg [CC2,1,0]***) + ***OV Threshold***) the *[OV]* flag in *SafetyAlert* is set.

When any *CapacitorVoltage5...1* exceeds (*ChargingVoltage* / number of capacitors (see ***Operation Cfg [CC2,1,0]***) + ***OV Threshold***) for a period greater than ***OV Time*** the *[OV]* flag in *SafetyStatus* is set.

When the bq33100 is configured for Pack Mode, when ***Operation Cfg [PACK]*** =1, then a fault is detected when *Voltage* exceeds (*ChargingVoltage* + ***OV Threshold***) the *[OV]* flag in *SafetyAlert* is set.

When the bq33100 is configured for Pack Mode, when ***Operation Cfg [PACK]*** =1, then a fault is detected when *Voltage* exceeds (*ChargingVoltage* + ***OV Threshold***) for a period greater than ***OV Time*** the *[OV]* flag in *SafetyStatus* is set.

This function is disabled if ***OV Time*** is set to zero.

In an overvoltage condition charging is disabled and the CHG FET is turned off, *ChargingCurrent* and *ChargingVoltage* are set to zero.

The bq33100 recovers from a capacitor overvoltage condition if all *CapacitorVoltages5..1* are equal to or lower than (*ChargingVoltage* / number of capacitors (see ***Operation Cfg [CC2,1,0]***) + ***OV Recovery***. If the bq33100 is configured for Pack Mode then the recover occurs when *Voltage* is equal to or lower than (*ChargingVoltage* + ***OV Recovery***.

On recovery the *[OV]* flag is reset, and *ChargingCurrent* and *ChargingVoltage* are set back to appropriate values per the charging algorithm.

Note: When *ChargingVoltage* has been set to 0 due to a detected condition then the capacitor overvoltage function is suspended.

Capacitor Voltage Imbalance (CIM)

The bq33100 starts capacitor voltage imbalance detection when *Current* is less than or equal to ***CIM Current*** AND ALL *CapacitorVoltage5..1* > ***Min CIM Check Voltage***. This function only operates when the bq33100 is in Normal mode, when ***Operation Cfg [PACK]*** =0.

When the difference between highest capacitor voltage and lowest capacitor voltage exceeds ***CIM Fail Voltage*** the *[CIM]* flag in *SafetyAlert* is set.

When the difference between highest capacitor voltage and lowest capacitor voltage exceeds ***CIM Fail Voltage*** for a period greater than ***CIM Time*** the *[CIM]* flag in *SafetyStatus* is set and *ChargingCurrent* and *ChargingVoltage* are set to 0 and the CHG FET is turned off.

This function is disabled if ***CIM Time*** is set to zero.

The capacitor voltage imbalance detection is cleared when the difference between highest capacitor voltage and lowest capacitor voltage is less than ***CIM Fail Voltage***. When this is detected then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[CIM]* flag in *SafetyStatus* is reset.

Weak Capacitor (CLBAD)

When the capacitor array has been fully charged (indicated by *OperationStatus [FC]* being set) then it is monitored for excessive leakage.

When *Current* exceeds ***CLBAD Current*** the *[CLBAD]* flag in *SafetyAlert* is set.

When *Current* exceeds ***CLBAD*** for a period greater than ***CLBAD Time*** the *[CLBAD]* flag in *SafetyStatus* is set.

This function is disabled if ***CLBAD Time*** is set to zero.

In a weak capacitor condition charging is disabled and the CHG FET is turned off, *ChargingCurrent* and *ChargingVoltage* are set to zero.

The weak capacitor fault is cleared when *Current* falls equal to or below the ***CLBAD Recovery*** limit. When the recovery condition is detected, then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[CLBAD]* flag in *SafetyStatus* is reset.

Overtemperature (OT)

The bq33100 has overtemperature protection to prevent charging at excessive temperatures.

When *Temperature* exceeds ***OT*** the *[OT]* flag in *SafetyAlert* is set.

When *Temperature* exceeds ***OT*** for a period greater than ***OT Time*** the *[OT]* flag in *SafetyStatus* is set.

This function is disabled if ***OT Time*** is set to zero.

In an overtemperature condition charging is disabled and the CHG FET is turned off, *ChargingCurrent* and *ChargingVoltage* are set to zero.

The overtemperature fault is cleared when *Temperature* falls equal to or below the ***OT Recovery*** limit. When the recovery condition is detected, then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[OT]* flag in *SafetyStatus* is reset.

Overcurrent During Charging (OC Chg)

The bq33100 has an independent level of recoverable overcurrent protection during charging.

When *Current* exceeds ***OC Chg*** the *[OCC]* flag in *SafetyAlert* is set.

When *Current* exceeds ***OC Chg*** for a period greater than ***OC Chg Time*** the *[OCC]* flag in *SafetyStatus* is set and *ChargingCurrent* and *ChargingVoltage* are set to 0.

This function is disabled if ***OC Chg Time*** is set to zero.

The overcurrent fault is cleared when *Current* falls below ***OC Chg Recovery***. When a charging-fault recovery condition is detected, then the CHG FET is allowed to be turned on, if other safety and configuration states permit, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[OCC]* flag in *SafetyStatus* is reset.

Overcurrent During Discharging (OC Dsg)

The bq33100 overcurrent is discharge detection executed by the integrated AFE is configured by the bq33100 data flash ***OC Dsg*** and ***OC Dsg Time*** registers.

When the integrated AFE detects a overcurrent in discharge condition the charge FET is turned off and the *[OCD]* flag in *SafetyStatus* is set, the internal current recovery timer is reset and *ChargingCurrent* and *ChargingVoltage* are set to 0.

The recovery is controlled by the bq33100 and requires that *Current* be ≤ ***OC Dsg Recovery*** threshold and that the internal AFE current recovery timer ≥ ***Current Recovery Time***.

When the recovery condition is detected, *ChargingCurrent* and *ChargingVoltage* are set to the appropriate value per the charging algorithm, and the *[OCD]* flag in*SafetyStatus* is reset.

Normal Mode - During normal operation, the bq33100 takes *Current*, *Voltage* and *Temperature* measurements, performs calculations, updates SBS data, and makes protection and status decisions at one-second intervals. Between these periods of activity, the bq33100 is in a reduced power state.

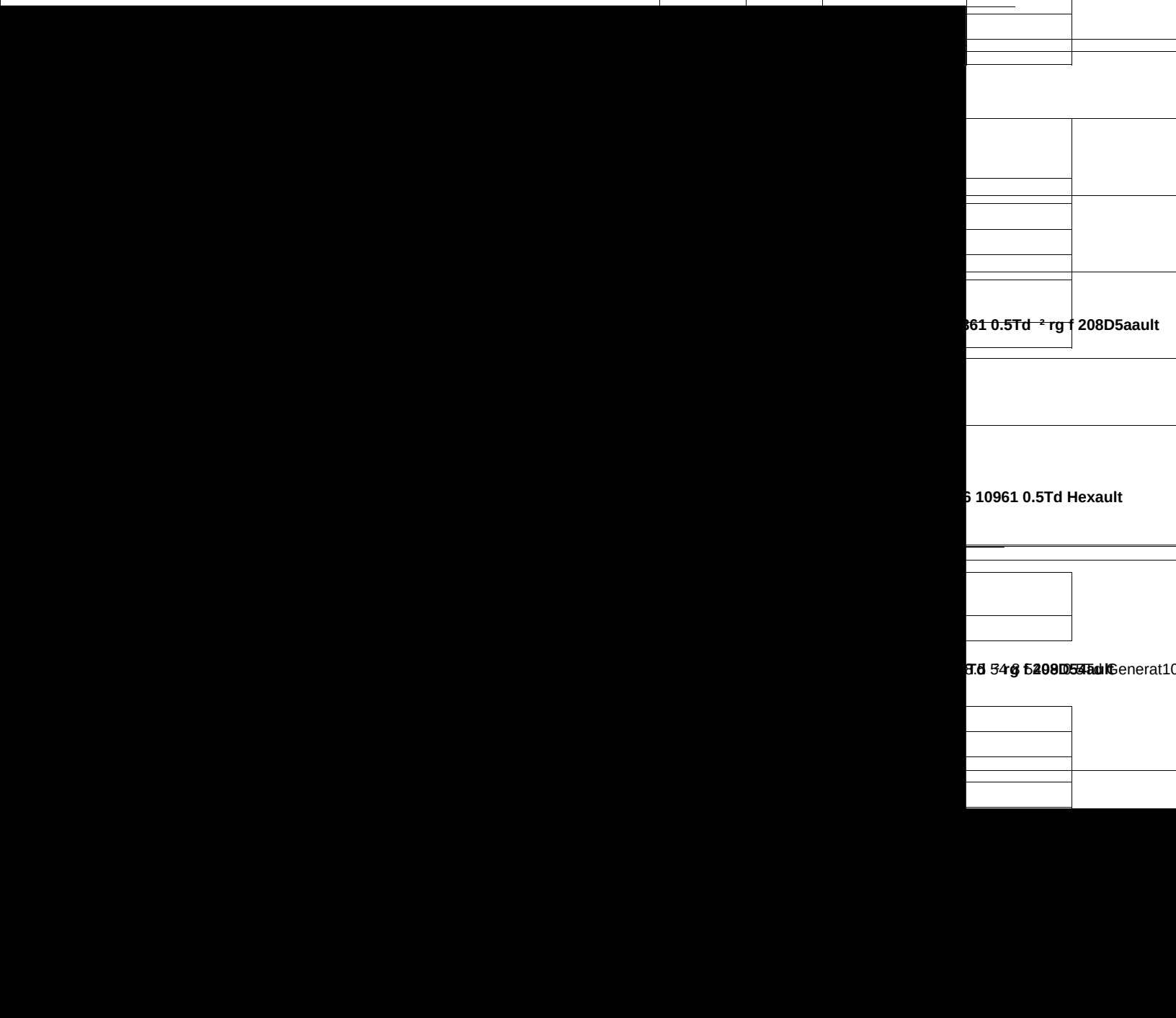
Shutdown - The bq33100 enters Shutdown mode if the following conditions are met:

- $V_{VCCPACK}$ ≤ Minimum Operating voltage
- *ManufacturerAccess*: *Shutdown* command received

Vaz rg f 24d (D)09e372 8 Tf 14ault

Cmd

Vaz rg f 24d (Def2BT 372 8 Tf 1R/WF1 8 Tf 100 Tz rgg f 208)Tj ET B0 rg .4 1372 8 Tf 1UnSealKey rg f 208



SBS

Cmd									

Bytes

Hardware Version k re 0 2e 0 [illegible] Tion

Learn Load Activation (0x0037)

This command drives the LLEN pin high. This command is only available when the bq33100 is in Unsealed mode.

Learn Load Clear (0x0038)

This command sets the LLEN pin back to low. This command is only available when the bq33100 is in Unsealed mode.

Calibration Mode (0x0040)

Places the bq33100 into calibration mode. This command is only available when the bq33100 is in Unsealed mode

Reset (0x0041)

The bq33100 undergoes a full reset. The bq33100 holds the clock line down for a few milliseconds to complete the reset. If *ChargingVoltage* < *Voltage* after a reset, then the pack is discharged using the capacitor voltage balancing circuitry. This command is only available when the bq33100 is in Unsealed mode.

Unseal Device *(UnsealKey)*

Instructs the bq33100 to enable access to the SBS functions and data flash space and clear the [SS] flag. This 2 step command needs to be written to *ManufacturerAccess* in the following order: 1st word of the UnSealKey followed by the 2nd word of the UnSealKey. If the command fails 4 seconds must pass before the command can be reissued. This command is only available when the bq33100 is in Sealed mode. See "Security" chapter in this document for detailed information.

Extended SBS Commands

Also available via *ManufacturerAccess* in sealed mode are some of the extended SBS commands. The result of these commands need to be read from *ManufacturerAccess* after a write to *ManufacturerAccess*.

Temperature (0x08)

This read-word function returns an unsigned integer value of the temperature in units of 0.1°K, as measured by the bq33100. It has a range of 0 to 6553.5°K. The source of the measured temperature is configured by the ***[TEMP1]*** and ***[TEMP0]*** bits in the ***Operation Cfg*** register.

Table 14. Temperature

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x08	R	Temperature	Unsigned Integer	2	0	65535	-	0.1°K

Voltage (0x09)

This read-word function returns an unsigned integer value of the sum of the individual Super Capacitor voltage measurements in mV with a range of 0 to 20000 mV

Table 15. Voltage

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x09	R	Voltage	Unsigned Integer	2	0	20000	-	mV

Current (0x0a)

This read-word function returns a signed integer value of the measured current being supplied (or accepted) by the super capacitor pack in mA, with a range of –32,768 to 32,767. A positive value indicates charge current and a negative value indicates discharge.

Any current value within the ***Deadband*** will be reported as 0 mA by the *Current* function.

Table 16. Current

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x0a	R	Current	Unsigned Integer	2	-32768	32767	-	mA

ESR (0x0b)

This read-word function returns an unsigned integer value of the Super Capacitor array total ESR in mΩ with a range of 0 to 65535mΩ

Table 17. ESR

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x0b	R	ESR	Unsigned Integer	2	0	65535	-	mΩ

RelativeStateofCharge (0x0d)

This read-word function returns an unsigned integer value of the predicted remaining super capacitor capacitance expressed as a percentage of *Capacitance* with a range of 0 to 100%, with fractions of % rounded up.

If the ***[RSOCL]*** bit in ***Operation Cfg*** is set then *RelativeStateofCharge* is held at 99% until primary charge termination occurs and only displays 100% upon entering primary charge termination.

If the ***[RSOCL]*** bit in***Operation Cfg*** is cleheld32.83 52.289 Td (in23.8 6 /F2 1024 82 Tz 0 0 0 rg 54Tj 15.4teofCharge)Tj /F2 10

thmely

ChargingCurrent (0x14)

This read-word function returns an unsigned integer value of the desired charging current, in mA, with a range of 0 to 65534.

Table 21. ChargingCurrent

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x14	R	ChargingCurrent	Unsigned Integer	2	0	65534	-	mA

ChargingVoltage (0x15)

This read-word function returns an unsigned integer value of the desired charging voltage, in mV, where the range is 0 to 65534.

Table 22. ChargingVoltage

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x15	R	ChargingVoltage	Unsigned Integer	2	0	65534	-	mV

CapacitorVoltage5..1 (0x3b..0x3f)

These read-word functions return an unsigned value of the calculated individual capacitor voltages, in mV, with a range of 0 to 65535. *CapacitorVoltage1* corresponds to the bottom most series capacitor element, while *CapacitorVoltage5* corresponds to the top most series capacitor element.

Table 23. CapacitorVoltage5..1

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x3b	R	CapacitorVoltage 5	Unsigned Integer	2	0	65535	-	mV
0x3c		CapacitorVoltage 4						
0x3d		CapacitorVoltage 3						
0x3e		CapacitorVoltage 2						
0x3f		CapacitorVoltage 1						

Extended SBS Commands

Also available via *ManufacturerAccess* in sealed mode are some of the extended SBS commands. The commands available are listed below. The result of these commands need to be read from *ManufacturerAccess* after a write to *ManufacturerAccess.*

FETCntrofTz 0 01j 23..21 0 Td (201 Td (FETControfTz 0 01j 23..21 0me)Tj 30.65 0 Td (of)Tj 14.54 0 Td (the)4(ManufacturerAccess.)T

Tz 0 0 0 rg 61 400.6 Td (SBS)Ti ET BT55

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
High Byte	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Low Byte	RSVD	RSVD	RSVD	RSVD	RSVD	CHG	RSVD	RSVD

LEGEND: All Values Read-Only

CHG — Charge (CHG) FET Control

0 = CHG FET is turned OFF.

1 = CHG FET is turned ON.

SafetyAlert (0x50)

This read-word function returns indications of pending safety issues, such as running safety timers, or fail counters that are nonzero but have not reached the reeha recounters

are_non5 /F2 7 Tf 100 Tz 0 0 0 rg 4 Td (ad (non5 /F2 7 Tf 100 Tz 0 0 0 rg 4 Td (ancti5 /F2 7 Tf 100 Tz 0 0 0 rg 4 S3i 21.8959.38 0 Td (not)

LEGEND: All Values Read-Only

CLBAD 1 = Excessive capacitor leakage fault

HWARN 1 = Health low warning

HLOW 1 = Health low indication

OTC 1 = Charge overtemperature fault

CIM 1 = Capacitor voltage Imbalance fault

OV 1 = Capacitor overvoltage fault

DFF 1 = Data Flash Fault permanent failure fault

AFE_C 1 = Permanent AFE Communications failure fault

WDF 1 = AFE Watchdog fault

OCC 1= Overcurrent during charge fault

OCD 1= AFE overcurrent during discharge fault

SCC 1= AFE short circuit during charge fault

SCD 1= AFE short circuit during discharge fault

OperationStatus (0x54)

This read-word function returns the current operation status

Table 27. OperationStatus

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x54	R	OperationStatus	hex	2	0x0000	0xf7f7	-	

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
High Byte	RSVD	DSG	SS	FC	LTE	RSVD	RSVD	CB
Low Byte	LDTO	LCTO	LPASS	CL	RSVD	CFET	RSVD	RSVD

DSG Discharging

0 = bq33100 is in charging mode

1 = bq33100 is in discharging mode, relaxation mode, or valid charge termination has occurred

SS 1 = Sealed security mode

FC 1 = Fully Charged

LTE 1 = Lifetime data and CHG FET operation enabled

CB 1 = Capacitor voltage balancing in progress

CL 1 = Capacitance learning in progress

LPASS 1 = Learning complete and successful

LCTO 1 = Learning charging phase time out

LDTO 1 = Learning discharging phase time out

SystemVoltage (0x5a)

This read-word function returns an unsigned integer value of the voltage at VCC (pin 24) in mV with a range of 0 to 20000 mV

Table 28. SystemVoltage

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x5a	R	SystemVoltage	Unsigned Integer	2	0	20000	-	mV

UnSealKey(0x60)

This read- or write-block command allows the user to change the Unseal key for the Sealed-to-Unsealed security-state transition. This function is only available when the bq33100 is in the Unsealed mode, indicated by a cleared *[SS]* flag.

The order of the bytes, when entered in *ManufacturerAccess*, is the reverse of what is written to or read from the part. For example, if the 1st and 2nd word of the UnSealKey block read returns 0x1234 and 0x5678, then in *ManufacturerAccess,* 0x3412 and 0x7856 should be entered to unseal the part.

Table 29. UnSealKey

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x60	R/W	UnSealKey	Hex	4	0x00000000	0xffffffff	-	

ManufacturerInfo(0x70)

This read/write block function returns the data stored in Manuf. Info where byte 0 is the MSB with a maximum length of 31 data + 1 length byte. When the bq33100 is in Unsealed mode, this block is read/write. When the bq33100 is in Sealed mode, this block is read only.

Table 30. ManufacturerInfo

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x70	R/W	ManufacturerInfo	String	31+1	-	-	-	

DATA FLASH

CAUTION

Care should be taken when mass programming the data flash space using previous versions of data flash memory map files (such as *.gg files) to make sure that all public locations are updated correctly.

Data Flash can only be updated if *Voltage* ≥ ***Flash Update OK Voltage***. Data flash reads and writes are verified according to the method detailed in the "Data Flash Fault Detection" section of this data sheet.

Accessing Data Flash

In different security modes, the data flash access conditions change. See "Security" and "ManufacturerAccess" sections for further details.

Data Flash Interface

The bq33100 data flash is organized into subclasses where each data flash variable is assigned an offset within its numbered subclass. For example: the OT Time location is defined as:

- Class = Safety
- SubClass = Temperature = 2
- Offset = 2

Note: Data Flash commands are NACKed if the bq33100 is in sealed mode (*[SS]* flag is set).

Each subclass can be addressed individually by using the *DataFlashSubClassID* (0x77) command and the data within each subclass is accessed by using the *DataFlashSubClassPage1..8* (0x78...0x7f) commands. Reading

and Writing subclass data are block operations which are each 32 Bytes long. Data can be written in shorter block sizes, however. The final block in one subclass can be shorter than 32 bytes so care must be taken not to write over the subclass boundary. None of the values written are bounded by the bq33100 and the values are not rejected by the bq33100. Writing an incorrect value may result in hardware failure due to firmware program interpretation of the invalid data. The data written is persistent, so a Power On Reset does resolve the fault.

Data Flash Summary

The following notation is used in the following table with regards to the Data Type column:

The **Alpha Character**

- H = Hexadecimal value
- I = Integer value
- S = String
- U = Unsigned Integer value

The **Numeric Value** following the Alpha Character is the length of the data in bytes, eg: ***OT Time*** Data Type = U1 = Unsigned Integer of 1 byte in length

Table 31. DATA FLASH VALUES

Class	Subclass ID	Subclass	Offset	Name	Data Type	Min Value	Max Value	Default Value	Units (EVSW Units)*
Safety	0	Voltage	0	OV Threshold	I2	0	1000	100	mV
Safety	0	Voltage	2	OV Recovery	I2	-500	1000	0	mV
Safety	0	Voltage	4	OV Time	U1	0	255	2	s
Safety	0	Voltage	5	CIM Voltage	I2	0	5000	550	mV
Safety	0	Voltage	7	CIM Time	U1	0	240	10	s
Safety	0	Voltage	8	CIM Recovery	I2	0	5000	500	mV
Safety	0	Voltage	10	Min CIM Check Voltage	U2	0	65535	1000	mV
Safety	1	Current	0	OC Chg	I2	0	5000	1000	mA
Safety	1	Current	2	OC Chg Time	U1	0	240	5	s
Safety	1	Current	3	OC Chg Recovery	I2	-1000	5000	900	mA
Safety	1	Current	5	CLBAD Current	I2	0	30000	15	mA
Safety	1	Current	7	CLBAD Time	U1	0	240	60	s
Safety	1	Current	8	CLBad Recovery	I2	0			

Table 31. DATA FLASH VALUES (continued)

Class	Subclass ID	Subclass	Offset	Name	Data Type	Min Value	Max Value	Default Value	Units (EVSW Units)*
Charge Control	35	Full Charge Cfg	0	Taper Current	I2	0	1000	3	mA
Charge Control	35	Full Charge Cfg	2	Taper Voltage	I2	0	1000	100	mV
Charge Control	35	Full Charge Cfg	4	Current Taper Window	U1	0	240	2	s
Charge Control	35	Full Charge Cfg	5	FC Set %	I1	-1	100	-1	%
Charge Control	35	Full Charge Cfg	6	FC Clear %	I1	-1	100	98	%
Charge Control	36	Capacitor Voltage Balancing Cfg	0	CB Threshold	I2	0	5000	1500	mV
Charge Control	36	Capacitor Voltage Balancing Cfg	2	CB Min	U1	0	255	5	mV
Charge Control	36	Capacitor Voltage Balancing Cfg	3	CB Restart	U1	0	255	10	mV
System Data	48	Data	0	Design Voltage	I2	0	25000	10500	mV
System Data	48	Data	2	Manuf Date	U2	0	65535	0	Day + Mo*32 + (Yr -1980)*256 (date)
System Data	48	Data	4	Ser. Num.	H2	0	0xffff	1	hex
System Data	48	Data	6	Design Capacitance	I2	0	65535	250	F
System Data	48	Data	8	Init 1st Capacitance	I2	0	65535	250	F
System Data	48	Data	10	Capacitance	I2	0	65535	250	F
System Data	48	Data	12	Design ESR	I2	0	65535	320	mΩ
System Data	48	Data	14	Initial ESR	I2	0	65535	320	mΩ
System Data	48	Data	16	ESR	I2	0	65535	320	mΩ
System Data	48	Data	18	Manuf Name	S12	x	x	Texas inst.	-
System Data	48	Data	30	Device Name	S8	x	x	bq33100	-
System Data	48	Data	38	Init safety Status	H2	0	0xffff	0	hex
System Data	56	Manufacturer Data	0	Pack Lot Code	H2	0	0xffff	0	-
System Data	56	Manufacturer Data	2	PCB Lot Code	H2	0	0xffff	0	-
System Data	56	Manufacturer Data	4	Firmware Version	H2	0	0xffff	0	-
System Data	56	Manufacturer Data	6	Hardware Version	H2	0	0xffff	0	-
System Data	58	Manufacturer Info	0	Manu. Info	S32	x	x	0123456789ABCDEF0123456789ABCDE	-
System Data	59	Lifetime Data	0	Lifetime Max Temp	I2	0	1400	0	0.1 degC (degC)
System Data	59	Lifetime Data	2	Lifetime Min Temp	I2	-600	1400	500	0.1 degC (degC)
System Data	59	Lifetime Data	4	Lifetime Max Capacitor Vol	I2	0	32767	0	mV
Configuration	64	Registers	0	Operation Cfg	H2	0	0xFFFF	0x0408	flg
Configuration	64	Registers	4	FET Action	H2	0	0xFFFF	0	flg
Configuration	64	Registers	8	Fault	H2	0	0xFFFF	0	flg
Configuration	65	AFE	1	AFE State_CTL	H1	0	ff	0	flg
Configuration	67	Power	0	Flash Update OK Voltage	I2	0	20000	4000	mV
Configuration	67	Power	2	Shutdown Voltage	I2	0	5500	4000	mV
Monitoring	86	System Requirement	0	Min Power	I2	0	16800	10	10mW
Monitoring	86	System Requirement	2	Required Time	I2	0	32767	60	s
Monitoring	86	System Requirement	4	Min Voltage	I2	0	10000	4000	mV

Table 31. DATA FLASH VALUES (continued)

Class	Subclass ID	Subclass	Offset	Name	Data Type	Min Value	Max Value	Default Value	Units (EVSW Units)*
Calibration	106	Temp Model	12	Ext Coef b2	I2	-32768	32767	-605	-
Calibration	106	Temp Model	14	Ext Coef b3	I2	-32768	32767	-2443	-
Calibration	106	Current	16	Ext Coef b4	I2	-32768	32767	4696	-
Calibration	106	Current	18	Ext rc0	I2	-32768	32767	11703	-
Calibration	106	Current	20	Ext adc0	I2	-32768	32767	11338	-
Calibration	106	Temp Model	22	Rpad	I2	-32768	32767	87	Ω
Calibration	106	Temp Model	24	Rint	I2	-32768	32767	17740	Ω
Calibration	106	Temp Model	26	Int Coef 1	I2	-32768	32767	0	-
Calibration	106	Temp Model	28	Int Coef 2	I2	-32768	32767	0	-
Calibration	106	Temp Model	30	Int Coef 3	I2	-32768	32767	-12263	-
Calibration	106	Temp Model	32	Int Coef 4	I2	-32768	32767	6106	-
Calibration	106	Temp Model	34	Int Min AD	I2	-32768	32767	0	cnt
Calibration	106	Temp Model	36	Int Max Temp	I2	-32768	32767	6106	0.1 degk (degk)
Calibration	107	Current	0	Filter	U1	0	255	239	num
Calibration	107	Current	1	Dead Band	U1	0	255	5	mA
Calibration	107	Current	2	CC Deadband	U1	0	255	10	294 nV

Specific Data Flash Programming Details

In this section the data flash values that are not detailed elsewhere in this data sheet are shown in detail and others are summarized for easy reference.

OC Dsg

The *OC Dsg* is programmed into the OCDV register of the integrated AFE device. The *OC Dsg* sets the overcurrent in discharging voltage threshold. Changes to this data flash value requires a firmware full reset or a power reset of the bq33100 to take effect.

Table 32. OC Dsg

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
1	Current	16	OC Dsg	Hex	1	0x00	0x0F	0x0F	-

Table 33. OCDV Register

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0
AFE OCDV Register	—	—	—	—	OCDV3	OCDV2	OCDV1	OCDV0

0000 is the bq33100 power on reset default.

OCDV3, OCDV2, OCDV1, OCDV0 — Sets the overcurrent voltage threshold in discharging of the integrated AFE.

0x0 - 0xf = sets the short circuit in discharging delay between 0ms - 915ms in 61ms steps.

[RSNS] = 0, 0x0 - 0xf sets the voltage threshold between 50mV and 200mV in 10mV steps.

[RSNS] = 1, 0x0 - 0xf sets the voltage threshold between 20mV and 100mV in 5mV steps.

OCDV (b7...b4) — Not used.

Cfg

Dsg

SC

39.

Register

Table

Subclass Name	Offset	Name	Format	Size in Bytes	Value Min	Value Max	Default Value	Unit
SCD								

4.4

Table

7 bit			4 bit			bit1	
SCDD3	SCDD2	SCDD1	SCDD0	-	SCDV2	SCDV1	SCDV0

with

Configuration Bits

0 =

(b2-b0)

SCDV

414

Table

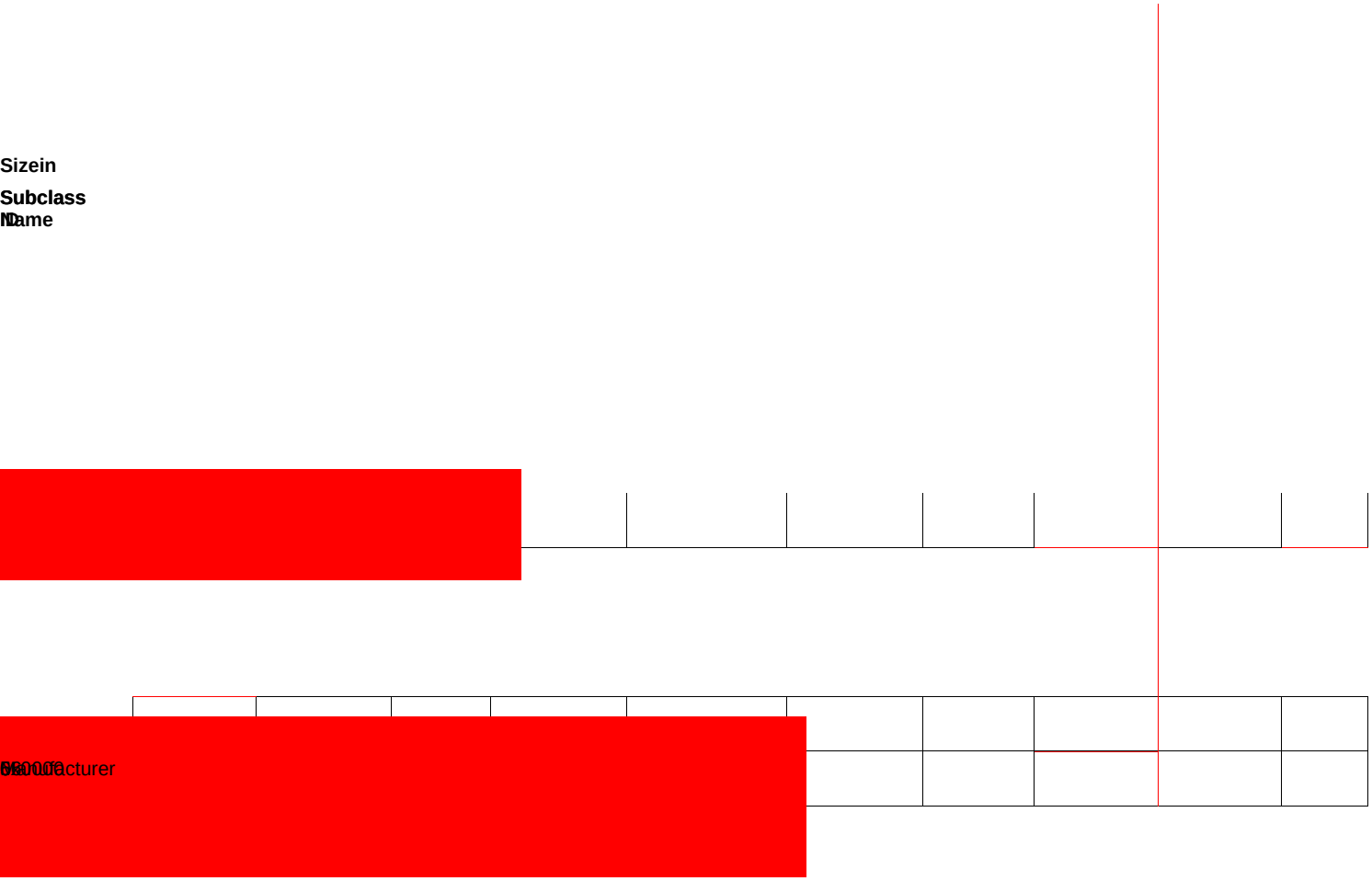
STATE_CTL[RSNS]

Setting	Threshold	Setting	Threshold
0x00	0.100	0x04	0.300
0x01	0.150	0x05	0.350
0x02	0.200	0x06	0.400
0x03	0.250	0x07	0.450

STATE_CTL[RSNS]

Setting	Threshold	Setting	Threshold
0x00	0.050	0x04	0.150
0x01	0.075	0x05	0.175
0x02	0.100	0x06	0.200
0x03	0.125	0x07	0.225

Setting	Delay	Setting	Delay	Setting	Delay	Setting	Delay
0x00	0 us	0x04	244 us	0x08	488 us	0x0c	732 us
0x01	61 us	0x05	305 us	0x09	549 us	0x0d	793 us
0x02	112 us	0x06	366 us	0x0a	610 us	0x0e	854 us
0x03	183 us	0x07	427 us	0x0b	671 us	0x0f	915 us



Sizein

Subclass

Name

Manufacturer

Offset

Subclass

Learning Frequency

Learning Frequency is the amount of time elapsed between automatic learning cycles.

Table 67. Learning Frequency

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
86	Capacitance Estimation	18	Learning Frequency	Unsigned Integer	1	0	255	2	week

Dsg Current Threshold

The bq33100 enters discharge mode from charge mode if *Current* < (-) ***Dsg Current Threshold***.

Table 68. Dsg Current Threshold

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
81	Current Thresholds	0	Dsg Current Threshold	Integer	2	0	2000	10	mA

Chg Current Threshold

The bq33100 enters charge mode from discharge mode if *Current* > ***Chg Current Threshold.***

Table 69. Chg Current Threshold

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
81	Current Thresholds	2	Chg Current Threshold	Integer	2	0	2000	0	mA

Quit Current

The bq33100 enters relaxation mode from charge mode if *Current* goes below ***Quit Current*** for 60 seconds. The bq33100 enters relaxation mode from discharge mode if *Current* goes above (-)***Quit Current*** for 60 seconds.

Table 70. Quit Current

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
81	Current Thresholds	4	Quit Current	Integer	2	0	1000	0	mA

MEASUREMENT SYSTEM AND CALIBRATION CONFIGURATION

Calibration

The bq33100 does not require calibration but can be calibrated for improved measurement accuracy.

Coulomb Counter Deadband

The bq33100 does not accumulate charge or discharge for monitoring when the current input is below the ***Deadband*** threshold which should be set sufficiently high to prevent false signal detection with no charge or discharge flowing through the sense resistor.

Auto Calibration

The bq33100 provides an auto-calibration feature to cancel the voltage offset error across SRP and SRN for maximum charge measurement accuracy. The bq33100 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s and *Temperature* is within bounds of 5°C and 45°C.

Current Gain

Current Gain sets the mA current scale factor for the coulomb counter. Use calibration routines to set this value.

SRP CaLink(s):s

Table 71. Current

Cap4 K-factor

This register value stores the ADC voltage translation factor for Capacitor 4, which is connected between the VC4 and VC5 pins. By default, this value is not used and the factory calibration are in effect. This value overrides the factory calibration when the K-factor Override Flag is set to 0x9669 by the software calibration process.

Table 76. Cap4 K-factor

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
104	Data	14	Cap4 K-factor	Integer	2	0	32767	20500	

Cap5 K-factor

This register value stores the

CC Offset

This register value stores the coulomb counter offset compensation. It is set during CC Offset calibration, or by automatic calibration of the bq33100 before the gauge enters shutdown. It is not recommended to manually change this value.

Table 81. CC Offset

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
104	Data	20	CC Offset	Integer	2	-32768	32767	-7744	(mV)

Board Offset

This register value stores the compensation for the PCB dependant coulomb counter offset. It is recommended to use characterization data of the actual PCB to set this value.

Unit

Table 82. Board Offset

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
104	Data	22	Board Offset	Integer	2	-32767	32767	0	uV

Int Temp Offset

This register value stores the internal temperature sensor offset compensation. Use calibration routines to set this value

Table 83. Int Temp Offset

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
104	Data	24	Int Temp Offset	Integer	1	-128	127	0	0.1 degC

Ext1 Temp Offset

This register value stores the temperature sensor offset compensation for the external temperature sensor 1 connected at the TS1 pin of the bq33100. Use calibration routines to set this value

Table 84. Ext1 Temp Offset

MaxValue

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
104	Data	25	Ext1 Temp Offset	Integer	1	-128	127	0	0.1 degC

CC Current

This Tz 0 0 0 /F1 11 Tf Tf 100 Tz /F2 8 Tf rg 424.9 258 Td (127)Tj ET BT /F2 8 Tf 100 Tz 00

Name

Voltage Signal

This value sets the voltage used for calibration when in calibration mode.

Table 86. Voltage Signal

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	2	Voltage Signal	Integer	2	0	32767	12600	mV

Temp Signal

This value sets the temperature used for the temperature calibration in calibration mode.

Table 87. Temp Signal

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	4	Temp Signal	Integer	2	0	32767	298	0.1 degK

CC Offset Time

This value sets the time used for the CC Offset calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 250. Numbers less than 250 will cause a CC Offset calibration error. Numbers greater than 250 will be rounded down to the nearest multiple of 250.

Table 88. CC Offset Time

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	6	CC Offset Time	Unsigned Integer	2	0	65535	250	s (ms)

ADC Offset Time

This constant defines the time for the ADC Offset calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 32. Numbers less than 32 will cause an ADC offset calibration error. Numbers greater than 32 will be rounded down to the nearest multiple of 32.

Table 89. ADC Offset Time

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	8	ADC Offset Time	Unsigned Integer	2	0	65535	32	ms

Current Gain Time

This constant defines the time for the Current Gain calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 250. Numbers less than 250 will cause a Current gain calibration error. Numbers greater than 250 will be rounded down to the nearest multiple of 250.

Table 90. Current Gain Time

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	10	Current Gain Time	Unsigned Integer	2	0	65535	250	ms

Voltage Time

This constant defines the time for the voltage calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 1984. Numbers less than 1984 will cause a voltage calibration error. Numbers greater than 1984 will be rounded down to the nearest multiple of 1984.

Table 91. Voltage Time

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	12	Voltage Time	Unsigned Integer	2	0	65535	1888	ms

Temperature Time

This constant defines the time for the temperature calibration in calibration mode. More time means more accuracy. The legitimate values for this constant are integer multiples of 32. Numbers less than 32 will cause a temperature calibration error. Numbers greater than 32 will be rounded down to the nearest multiple of 32.

Table 92. Temperature Time

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	14	Temperature Time	Unsigned Integer	2	0	65535	32	ms

Cal Mode Timeout

The bq33100 will exit calibration mode automatically after a ***Cal Mode Timeout*** period.

Table 93. Cal Mode Timeout

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
105	Config	17	Cal Mode	Unsigned	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Rpad

This value characterize the pad resistance of the bq33100. Do not modify without consulting TI.

Table 95. Rpad

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
106	Temp Model	22	Rpad	Integer	2	-32768	32767	87	Ohm

Rint

This value characterize the internal resistance of the bq3100. Do not modify without consulting TI.

Table 96. Rint

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
106	Temp Model	24	Rint	Integer	2	-32768	32767	17740	Ohm

Int Coef 1..4, Int Min AD, Int Max Temp

These values characterize the internal thermistor of the bq33100. Do not modify these values without consulting TI.

Table 97. Int Coef 1..4, Int Min AD, Int Max Temp

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
106	Temp Model	26	Int Coef 1	Integer	2	-32768	32767	0	s
		28	Int Coef 2					0	
		30	Int Coef 3					-12263	
		32	Int Coef 4					6106	
		34	Int Min AD					0	
		36	Int Max Temp					6106	0.1 degK

Filter

Filter defines the filter constant used in the AverageCurrent calculation:

AverageCurrent new = a x *AverageCurrent* old + (1 - a) x Current

with:

a = <***Filter***> / 256; the time constant = 1 sec/ln(1/a) (default 14.5 sec)

Table 98. Filter

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
107	Current	0	Filter	Unsigned Integer	1	0	255	239	

Deadband

Any current within ±***DeadBand*** will be reported as 0 mA by the *Current* function

Table 99. Deadband

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
107	Current	1	Deadband	Unsigned Integer	1	0	255	0	mA

CC Deadband

This constant defines the Deadband voltage for the measured voltage between the SR1 and SR2 pins used for capacitance accumulation in units of 294 nV. Any voltages within ±C***C Deadband*** do not contribute to capacitance accumulation.

Table 100. CC Deadband

Subclass ID	Subclass Name	Offset	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
107	Current	2	Deadband	Unsigned Integer	1	0	255	10	294 nV

APPLICATION INFORMATION

APPLICATION SCHEMATIC

Application Reference Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ33100PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	33100	Samples
BQ33100PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85		

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