2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: bq3050

FEATURES

- **Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection**
- **Advanced Compensated End-of-Discharge Voltage (CEDV) Gauging**
- **High Side N-CH Protection FET Drive**
- **Integrated Pre-Charge FET**
- **Integrated Cell Balancing**
- **Low Power Modes**
  - **Low Power: < 180 μA**
  - **Sleep < 76 μA**
- **Full Array of Programmable Protection Features**
  - **Voltage**
  - **Current**
  - **Temperature**
- **Sophisticated Charge Algorithms**
  - **JEITA**
  - **Enhanced Charging**
  - **Adaptive Charging**
- **Supports Two-Wire SMBus v1.1 Interface**
- **SHA-1 Authentication**
- **Compact Package: 38-Lead TSSOP**

APPLICATIONS

- **Notebook/Netbook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq3050 device is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq3050 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

The bq3050 provides software-based 1st-level and 2nd-level safety protection for overvoltage, undervoltage, overtemperature, and overcharge conditions, as well as hardware-based protection for overcurrent in discharge and short circuit in charge and discharge conditions.

SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs beyond any doubt.

The compact 38-lead TSSOP package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING INFORMATION[(1)]	
					TUBE[(2)]	TAPE AND REEL[(3)]
–40°C to 85°C	bq3050	TSSOP-38	DBT	bq3050	bq3050DBT	bq3050DBTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at www.ti.com.
(2) A single tube quantity is 50 units.
(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

THERMAL METRIC[(1)]		bq3050	UNITS
		TSSOP	
		38 PINS	
$\theta_{JA, High K}$	Junction-to-ambient thermal resistance[(2)]	64.2	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance [(3)]	16.5	
θ_{JB}	Junction-to-board thermal resistance [(4)]	31.2	
ψ_{JT}	Junction-to-top characterization parameter [(5)]	0.3	
ψ_{JB}	Junction-to-board characterization parameter [(6)]	26.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance [(7)]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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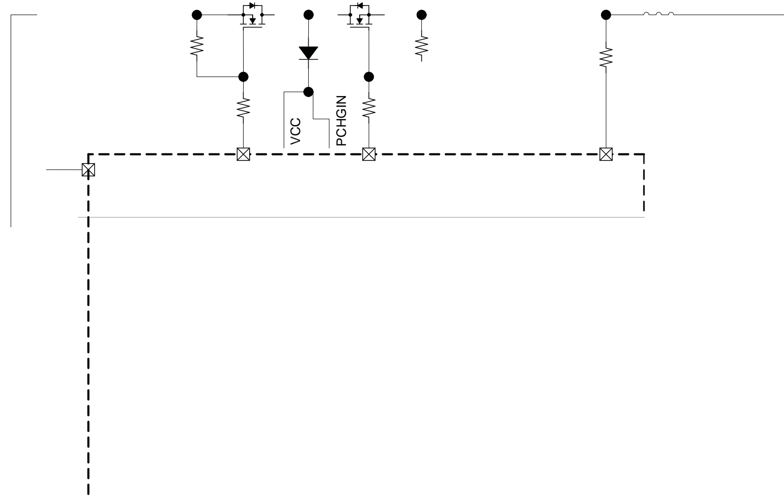
VCC
PCHGIN

Pin-Out Diagram

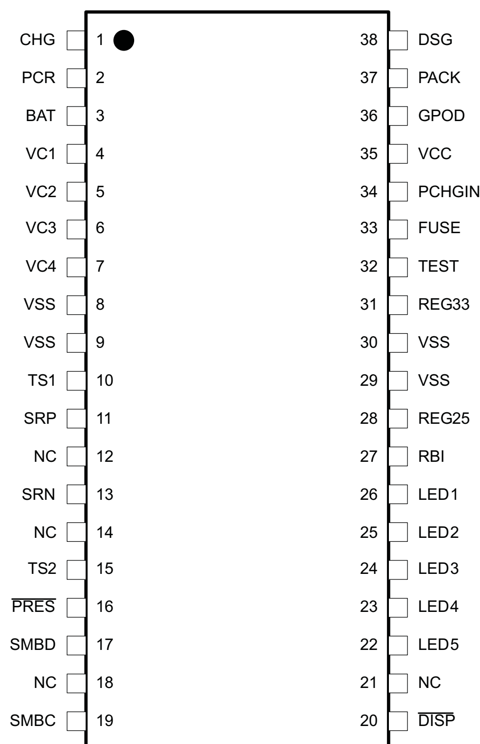

Figure 2. bq3050 Pin-Out Diagram

PIN FUNCTIONS

PIN NAME	PIN NUMBER	TYPE(1)	DESCRIPTION
	bq3050-DBT		
CHG	1	O	Charge N-FET gate drive
PCR	2	O	Internal Pre-Charge FET output
BAT	3	P	Alternate power source
VC1	4	I	Sense input for positive voltage of top most cell in stack and cell balancing input for top most cell in stack
VC2	5	I	Sense input for positive voltage of third lowest cell in stack and cell balancing input for third lowest cell in stack
VC3	6	I	Sense input for positive voltage of second lowest cell in stack and cell balancing input for second lowest cell in stack
VC4	7	I	Sense input for positive voltage of lowest cell in stack and cell balancing input for lowest cell in stack
VSS	8	P	Device ground
VSS	9	P	Device ground
TS1	10	AI	Temperature sensor 1 thermistor input
SRP	11	AI	Differential Coulomb Counter input
NC	12	—	

otherwiseeE5441.21 r0e 0 noted)eE54/F 06q305T /20 3.6 re 0(1)eE54 7l10 0T 8q3050soldering.eE5439.747 te 0 10eE5411.3q te 0 s).eE5411.29q te 0 TeE54/F 06q3054.85 -1.6 re 0SOLDEReE54 7l10 0 08q30501)eE54e7.88q te 0 Stress

ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	C_L = 4700 pF R_G = 5.1 kΩ VCC < 8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V V_{CHG}: V_{PACK} to V_{PACK} + 4 V		800	1400	µs
		C_L = 4700 pF R_G = 5.1 kΩ VCC > 8.4 V_{DSG}: V_{BAT} to V_{BAT} + 4 V V_{CHG}: V_{PACK} to V_{PACK} + 4 V		200	500	µs
t_f	Fall time	C_L = 4700 pF R_G = 5.1 kΩ V_{DSG}: V_{BAT} + $V_{O(FETONDSG)}$ to V_{BAT} + 1 V V_{CHG}: V_{PACK} + $V_{O(FETONCHG)}$ to V_{PACK} + 1 V		80	200	µs

ELECTRICAL CHARACTERISTICS: INTERNAL PRE-CHARGE LIMITING

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{PCHGMAX}$	Maximum Pre-charge current	3-cell and 4-cell configuration [illegible]			[illegible]	[illegible]
		$V_{DS(PRECHG)}$ = [illegible]				

TYP pF (TA)T 240.2 435 Td (3-cell2 8 Tf186.6 Td (1Td (DS(PRECHG))Tj /F3 8 Tf 40.3 1.6 30f 4206.6 Td (n2 8 Tf 100 Tz 0 0 0 rg)Tj /F3 9 BT /F2 8 17/F1 8 Tf 240.2 598.8 Td (R)Tj /F2 6 Tf 5.7 -1.6 Td (G)Tj /F2 8 Tf 7 1.6 Td (=

ELECTRICAL CHARACTERISTICS: LED5, LED4, LED3, LED2, LED1

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	μA
I_{OL}	Low-level output current	VOL = 0.4 V, 3 mA setting	2.5	3.5	4.5	mA
		VOL = 0.4 V, 4 mA setting	3.0	4.5	6.0	mA
		VOL = 0.4 V, 5 mA setting	3.5	5.5	7.5	mA
I_{LEDx}	Current matching between LEDx			0.1		mA

ELECTRICAL CHARACTERISTICS: COULOMB COUNTER

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	SRP – SRN	–0.20		0.25	V
	Conversion time	Single conversion		250		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution	Single conversion, signed	15			Bits
	Offset error	Post calibrated		10		μV
	Offset error drift			0.3	0.5	μV/°C
	Full-scale error		–0.8%	0.2%	0.8%	
	Full-scale error drift				150	PPM/°C
	Effective input resistance		2.5			mΩ

ELECTRICAL CHARACTERISTICS: VC1, VC2, VC3, VC4

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		VC4 – VC3, VC3				

ELECTRICAL CHARACTERISTICS: TS1, TS2 (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	TS1 – VSS, TS2 – VSS	–0.20		0.8 × V_{REG25}	V
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

ELECTRICAL CHARACTERISTICS: Internal Temperature Sensor

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage		–1.9	–2.0	–2.1	mV/°C
	Conversion Time			16		ms
	Resolution (no missing codes)		16			Bits
	Effective resolution		11	12		Bits

ELECTRICAL CHARACTERISTICS: Internal Thermal Shutdown

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX1}	Maximum PCHG temperature		110		150	°C
T_{MAX2}	Maximum REG33 temperature		125		175	
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C
$t_{PROTECT}$	Protection time			5		µs

ELECTRICAL CHARACTERISTICS: High Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU Clock			4.194		MHz
$f_{(EIO)}$	Frequency error[1][2]	T_A = –20°C to 70°C	–2%	±0.25%	2%	
		T_A = –40°C to 85°C	–3%	±0.25%	3%	
$t_{(SXO)}$	Start-up time[3]	T_A = –25°C to 85°C		3	6	ms

(1) The frequency error is measured from 4.194 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{REG25} = 2.5V, T_A = 25°C.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3% when the device is already powered.

ELECTRICAL CHARACTERISTICS: Low Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error[1][2]	T_A = –20°C to 70°C	–1.5%	±0.25%	1.5%	
		T_A = –40°C to 85°C	–2.5%	±0.25%	2.5%	
$t_{(LSXO)}$	Start-up time[3]	T_A = –25°C to 85°C			100	µs

(1) The frequency drift is included and measured from the trimmed frequency at VCC = 2.5V, T_A = 25°C.
(2) The frequency error is measured from 32.768 kHz.
(3) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.

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T_A = 25ºC and VCC = 14.4 V. Min/Max values stated where T_A = –40ºC to 85ºC and VCC = 3.8 V

ELECTRICAL CHARACTERISTICS: SCD1 Current Protection (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD2 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

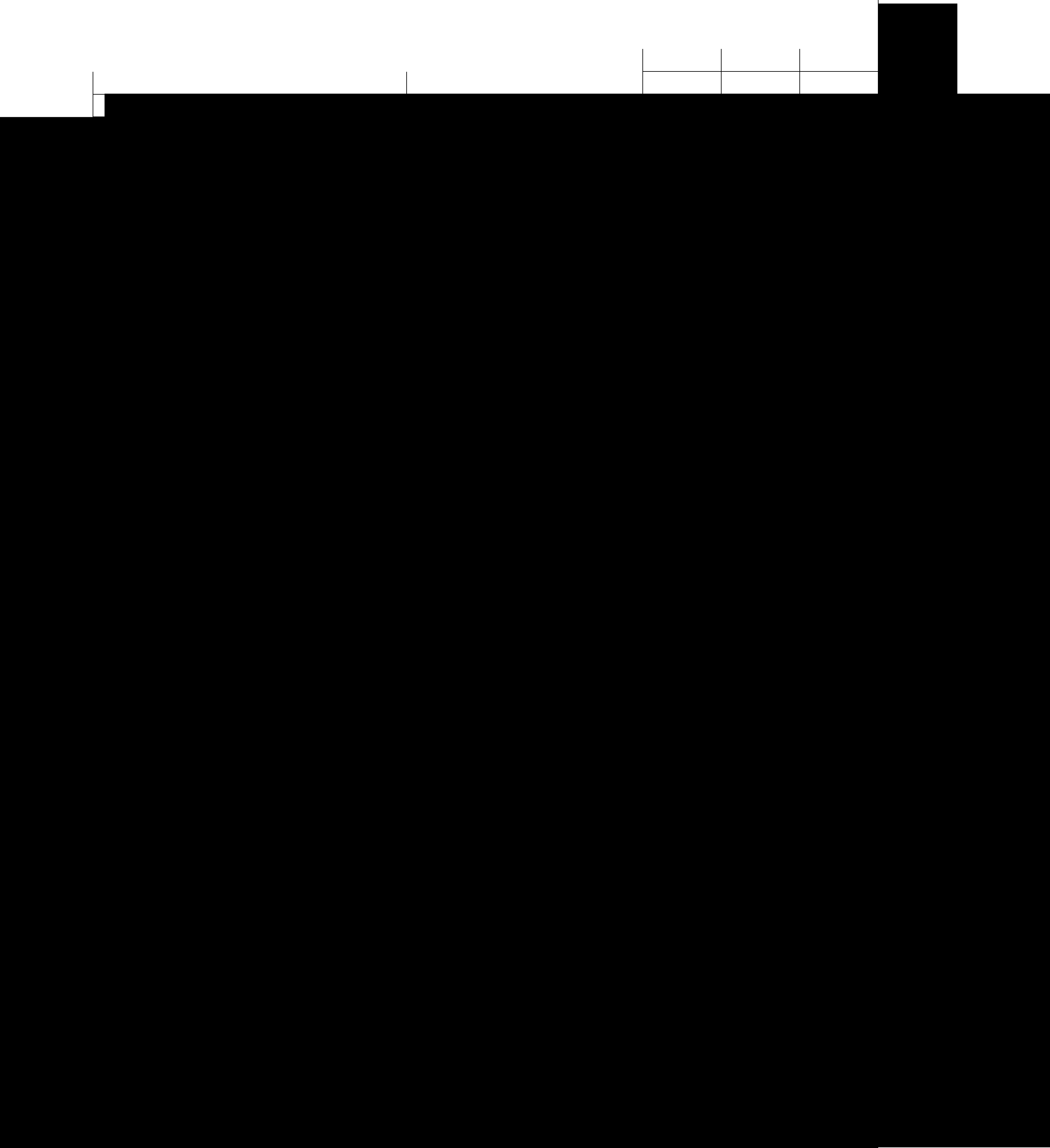
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC2)}$	SCD2 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD2T)}$	SCD2 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD2 offset		–10		10	mV
$V_{(Scale_Err)}$	SCD2 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		458	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		915	µs
$t_{(SCD2D_STEP)}$	SCD2D Step options	AFE.STATE_CNTL[SCDDx2] = 0		30.5		µs
		AFE.STATE_CNTL[SCDDx2] = 1		61		µs
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCC Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0	–100	[illegible]	[illegible]	[illegible]
		RSNS = 1	–50		–225	mV
$\Delta V_{(SCCDT)}$	SCC detection threshold voltage program step	RSNS = 0		–50		mV
		RSNS = 1		–25		mV
$V_{(OFFSET)}$	SCC offset		–10		10	mV
$V_{(Scale_Err)}$	SCC scale error		–10		10	%
$t_{(SCCD)}$	Short Circuit in Charge Delay		0		915	ms
$t_{(SCCD_STEP)}$	SCCD Step options			61		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

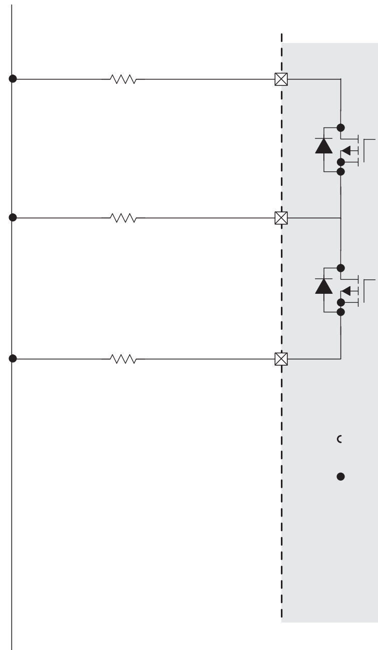
ELECTRICAL CHARACTERISTICS: SBS [illegible]



FEATURE SET

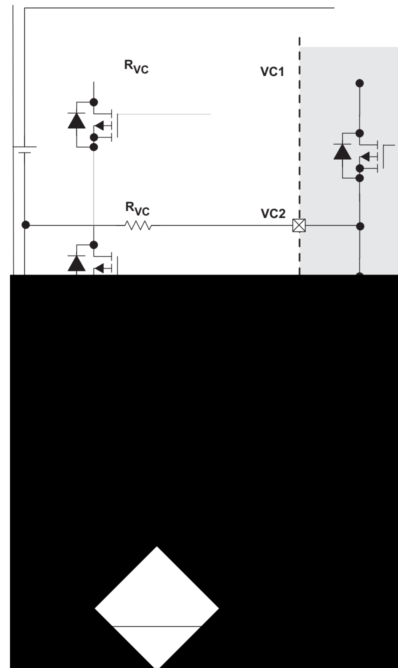
Primary (1st Level) Safety Features

The bq3050 supports a wide range of battery and system protection features that can easily be configured.



External Cell Balancing

When external cell balancing is configured, the cell balance current is defined by R_B. Only one cell at a time can be balanced.



BATTERY PARAMETER MEASUREMENTS

Charge and Discharge

APPLICATION SCHEMATIC

REVISION HISTORY

Changes from Original (January 2011) to Revision A **Page**

- Changed Block Diagram 3
- Changed TS2 pin number 4
- Changed TEST pin resistor value 5
- Changed schematic 20

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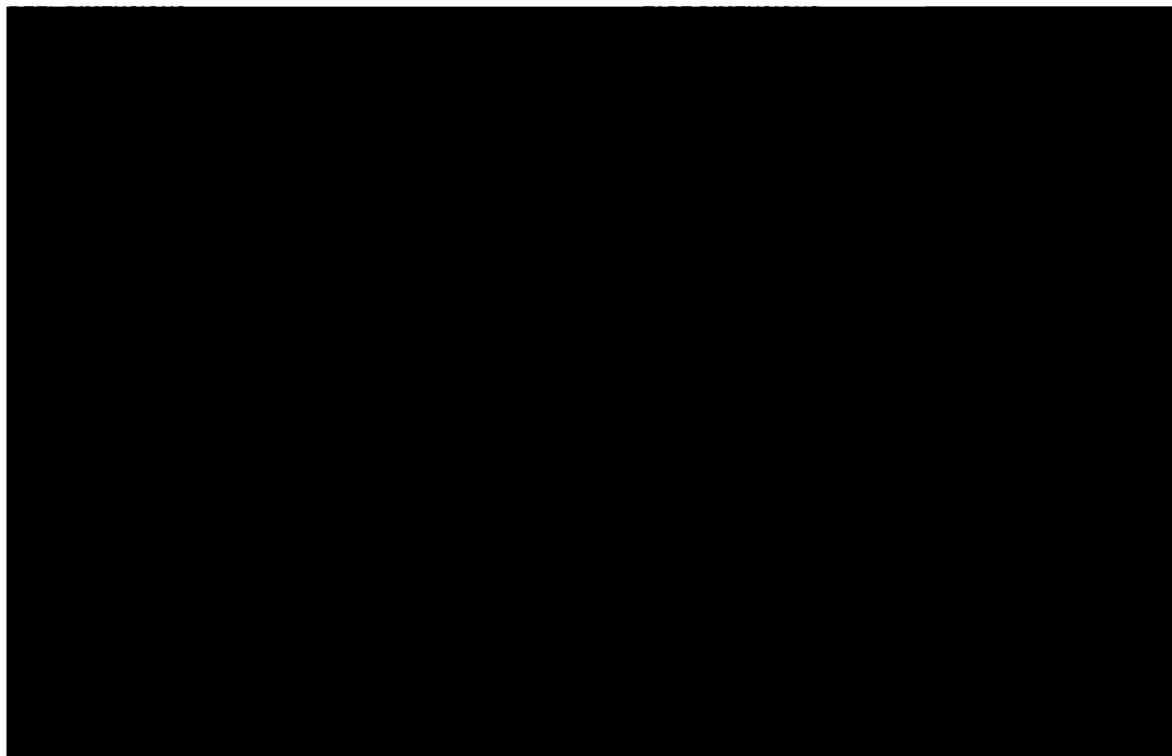
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ3050DBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ3050DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND:

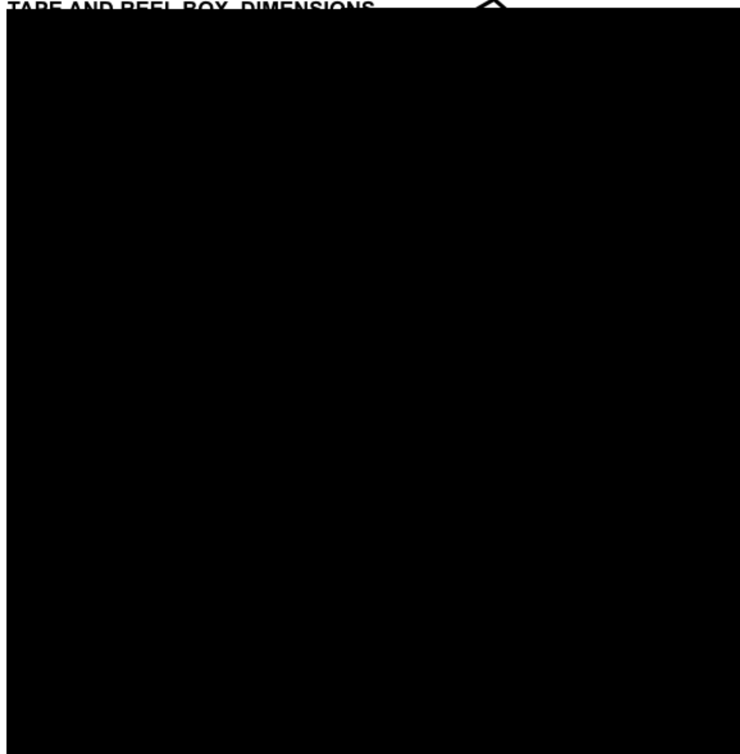
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ3050DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

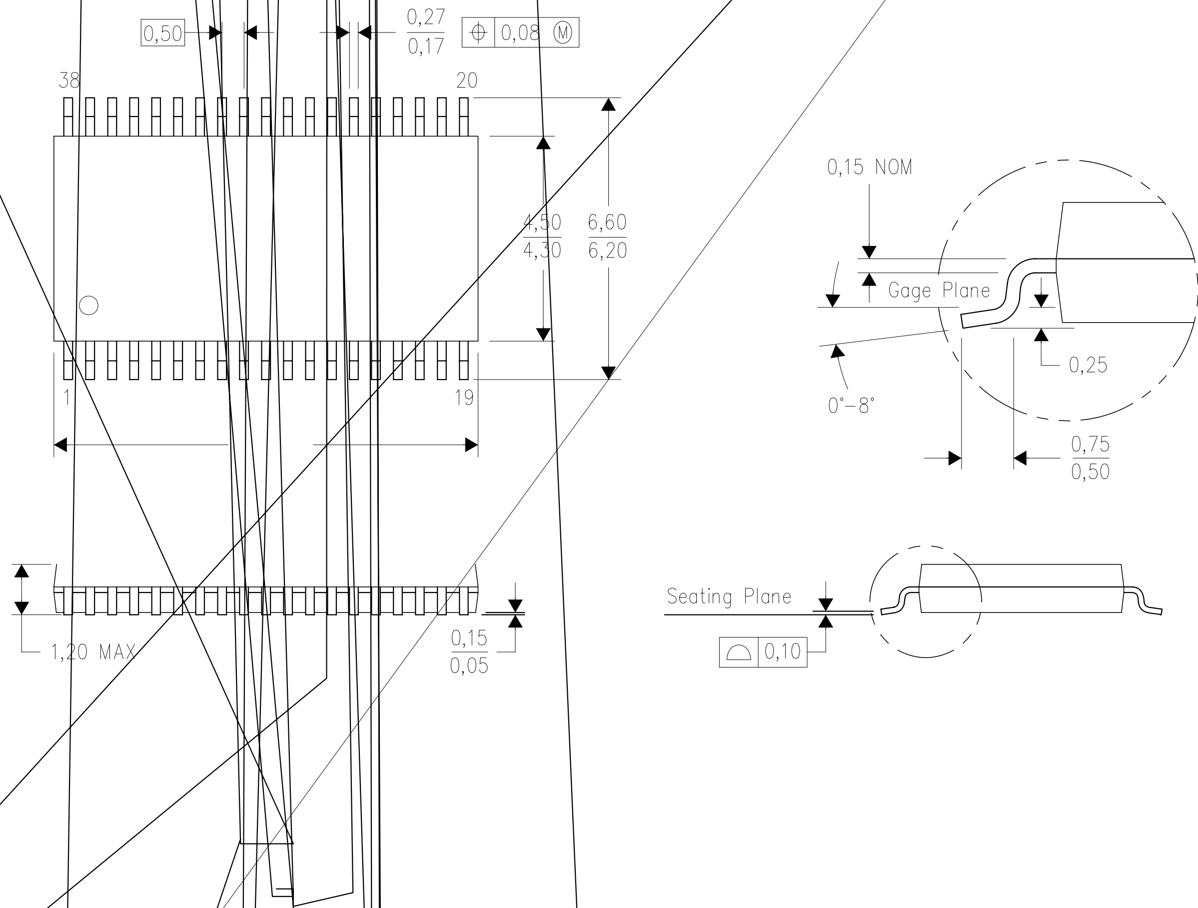
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ3050DBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0

DBT (R-PDSO-G38) PLASTIC SMALL OUTLINE



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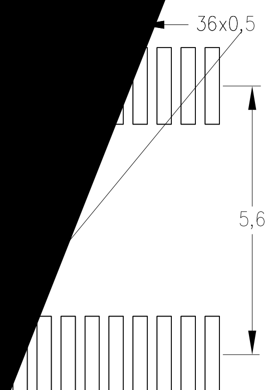
NOTES:
A. All linear dimensions are in r... cr ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.



NOTES: dimensions are in

B. This drawing is subject to change without notice.

D. res with trans

contact their board assembl

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No TI components are o1.74s0 Tdsfa57