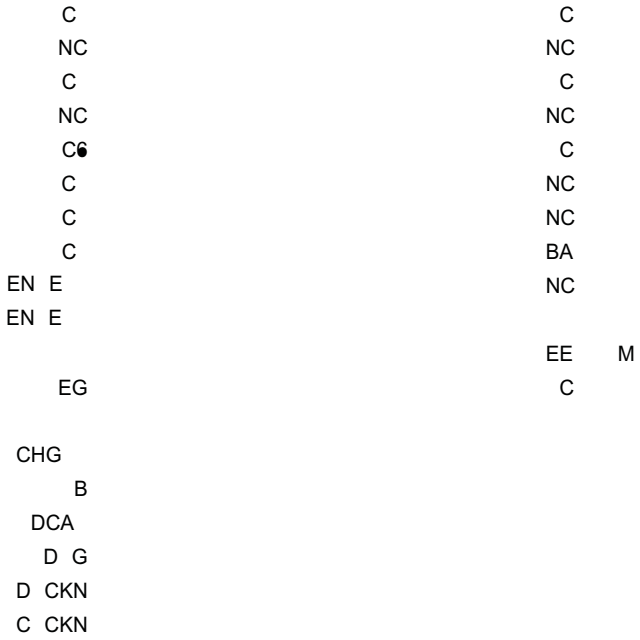
PIN DETAILS

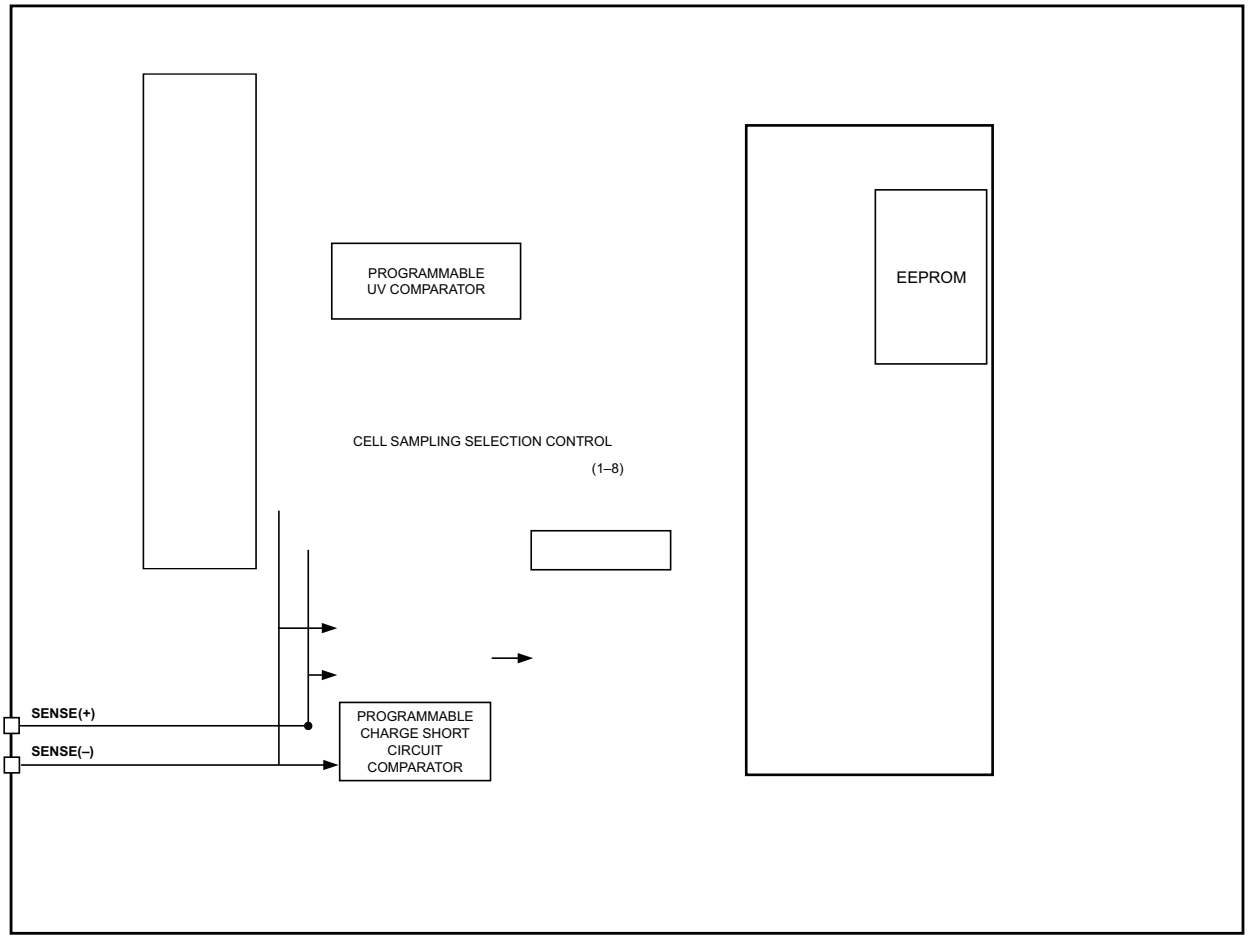
PIN FUNCTIONS (38-Pin Package)

PIN		DESCRIPTION
NAME	NO.	
BAT	31	Power supply voltage, tied to highest cell(+)
CCAP	20	Energy storage capacitor for charge FET drive
CHG	21	Charge FET (n-channel) gate drive
CHGST	14	Charger-status input, used to detect charger connection/wakeup
CPCKN	19	Pack – charger negative terminal (charger return)
DCAP	16	Energy storage capacitor for discharge FET drive
DPCKN	18	Pack – discharge negative terminal (load return)
DSG	17	Discharge FET (n-channel) gate drive
EEPROM	28	EEPROM programming voltage input. Connect to VSS for normal operation.
GND	23, 24, 25	Logic ground (not for power return or analog reference). Tie to VSS.
NC	2, 4, 30, 32, 33, 35, 37	No connect (DO NOT CONNECT) externally. Failure to leave NC pins open can cause faulty operation.
SCLK	27	Serial-communication clock input used for EEPROM programming
SDATA	26	Serial-communication data input/output used for EEPROM programming (open-drain)
SENSE(+)	10	Current-sense input
SENSE(–)	9	Current-sense input
TS	13	Temperature sensing input
VC1	34	Sense-voltage input terminal for most-positive cell
VC2	36	Sense-voltage input terminal for second-most-positive cell
VC3	38	Sense-voltage input terminal for third-most-positive cell
VC4	1	Sense-voltage input terminal for fourth-most-positive cell
VC5	3	Sense-voltage input terminal for fifth-most-positive cell
VC6	5	Sense-voltage input terminal for sixth-most-positive cell
VC7	6	Sense-voltage input terminal for seventh-most-positive cell
VC8	7	Sense-voltage input terminal for eighthmost-positive (most-negative) cell
VC9	8	Most-negative cell(–) terminal (BAT–)
VREG	12	Integrated 3.3-V regulator output
VSS1	29	Analog ground (substrate reference)
VSS2	11	Analog ground (substrate reference)
VTSB	15	Thermistor bias supply (sourced from VREG)
ZEDE	22	*Zero Delay* test mode pin. Enables serial communications interface and minimizes protection delay times when connected to logic high. Connect to VSS for normal operation. A strong connection is recommended.

PIN DIAGRAM – bq77908A – 38-Pin SSOP DBT PACKAGE



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PACKAGING
bq77908ADBT	TSSOP	50-piece tube
bq77908ADBTR	TSSOP	2000-piece reel

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE/UNIT
DC supply-voltage range, V_{MAX}	BAT	–0.3 to (5 × N) V, N = number of cells implemented in pack
Input voltage range, V_{IN}	DPCKN	–0.3 V to 50 V
	CPCKN	(BAT – 50) V to (BAT + 0.9) V
	Cell-to-cell differential, VCx to VC(x+1), x = 1 to 8	–0.3 V to 9 V
	SENSE(+)	–3 V to 3 V
	SENSE(–)	–0.3 V to 50 V
	SCLK, SDATA, ZEDE (2)	–0.3 V to 7 V
	TS, CHGST(3)(4)	–0.3 V to BAT V
	EEPROM	–0.3 V to 15 V
	Cell input VCx, x = 1–8	(9 – x) × 5 V
	Cell input VC9	–3 V to 3 V
Output voltage range, V_O	CHG referenced to CPCKN	– 0.3 V to 15 V
	DSG referenced to VSS	–0.3 V to 15 V
	VTSB	–0.3 V to 5 V
Current for cell balancing, I_{CB}		70 mA
Regulator current, I_{REG}		45 mA
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device and expose the system to potential safety risks, resulting from the damage to the IC. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability or cause damage to the device.
(2) All signal/logic pins which may be connected to the pack external terminals are internally clamped to a maximum voltage of 5 V. If the external source driving these signals exceeds the clamp threshold, series resistance from the pin to the pack terminal is required to avoid overstress on the clamping circuit.
(3) CHGST and TS pins are tolerant of applied overvoltage as noted to allow for charger single-fault tolerance. Normal operating range is typically 3.3 V or less at this pin; thus, high voltage seen here may correspond to a fault condition.
(4) Although no damage results when CHGST = VSS – 0.3 V, for proper operation at power up, CHGST must be ≥ VSS – 0.25 V.

THERMAL INFORMATION

THERMAL METRIC(1)		bq77908A DBT 38 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, non-LDO(2)	71.7	°C/W
θ_{JA2}	Junction-to-ambient thermal resistance, LDO(2) (3)	115.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(4)	18.5	°C/W
θ_{JB}	Junction-to-board thermal resistance(5)	33.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter, non-LDO(6)	1	°C/W
ψ_{JT2}	Junction-to-top characterization parameter, LDO(6) (3)	38.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) These metrics should be used only for calculating junction temperature due to power dissipation resulting from the I_{OUT} load on VREG. Junction temperature calculations for all other sources of power dissipation should use the standard values θ_{JA} and ψ_{JT}.
(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(6) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

THERMAL INFORMATION (continued)

THERMAL METRIC[1]		bq77908A DBT 38 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter[7]	33.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[8]	N/A	°C/W

(7) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
Supply voltage		BAT[1]	5.6[2]		35[3]	V
V_I	Input voltage range	Cell differential, VCx to VC(x + 1), (x = 1 to 8)	1.4		4.375	V
		Cell input VCx, x = 1 – 8			(9 – x) × 4.375 V	
		Cell input VC9	–1		1	
V_{IH}	Logic-level input, high	SCLK, SDATA, EEPROM, ZEDE	0.8 × V_{REG}			V
V_{IL}	Logic-level input, low				0.2 × V_{REG}	V
VSENSE(+)	Voltage applied at SENSE(±) pins		VSS – 1		VSS + 1	V
VSENSE(–)			–0.2		BAT	V
R_{VCX}	Recommended VCx nominal input resistance		50	100	1000	Ω
I_{REG}	Regulator current				10	mA
I_{CB}	Cell balancing current				50	mA
C_{VCX}	Recommended VCx nominal input filter capacitance				1	µF
R_{CPCKN}, R_{DPCKN}	Recommended isolation-pin input resistance			100		Ω
R_{LDRM_DET}	Pulldown for load-removal detection			50		kΩ
C_{VREG}	External 3.3-V REG capacitor		1			µF
	EEPROM number of writes				3	times
T_{OPR}	Operating temperature	Meeting all specification limits	–25		85	°C
T_{FUNC}	Functional temperature	Operational but may be out of spec limits, no damage to part	–40		100	°C
C_{CCAP}, C_{DCAP}	External capacitance on CCAP and DCAP pins[4]		0.1	1		µF
R_P	Serial communication interface pullup resistance[5]	SCLK, SDATA		2.2		kΩ

(1) The voltage rate of change at the BAT pin should be limited to a maximum of 1 V per µs in order to prevent unwanted device shutdown.
(2) Minimum voltage assumes 4-cell connection at 1.4 V/cell.
(3) Maximum voltage assumes 8-cell connection at 4.375 V/cell.
(4) C_{CCAP} and C_{DCAP} act as charge reservoirs for the CHG and DSG pins when driving large protection FETs. Minimum value is required for stability, independent of the CHG and DSG loading.
(5) Pullups for configuration of device during pack manufacturing. SCLK and SDATA should be pulled high or low in application.

NOTE

Refer to the Open-Cell Detection overview in the *Application Information* section for a description of RVCX and CVCX sizing.

ELECTRICAL CHARACTERISTICS

Vcell(n) = 1.4 to 4.375 for all cells, T_A = –25°C to 85ºC, BAT = 5.6 to 35 V; Typical values stated where T_A = 25°C and BAT = 28.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC}	Normal-mode average supply current	CHG, DSG = on (no dc load), VREG = on, I_{REG} = 0 mA, BAT = 28.8 V			50	75	µA
$I_{SHUTDOWN\_2}$ (1)	Shutdown mode, LDO off	Vcell < Vuv, VREG = off (EEPROM set), CPCKN = 0.3 V			5	17	µA
		Vcell < Vuv, VREG = off (EEPROM set), CPCKN = 0.5 V			20	60	
INTERNAL POWER CONTROL (STARTUP, SHUTDOWN, GATE DRIVE UNDERVOLTAGE)							
$V_{STARTUP}$	Minimum voltage for initial power up (2)	Measured at BAT pin				7	V
V_{POR} (3)	LDO POR voltage – voltage on LDO that initiates a POR	I_{LDO} = 2 mA		2.7		3.2	V
V_{GATE_UV}	FET gate shutdown threshold (voltage falling)	Measured at CCAP/DCAP pins		4.5	4.9	5.3	V
$V_{GATE\_UV\_H}$	FET gate shutdown hysteresis voltage	Measured at CCAP/DCAP pins		0.45		0.7	V
FET DRIVE (4)							
$V_{(FETON)}$	Gate drive voltage at DSG and CHG pins for FET ON (enabled) conditions	BAT voltage = 35 V (gate-drive circuit in regulation mode), no dc load		11	12	14	V
		BAT voltage = 10 V (gate-drive circuit in dropout mode), no dc load		9			
		BAT voltage = 6.4 V (gate-drive circuit in dropout mode), no dc load		>V_{GATE_UV}			
$V_{(FETOFF)}$	Gate drive voltage at DSG and CHG pins for FET OFF (disabled) conditions	$V_{O(FETOFFDSG)} = V_{(DSG)} – V_{GND}$				0.2	V
		$V_{O(FETOFFCHG)} = V_{(VHG)} – V_{pack–}$				0.2	
t_r	Rise time, measured at IC pin (CHG or DSG)	C_L = 50 nF, BAT = 35 V	V_{DSG}: 10% to 90%		90	140	µs
			V_{CHG}: 10% to 90%		90	140	
		C_L = 50 nF, BAT = 6.4 V	V_{DSG}: 10% to 90%		90	140	
			V_{CHG}: 10% to 90%		90	140	
t_f	Fall time, measured at IC pin (CHG or DSG)	C_L = 50 nF, BAT = 35 V	V_{DSG} : 90% to 10%		10	20	µs
			V_{CHG}: 90% to 10%		20	40	
		C_L = 50 nF, BAT = 6.4 V	V_{DSG} : 90% to 10%		50	100	
			V_{CHG}: 90% to 10%		50	100	
VREG, INTEGRATED 3.3-V LDO							
V_{REG}	Output-voltage regulation under all line, load, temperature conditions	I_{OUT} = 10 mA (maximum dc load) (5)		3.1	3.3	3.55	V
		I_{OUT} = 0.2 mA		3.1	3.3	3.55	V
I_{SC}	Short-circuit current limit	VREG = 0 V, forced external short (thermally protected) (6)		20		45	mA

(1) For predictable shutdown current, the voltage at CPCKN with respect20

/Artifact<

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

ELECTRICAL CHARACTERISTICS (continued)

Vcell(n) = 1.4 to 4.375 for all cells, T_A = –25°C to 85ºC, BAT = 5.6 to 35 V; Typical values stated where T_A = 25°C and BAT = 28.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGER DETECTION(11)						
V_{CHG_DET1}	Voltage at CHGST pin, referenced to VSS, to determine charger present (charger insertion detected when voltage at CHGST pin > V_{CHG_DET1})	5.6 V < BAT < 35 V	0.3	0.5	0.7	V
LOAD REMOVAL DETECTION						
V_{OPEN_LOAD}	Voltage at DPCKN, referenced to VSS, with DSG FET *disabled* to detect load removal (load removal detected when voltage at DPCKN < V_{OPEN_LOAD})	5.6 V < BAT < 35 V	1.5	2	2.5	V
R_{DSG_GND}	Internal resistance between DPCKN and VSS	5.6 V < BAT < 35 V	1000	1500	3000	kΩ
EEPROM LIFETIME						
T_{DR}	Data retention	5.6 V < BAT < 35 V	10			years

(11) Alternate charger detection options are available using the CPCKN pin. Contact TI for additional configuration versions.

SERIAL COMMUNICATION INTERFACE (for Configuration Only)

BAT = 5.6 V to 35 V, T_A = –25°C to 85°C

PARAMETER		MIN	MAX	UNIT
t_r	SCLK, SDATA rise time		1000	ns
t_f	SCLK, SDATA fall time		300	ns
$t_{w(H)}$	SCLK pulse duration, high	8		µs
$t_{w(L)}$	SCLK pulse duration, low	10		µs
$t_{su(STA)}$	Setup time for START condition	9.4		µs
$t_{h(STA)}$	START condition hold time after which first clock pulse is generated	8		µs
$t_{su(DAT)}$	Data setup time	250		ns
$t_{h(DAT)}$	Data hold time	0		µs
$t_{su(STOP)}$	Setup time for STOP condition	8		µs
$t_{su(BUF)}$	Time the bus must be free before new transmission can start	9.4		µs
t_V	Clock low to data out valid		900	ns
$t_{h(CH)}$	Data out hold time after clock low	0		ns
f_{SCL}	Clock frequency	0	50	kHz

GENERAL OPERATIONAL OVERVIEW

POWER MODES

WARNING

The Texas Instruments bq77908/bq77908A-series and bq77910/bq77910A-series integrated circuits help system designers greatly enhance the safety of their Li-Ion and Li-Polymer battery packs when these ICs are integrated effectively and in accordance with the instructions detailed in this document by technically qualified personnel familiar with battery pack application safety. Failure to follow the instructions in this document could result in risk of property damage, personal injury, or death due to the hazards associated with a battery pack overheating, fire, rupture, or explosion.

The bq77908A has the following power modes: active and shutdown (LDO disabled). The following table outlines the operational functions in the different power modes.

POWER MODE	MODE DESCRIPTION
Active	The IC is operating with internal LDO enabled and battery monitoring functions available and operating. The active power mode includes *normal* operation, i.e., all cell voltages, load current, and temperature are within range, and DSG and CHG FETs are enabled. The active power mode also includes any fault detection/protection states which do not require the IC to drop to a low-power state.
Shutdown – LDO	Under certain fault conditions (see Table 2), the bq77908A fault CHG

Table 1. Detection Voltage, Detection Delay Time Summary

PARAMETER		RANGE (EEPROM Selected)	MIN	MAX	STEP
Overvoltage	Cell voltage		2.8 V	4.375 V	25 mV
	Delay		0.5 s	2.25 s	0.25 s
	Hysteresis		0 mV	300 mV	25 mV or 50 mV
Undervoltage	Cell voltage		1.4 V	2.9 V	100 mV
	Delay		500 ms	32 s	Binary spacing
	Hysteresis		400 mV	1600 mV	400 mV
Discharge overcurrent	SENSE(–) pin voltage with respect to SENSE(+)	Low	25 mV	100 mV	5 mV
		High	125 mV	500 mV	25 mV
	Delay		20 ms	300 ms	20 ms
			400 ms	2000 ms	100 ms
Discharge short circuit	SENSE(–) pin voltage with respect to SENSE(+)	Low	40 mV	190 mV	10 mV
		High	200 mV	950 mV	50 mV
	Delay	Fast	60 µs	960 µs	60 µs
		Slow	50 ms	1500 ms	50 ms or 100 ms
Charge short circuit	SENSE(–) pin voltage with respect to SENSE(+)	Low	–10 mV	–85 mV	5 mV
		High	–50 mV	–425 mV	25 mV
	Delay		60 µs	960 µs	60 µs

Cell Overvoltage Detection and Recovery

The CHG FET is turned off if any one of the cell voltages remains higher than V_{OV} for a period greater than t_{OV}. As a result, the cells are protected from an overcharge condition. After an overvoltage event occurs, the all cells must relax to less than ($V_{OV} – V_{HYST}$) to allow recovery.

The V_{OV}, t_{OV}, and V_{HYST} values can be set via the EEPROM bits OVT, OVD, and OVH.

Cell Undervoltage Detection and Recovery

When any one of the cell voltages falls below V_{UV}, for a period of t_{UV}, the bq77908A enters the undervoltage protection state. The DSG FET is turned off, and depending on configuration, the device could enter the SHUTDOWN mode. Both V_{UV} and t_{UV} can be configured via EEPROM bits UVT and UVD.

The recovery (fault release) is controlled by the EEPROM configuration bit UV_REC.

If UV_REC = 0, the DSG FET is re-enabled when **all** the cell voltages increase back above the V_{UV} threshold level plus the hysteresis value; there is no time-delay part of the recovery. In this case, when UV_REC = 0 and under high load currents, the Vcell voltages could recover to >UV + hyst very quickly, re-enabling the FETs and allowing the high load current to persist. Care should be taken when using this UV_REC = 0 mode, as the power MOSFETs could oscillate rapidly.

WARNING

To minimize application safety risk, care should be taken to properly set overcurrent and cell undervoltage trip thresholds, because it is possible that a fully charged pack with a continuous high discharge load can oscillate in and out of the undervoltage condition. This may result in overheating of the cells or protection MOSFETs due to the potentially high-duty-cycle operation.

If UV_REC = 1, the DSG FET is re-enabled when **all** the cell voltages increase back above the V_{UV} threshold level plus the hysteresis value **AND** the load is removed.

Current is interrupted by opening the FETs, and at this point the cell voltages may quickly recover above the UV + hyst levels if the battery pack is not completely depleted. However, the external load may remain attached. When the external load is removed, the IC detects load removal and reconnects the DSG FET.

If UV_REC_DLY = 1 and any cell remains below the VUV threshold level plus the hysteresis for longer than 8 seconds, the device enters SHUTDOWN mode. If UV_REC_DLY = 0, the device does **not** enter the SHUTDOWN mode from the cell undervoltage fault condition.

The LDO is turned off during the SHUTDOWN mode. Insertion into a charger is required to recover from the SHUTDOWN mode.

Charger detection methods are discussed in later sections, such as *Application Information*.

Overcurrent in Discharge (OCD) Detection

The OCD detection feature senses an overload current by measuring the voltage across the sense resistor. When an overload condition is detected, both of the power FETS are disabled to prevent damage to the cells and FET components. Criteria for fault recovery depend on the state of the SOR (EEPROM bit). Overcurrent trip level (V_{OCD}) and blanking time delay (t_{OCD}) are programmable via EEPROM bits OCDT and OCDD to match individual application requirements.

Short Circuit in Discharge (SCD) Detection

The SCD detection function senses severe discharge current by measuring the voltage across the sense resistor. When a short circuit is detected, both of the power FETs are disabled to prevent damage to the cells and FET components. Criteria for fault recovery depend on the state of the of the SOR (EEPROM bit). Short-circuit trip level (V_{SCD}) and blanking time delay (t_{SCD}) are programmable via EEPROM bits SCDT and SCDD to match individual application requirements.

Load Removal Detection/OCD and SCD Fault Recovery

The part includes an internal high-impedance connection between the DPCKN and VSS pins of approximately 1.5 MΩ. An external load (for example power tool motor winding), if still connected to the pack terminals, would present a very low impedance relative to the high internal pulldown resistance.

NOTE

If the external load presents additional capacitance, then an external pulldown may be required between the DPCKN and VSS pins. This extra pulldown does not increase battery load current when the external load is removed.

If the DSG power FET is disabled after an overload or short-circuit event, the voltage at the DPCKN is approximately equivalent to the BAT voltage potential while an external load (e.g., power tool motor) is present at the pack terminals. When the external load is removed, the high-value internal resistance pulls down the DPCKN potential to the internal VSS level. An internal comparator monitors the DPCKN terminal voltage during the protection state. When the DPCKN voltage falls to < V_{OPEN_LOAD} (approximately 2 V), the load removal is detected. Fault recovery from an OCD or SCD event depends on the state of the SOR EEPROM bit.

If SOR = 0, the FETs are re-enabled only after the external load removal is detected.

If SOR = 1, the FETs are re-enabled after the load is removed **and** a charger insertion is detected.

(Details of charger presence detection methods are discussed in later sections.)

Short Circuit in Charge (SCC) Detection

The SCC detection function senses severe charge current by measuring the voltage across the sense resistor. In this case, the voltage is negative (opposite polarity of OCD and SCD detection). When a short circuit is detected, both of the power FETS are disabled to prevent damage to the cells and FET components. Short-circuit trip level (V_{SCD}) and blanking time delay (t_{SCD}) are programmable via EEPROM bits SCCT and SCCD to match individual application requirements.

NOTE

The current sensing element must be located along a common charge and discharge path in order to protect against both charge and discharge current faults. This is particularly important to note for parallel FET configurations or configurations that combine the FET with the sense element.

Short Circuit in Charge Recovery

An SCC fault is cleared after charger removal is detected. (See later sections for details of charger insertion and removal detection methods).

FIXED HARDWARE FAULT-PROTECTION FUNCTIONS

The bq77908A provides a number of fixed protection settings for hardware faults as listed:

- Open-cell connection
- Pack voltage *Brownout* condition – power FET protection
- Charger-enable temperature range
- Open thermistor connection
- Shorted thermistor connection
- Overtemperature protection

Open-Cell Connection

A mechanical or assembly fault in the pack can cause a high-impedance or broken connection between the IC cell sense pins and the actual cells. During operation, the bq77908A periodically checks the validity of the individual cell voltage reading by applying a micropower pulsed load across each cell. If the connection between the pin and the cell is opened, the apparent cell voltage will collapse and a fault (permanent failure) condition is detected. The open-cell detection reading is taken at a time interval of $t_{OPEN\_CELL\_CHECK}$, as specified in the parametric tables. Recommended external filter-capacitor maximum value is also listed in the *Recommended Operating Conditions*. Because an open-cell fault may be considered as a permanent failure, the fault detection logic must detect two consecutive open-cell conditions prior to activating the protection condition for an open-cell fault. Due to the nature of open-cell fault conditions, other *apparent* faults may be observed during an open-cell condition.

Summary of open-cell detection-logic operation:

- For an N-cell battery pack, the bq77908A always protects (by opening the FETs) in some manner within the 2 × N × $t_{OPEN\_CELL\_CHECK}$ time frame (sampling interval is $t_{OPEN\_CELL\_CHECK}$, and two successive open-cell faults are required to avoid nuisance tripping).
- Because an open-cell connection results in a floating VCx input, a UV or an OV fault may be detected before the open-cell fault due to their shorter fault filter times. Furthermore, the OV or UV condition may not be stable and the fault may recover during the open-cell check interval (i.e., the FETs may toggle). In all cases the open-cell fault is detected within the open-cell fault filter time and the FETs are shut off until the recovery conditions are satisfied. .
- The LDO shuts down following the detection of an open-cell fault, provided that a charger is not detected. When the pack is awakened following this, the open-cell fault is initially cleared (FETs closed) and must be re-evaluated over the filter time before the fault is again registered. Charger detection inhibits LDO shutdown; however, once the charger is disconnected, the LDO then shuts down, provided that the recovery conditions have not yet been satisfied.

Additional Fault Protection Functions

The brownout protection functionality is discussed in the *IC Internal Power Control* section of this document. Thermistor fault detection, charger/thermistor interface and control are discussed in the *Application Information* section.

IC INTERNAL POWER CONTROL

Power-On Reset/UVLO

On initial application of power to the BAT pin, the IC internal power supply rail begins to ramp up. The IC contains an internal undervoltage lockout (UVLO)/power-on reset (POR) circuit that prevents operation until the BAT voltage is sufficient to ensure predictable start-up and operation. All power for the IC internal circuitry is derived from the BAT pin. The UVLO/POR start-up threshold is specified in the parametric table as $V_{STARTUP}$. Once the BAT voltage has exceeded this level, the internal LDO regulator and control circuitry are enabled and continue to operate even if BAT falls below enable

BAT Voltage Peak Detection/Transient Suppression

The use of an external diode and holdup capacitor allows the IC to provide controlled operation during brownout conditions. However, when the battery pack is at a high level, a different issue must be considered.

During normal operation of power equipment, load transients may induce high-voltage pulses on the PACK(+) rail that exceed the steady-state dc voltage output of the battery pack. In some cases, these transient voltages can exceed the battery rail by several volts. The voltage at the BAT pin may be *held up* to these higher voltages for a longer duration because the diode prevents the capacitor from discharging back into the cell stack after the transient pulses decay. When the dc level of the battery pack voltage is near 35 Vdc, high-current load disconnection may cause transients that would exceed the absolute maximum ratings of the device.

The BAT pin incorporates an internal Zener clamp that dissipates any transient voltage at the BAT pin that exceeds 50 V. This internal clamp has very limited energy absorption ability. Therefore, additional external circuitry is required for transient suppression, depending on the application environment. A Zener or equivalent rated at <5 Ω and >3 W is recommended.

BAT Voltage Rate of Change

In addition to providing the holdup function, the filter components at the BAT pin serve to limit the maximum voltage rate of change. The voltage rate of change at the BAT pin should be limited to a maximum of 1 V per µs in order to prevent unwanted device shutdown.

Figure 2. Example 5-Cell, Series FET Configuration Schematic Using bq77908A

Waveforms illustrative of load transients during high pack voltage conditions are shown here.

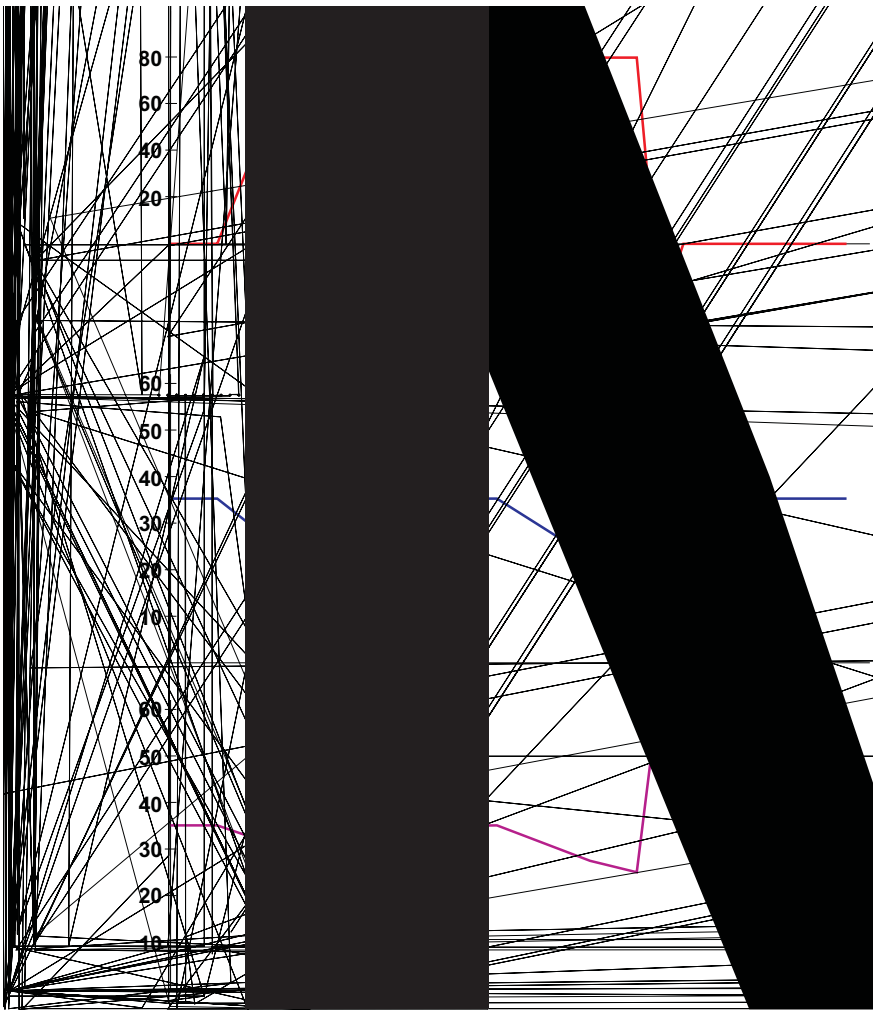


Figure 3. High-Voltage Load-Transient Waveforms

FET Gate Drive Control

As noted in the previous section, the BAT voltage at the IC pin is held up slightly longer than the external PACK(+) voltage using the external diode/capacitor to feed the BAT rail. Thus, if the BAT pin voltage at the IC sags, the external voltage sag will have exceeded the holdup time, and the IC is no longer able to operate for an extended period of time. At this point, the DSG and CHG gate drive outputs are actively driven low. The FET driver stages use two additional external capacitors (connected at the CCAP and DCAP pins) to maintain a local power reservoir dedicated to the gate drive circuitry, as the system (BAT) voltage may be collapsing during the time that the FETs are being turned off. The FETs are turned off when the voltage at the CCAP and/or DCAP pins falls below V_{GATE_UV}.

By turning off the FETs quickly, the system avoids the condition of insufficient gate drive due to low battery voltage.

NOTE

If the FET gate drive is not high enough, the power components may not be in their linear operating region, and could overheat due to resistive losses at high load currents.

In the case of a system undervoltage condition, both FETs are disabled within 500 µs maximum; in all cases the FET fall time is less than fall time specified in the *Electrical Characteristics* section (FET Drive). During initial power up, once the UVLO threshold has been reached and the IC powers up fully, the rise time of the FET gate drive signal is also < 200 µs. This assumes a nominal gate capacitance of 50 nF as specified in the *Electrical Characteristics* tables.

NOTE

Selection of power FETs should consider the resistive losses that may occur during the undefined voltage range during power up from a complete collapse of battery voltage and holdup capacitance.

INITIAL POWER UP

Cell Connection

The IC design allows connection of the cells in any order. For EEPROM programming, only the VSS and BAT terminals must be connected to allow the device to communicate using the serial communication interface.

For normal pack assembly, the recommended connection procedure is to start with the VSS connection, followed by the (+) terminal of the lowest (most negative) cell, and continuing up the stack to the top (most positive) cell. The BAT voltage shown in Start-Up Timing assumes this connection sequence is used.

Power-Up Sequence and Continuous Fault-Detection Logic

The bq77908A goes through a fixed set of safety checks on each power-up sequence. The same checks are performed on each recovery cycle from the SHUTDOWN state (after a charger is detected).

For each power up, the following tests are made. If any of the conditions indicate a fault, the IC goes into the appropriate protection state. External connections may be required for fault recovery (such as load removal or insertion into charger). *The device goes through a power-up sequence in < 100 ms, assuming no faults exist.*

After the release of the internal digital reset, the logic begins a power-up safety check. Two internal signals, designated PWRUP_SAFE_CHK and PWRUP_DONE, control the sequence.

When PWRUP_DONE is low, the following conditions are forced:

1. CHG and DSG external pins/gate drive signals are low.
2. UV_HYST = HI (internal logic signal – use hysteresis level above UV threshold to clear fault)
3. OV_HYST = HI (internal logic signal – use hysteresis level below OV threshold to clear fault)

After 50 ms of time has elapsed, a pulse of PWRUP_SAFE_CHK performs a check of each of the following circuits (with all time delays disabled):

1. UV comparator
2. OV comparator
3. OCD comparator
4. SCD comparator

If a fault condition was found for any of the above protection circuits, an internal fault status bit is set. For another 50 ms, the circuit has a chance to recover if the sample was corrupted. At the end of 100 ms, the PWRUP_DONE signal is released. If no faults exist, the CHG, DSG, UV_HYST, and OV_HYST return to their normal-mode state.

Several of the protection circuits were not included in the power-up sequence (SCC, OT, TS, TO, OC). These faults are checked after the power-up sequence is completed.

NOTE

This check is only performed on a power up from LDO-off or a digital reset occurring (i.e., POR state).

Start-Up Timing

The following timing diagrams refer to signals at the device pins as well as to the following INTERNAL logic signals.

- BAT_UVLO = HI when the BAT pin is below the POR threshold (undervoltage lockout).
- WAKEUP = HI whenever a charger is attached.
- UV_STATUS = HI when n UV condition has been detected.
- OV_STATUS = HI when an OV condition has been detected.

Figure 4. Initial Power Up With Single-Cell UV Fault

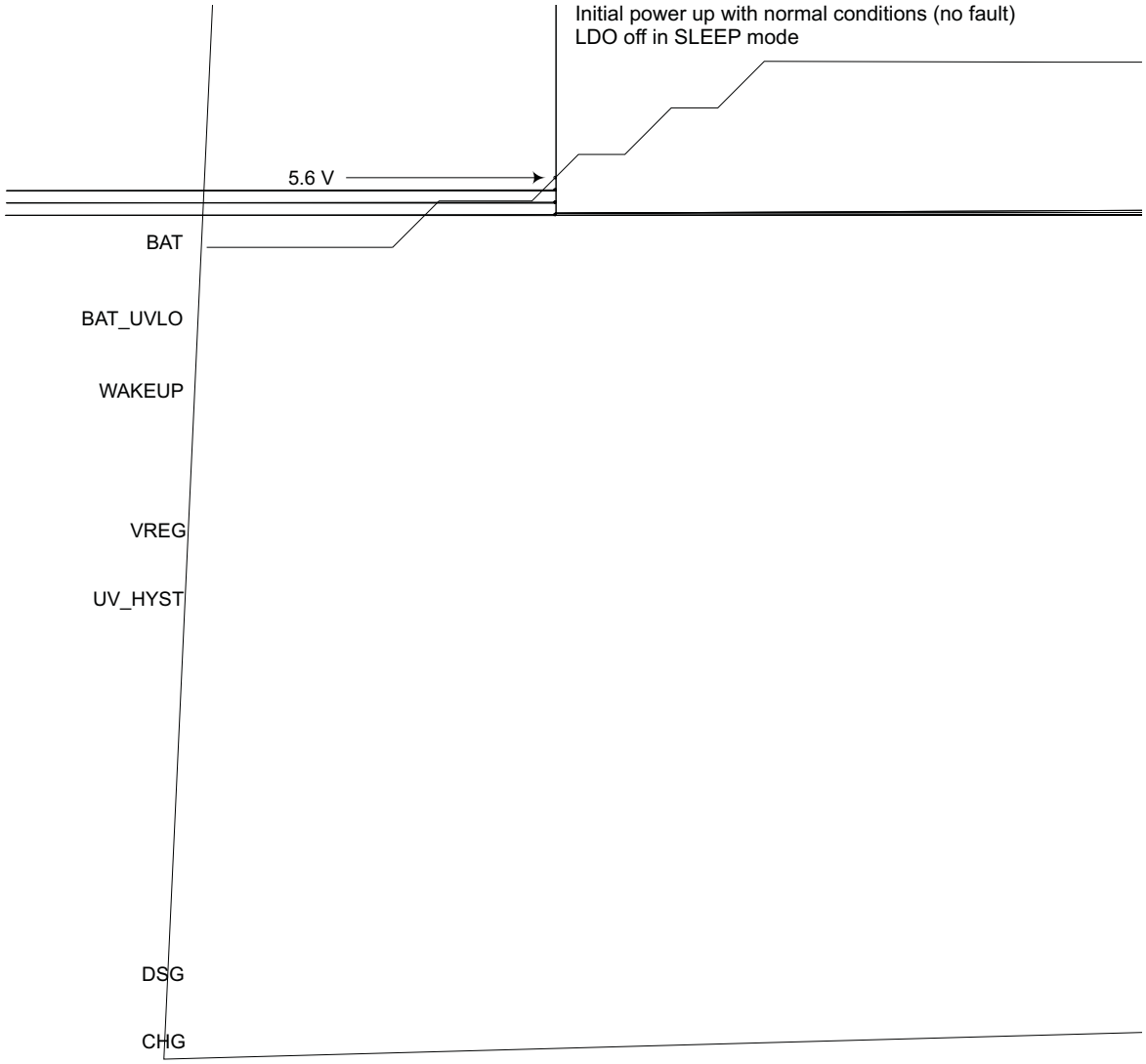


Figure 5. Initial Power Up With Normal Conditions (No Fault)

Table 2. Fault Detection, Action, and Recovery Condition Summary

Fault Condition	Fault Detection Parameter	Filter Time	Action Taken			EEPROM Config (if Applicable)	Recovery Conditions
			FET		MODE		
			CHG	DSG			
CELL OVERVOLTAGE	Any cell > V_{OV}	t_{OV}	OFF	ON	OV FAULT protection state	OV_TS_CTRL = 0	All cells < OV-hyst
					EXT CHGR DISABLE (TS pin→low)	OV_TS_CTRL = 1	
CELL UNDER-VOLTAGE	Any cell < V_{UV}	t_{UV}	OFF(1)(2)	OFF	UV FAULT protection state(3)	UV_REC bit = 0	1) Both FETS ON when all cells >UV + hyst (4) 2) CHG FET enabled immediately if charger detected
			OFF(5)(2)	OFF	UV FAULT protection state(3)	UV_REC bit = 1	1) Both FETs enabled when all cells >UV + hyst AND load removed 2) CHG FET enabled immediately if charger detected
PACK OVER-TEMPERATURE	Pack temperature out of range, $V_{TS} < V_{HOT}$	(1-2) × t_{THERM_CHECK}	OFF	OFF	OT FAULT protection state	TMP_REC bit = 0	V_{TS} > VHOT + hysteresis(6)
			OFF	OFF		TMP_REC bit = 1	V_{TS} > VHOT + hysteresis(6) and load removed
OVERCURRENT IN DISCHARGE	(V_{SC} – VSS) > V_{OCD}	t_{OCD}	OFF	OFF	OCD FAULT protection state	SOR bit = 0	Both ON when load removed
						SOR bit = 1	Both ON when load removed **AND** charger detected
SHORT CIRCUIT IN DISCHARGE	(V_{SC} – VSS) > V_{SCD}	t_{SCD}	OFF	OFF	SCD FAULT protection state	SOR bit = 0	Both ON when load removed
						SOR bit = 1	Both ON when load removed **AND** charger detected
SHORT CIRCUIT IN CHARGE	(V_{SS} – V_{SC}) > V_{SCC}	t_{SCC}	OFF	OFF	SCD FAULT protection state	N/A	Charger removed
OPEN THERMISTOR	V_{TS} > V_{TH_OPEN}	(1 to 2) × t_{THERM_CHECK}	OFF	OFF	OPEN THERM/UNDERTEMP protection state	N/A	V_{TS} < V_{TH_OPEN} – V_{TH_HYST}(6)
SHORTED THERMISTOR	V_{TS} < V_{TH_SHORT}	(1 to 2) × t_{THERM_CHECK}	OFF	OFF	SHUTDOWN (low-power state)		Charger detected and V_{TS} > V_{TH_SHORT} + V_{TH_HYST} (6)(7)(8)
OPEN-CELL INPUT	Cell-to-pin impedance > R_{OPEN_CELL}	(1 to 2) × $t_{OPEN\_CELL\_CHECK}$	OFF	OFF	SHUTDOWN (low-power state)		Charger detected and open-cell condition absent > filter time(9)

(1) The LDO is turned off in the SHUTDOWN mode. *When the LDO is disabled, the CHG FET drive output is OFF by default, as all outputs of the device are disabled.*

(2) Regardless of EEPROM setting, if a battery pack in the UV protection state is inserted into a charger (charger presence is detected), the CHG FET is turned ON to allow recharge of the pack. The DSG FET is turned on after UV recovery, as noted in Table 2 (conditions based on EEPROM setting).

(3) **a)** If UV_REC_DLY = 1 and any cell remains < UV + hyst for longer than 8 seconds, the device enters SHUTDOWN mode and requires insertion into charger to recover. If UV_REC_DLY = 0, the device does not enter SHUTDOWN mode from the UV FAULT protection state.

b) The LDO is turned off in the SHUTDOWN mode. *Charger insertion is required to recover from the SHUTDOWN mode.*

CAUTION: Care should be taken when using UV_REC = 0, because the power MOSFETs can oscillate when high load currents cause repeated cell UV conditions, which could result in overheating of cells or MOSFETs.

(4) If the UV_HYST_INH bit = 1, then the hysteresis threshold is inhibited and recovery occurs whenever the cells exceed the UV threshold (without hysteresis). If UV_HYST_INH = 1, the UV_REC bit should also be configured = 1. Otherwise, UV fault/recovery modes may chatter without hysteresis.

(5) If the LDO is left ON, the CHG FET is disabled when the fault condition occurs and re-enabled as soon as a charger is attached. The DSG FET is not affected.

(6) Recovery occurs within t_{THERM_CHECK}

CELL-BALANCING FUNCTION

The bq77908A implements an internal cell-balance control circuit and power FET structure. Because no CPU is available to manage a complex algorithm, a simple and robust hardware algorithm is implemented.

Overview

- Uses a separate comparator to check if cells have reached the balancing threshold to start balancing (i.e., does not use the OV trip comparator)
- Balance and charge can run concurrently – no charge-time extension
- Compare cell voltages – cell with highest voltage is bled off for time $t_{CELL\_BAL\_CHECK}$.
- Balancing current set by R_{VCX} – effect of balancing current on cell-to-cell voltage differential depends on cell capacity and $t_{CELL\_BAL\_CHECK}$.
- Cell-balancing options programmable – balancing threshold, when to balance (always, only during charge, or never), and how long to balance

Control Algorithm Description

- **Potential balancing action is updated (latched) every *minimum dwell time* $t_{CELL\_BAL\_CHECK}$**
  1. Action = bleed highest cell above cell-balance start voltage [Note: no hysteresis]
  2. Only one cell is bled at a time
  3. A minimum dwell time of 7.5 minutes equates to <0.5% capacity at 2 Ah and 50 mA balancing current)
  4. Calculation of potential balancing action is reset/inhibited when timer is expired to minimize current draw on the cell stack in case of charger termination
- **Balancing action is suppressed if any of the following are true:**
  1. Highest cell voltage < cell-balance start voltage
  2. Balance timer has expired (when configured for balancing time-out)
  3. Charger is not detected when configured to balance only in charger
  4. Cell-voltage measurement is active
- **Balancing action inhibited during cell measurement**
  1. Measure for 50 ms, balance for 200 ms per each 250-ms cycle (80% utilization)
  2. Cell measurements are *frozen* when balancing output is asserted
  3. OV, UV protection delay time is constrained to be 500 ms or longer
  4. Cell balancing is suspended when an OV/UV condition is present and is being timed for fault determination (maximum time for OV = 2.25 s; UV = 32 s).
  5. Cell balancing is resumed after the fault checking has been completed, whether faults are cleared or latched
- **Recommended system design – charger continues to *top up* the pack when connected**
  1. This may not be the case with certain chargers which shut down once charge current taper limit is reached.
  2. Timer should be enabled to prevent balancing from discharging the pack (maximum balance time is limited).
  3. Timer value is selectable via EEPROM (1, 2, 4, or 8 hours).
  4. Timer value of 4 hours limits discharge of 4-cell pack to ~2.5% at 2 Ah and 50-mA balance current; 8-cell pack to ~1.25% at 2 Ah and 50-mA balance current.
  5. Initialize timer when balancing action starts (first cell voltage > cell balance-start threshold).
  6. Suspend balancing immediately if charger is disconnected.

Balancing Algorithm Configurable Parameters

- Cell-balance start voltage: 4 bits, 3.9 V–2.4 V in 0.1-V increments, default = 3.9 V
- Cell-balance enable/control: based on charger present, timer expiration, or both (*See EEPROM map for details*)
- Time-out value (optional): 2 bits: 1, 2, 4, 8 hours

External Connections for Cell Balancing

Multiple options are supported for different cell-balancing requirements. These are summarized in the following sections. These diagrams do NOT show the other external connections such as BAT, TS, CHGST, or power FET arrangements. See subsequent sections for more complete application diagrams showing all external connections.

Normal Configuration – Balancing With Internal FETs

The basic cell balancing-configuration is shown here. Balance current must be limited using external resistance. Resistive component sizes limit the balance current as the return current flows through the VCx pins. Because resistor values are relatively low (to allow sufficient balance current), it may be necessary to maximize external capacitor sizes, depending on the filtering requirements.

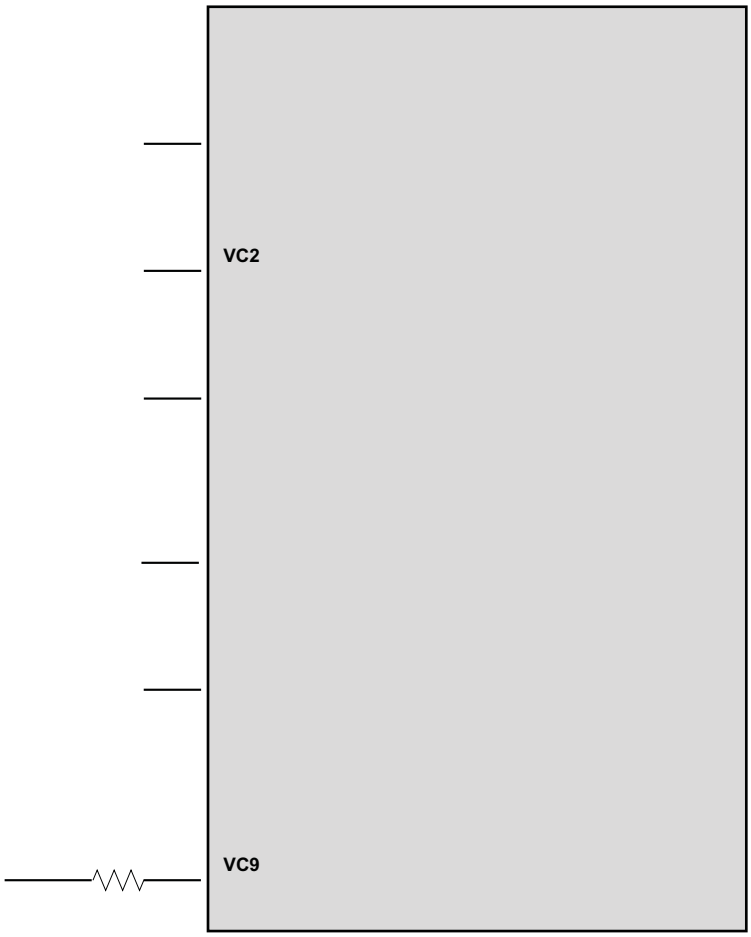


Figure 6. Typical Balancing Configuration (~50 mA)

Low-Current Cell Balancing –

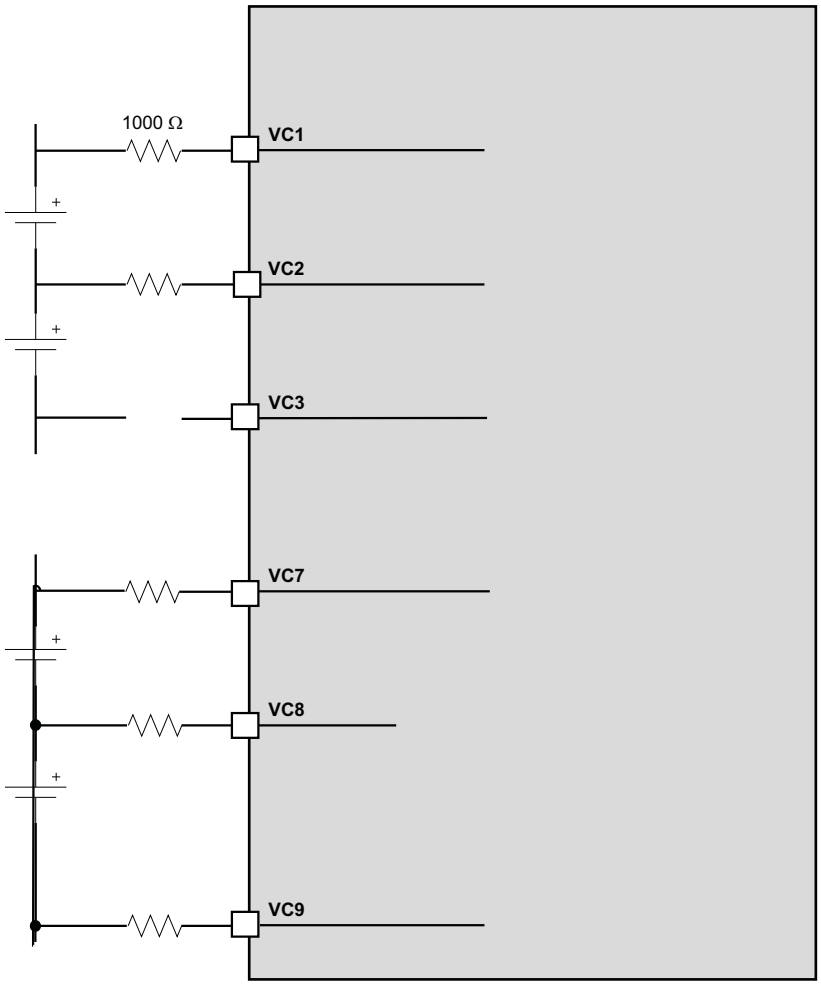


Figure 7. Typical Low-Current Balancing Configuration (~2 mA)

High-Current (Approximately 100-mA to 150-mA) Balancing Using External Power FETs

In this example, external PMOS devices are driven from the IC internal NMOS balance FETs. Current limiting is controlled by the external resistors and is on the order of 100 mA to 150 mA, depending on cell voltage. Contact TI for application example.

APPLICATION INFORMATION

Open-Cell Detection

As part of the bq77908A open-cell detection feature, a small load current is periodically applied across each cell in succession. This load results in a momentary voltage drop that reduces the apparent cell voltage measured by the bq77908A. The voltage drop must be taken into consideration when choosing the desired over voltage (OV) hysteresis and selecting resistor values for the cell input filters.

A mechanical or assembly fault during pack can cause a high-impedance or broken connection between the IC cell sense pins and the actual cells. During operation, the bq77908A periodically checks the validity of the individual cell voltage reading by applying a test current across each cell. If the connection between the pin and the cell is open the apparent cell voltage will collapse and a fault condition is detected.

Figure 8. Open-Cell Check

Detecting an Open-Cell

Referring to Figure 8, $V_{CELL,N}$ is measured as the difference between VC_A and VC_B. If the wire connecting VC_A to the cell is open, the test current will disj 213.8 0 Td 6.9 0 Td (cell)3A thre Tf 13.8 -2 Td 0acroj /F2 1I0 Tf 27.6 2 Td

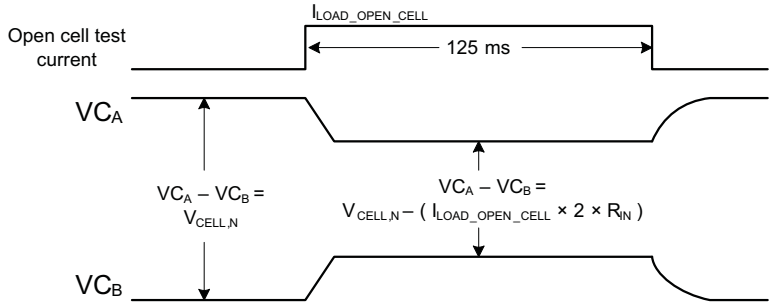


Figure 9. Effect of Open-Cell Check on Cell Voltage Measurement

Effect of Measurement Error on OV and UV Detection

The measurement error induced by the open-cell check does not affect the over voltage (OV) and under voltage (UV) fault detection accuracy because the minimum fault filtering time (500 ms) is four times longer than the time the test current is applied (125 ms). Furthermore, the test current is applied to only one cell every 4 seconds. In a system with N cells, each cell has the test current applied only once every N × 4 seconds.

Effect of Measurement Error on OV Recovery

Recovery from an OV fault occurs when the measured cell voltage drops below the OV threshold minus the OV hysteresis. Recovery is immediate; there is no minimum filtering time for fault recovery.

Therefore, an open-cell check that causes a drop in the measured cell voltage can cause a spontaneous OV recovery if the actual cell voltage minus the drop is less than the OV threshold minus the OV hysteresis setting:

$$\mathbf{V_{CELL,N}} - \left(\mathbf{I_{LOAD\_OPEN\_CELL}} \times 2 \times \mathbf{R_{IN}}\right) < \mathbf{V_{OV}} - \mathbf{V_{OV\_HYST}}$$

It is important to note that because the open-cell check is performed on only one cell at a time, spontaneous recovery due to the open-cell check will only occur if all other cells are also below the OV threshold by at least the OV hysteresis voltage.

Selection of R_{IN} and OV Hysteresis to

$$\mathbf{V_{CELL,N}} = \mathbf{V_{OV}} - \left(\mathbf{V_{OV\_HYST}} - \mathbf{I_{LOAD\_OPEN\_CELL}} \times 2 \times \mathbf{R_{IN}}\right)$$

$$\mathbf{V_{OV\_HYST,EFF}} = \mathbf{V_{OV\_HYST}} - \mathbf{I_{LOAD\_OPEN\_CELL}} \times 2 \times \mathbf{R_{IN}}$$

NOTE

Again it should be noted that $V_{OV\_HYST,EFF}$ applies only during the 125 ms during which a cell is being checked for an open condition, and only one cell is checked every 4 sec. Otherwise, the hysteresis is the programmed value V_{OV_HYST}. Therefore, the actual hysteresis observed in a system can be either of these two values. For example, if V_{OV_HYST} = 200 mV and RIN = 56 Ω, the observed hysteresis can be either 150 or 200 mV (see Table 3).

Additionally, when selecting the appropriate value for lower R_{IN}, the upper limit on cell balancing of 50 mA per cell must be observed. For example, if your cells have a maximum of 4.3 V, each R_{IN} must not fall below 43 Ω, as (4.3 V / (2 × 43 Ω) = 50 mA. If such lower resistances are to be used, the cell balancing feature must be disabled.

Table 3. $V_{OV\_HYST,EFF}$ for Various V_{OV_HYST} and R_{IN} Selections

VOV_HYST (mV)	RIN (Ω)	VOV_HYST,EFF (mv)
0	This Setting Must Only Be Used When Not Directly Controlling FETs with the CHG/DSG Outputs and Recovery Decisions are Made By A Separate Device	
25		
50	44	10
100	83	25
100	56	50
150	139	25
150	111	50
150	56	100
200	194	25
200	167	50
200	111	100
200	56	150
250	250	25
250	222	50
250	167	100
250	111	150
250	56	200
300	306	25
300	278	50
300	222	100
300	167	150
300	111	200

Internal Voltage Regulator

The bq77908A has an integrated low-power linear regulator that provides power to both internal and any optional user-defined external circuitry. The input for the regulator is derived from the BAT terminals. VREG nominal output value is 3.3 V and is also internally current-limited. The minimum output capacitance for stable operation is 1 µF.

The regulator (and the IC internal circuitry) is disabled during the SHUTDOWN mode. When the regulator circuit is disabled (including the time during the power-up sequence of the IC) the DSG and CHG FETs are driven OFF.

Charger Detection and Wake-Up

The bq77908A contains a mechanism to detect the presence of an external charger and allow the device to wake up from the low-power shutdown mode when the LDO has been turned off. A low-power wake-up circuit monitors the CHGST pin to determine the charger connection event.

CHGST Pin Detection

Because the bq77908A is designed to use low-side NMOS FETs to control current flow to/from the battery pack, charger presence detection cannot be determined simply by checking the positive terminal voltage. To allow detection of the presence/absence of an external charger under any operating conditions, the bq77908A implements a charger sense pin, designated CHGST. If a voltage of greater than (nominally) 0.5 V is detected at the CHGST pin, the bq77908A logic assumes that a charger has been connected. *The voltage monitoring circuit at the CHGST pin is an always-on subsystem within the chip. When the proper voltage appears at the CHGST pin, the IC wakes up from the SHUTDOWN mode after a charger is connected.* If fault conditions exist, the part may re-enter a low-power or SHUTDOWN state, depending on the configuration.

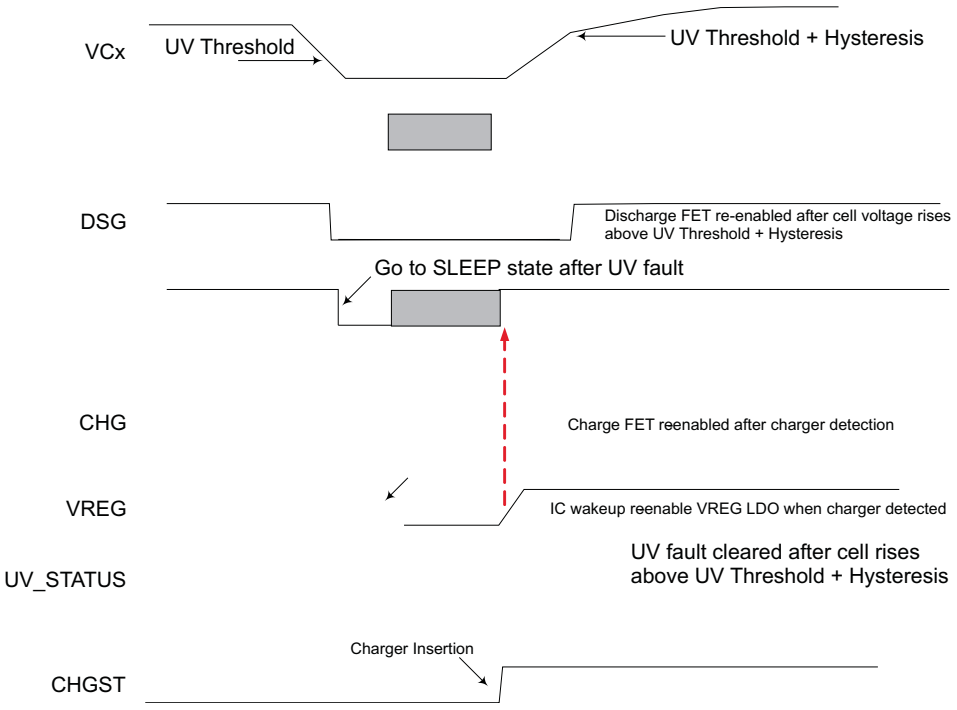
The means of connecting the CHGST pin is user- and application-dependent, and may vary with the external contact structure of the battery pack.

For example, a dedicated CHARGER(+) contact with attenuating resistors can be used such that the CHGST pin is pulled high whenever the pack is inserted into a charger.

For a system/application which uses a charge-protection FET to disconnect the charger (–) during a fault condition, it is recommended that the connection to the CHGST pin be pulled up to the charger (+) potential (using a pullup resistor) on the charger side to prevent this signal from going negative with respect to the pack internal reference (VSS pin) when the charge FET in the battery pack may be open.

If the system does not use a charge FET within the battery pack, the VSS (internal) reference and CPCKN (charger reference) are the same, which allows CHGST to be pulled up to any logic-high level above V_{CHG_DET1} to detect charger insertion.

A timing diagram corresponding to the UV fault/recovery condition using the CHGST signal is shown in



Temperature Sensing

TS and VTSB Pin Interface

The bq77908A uses the TS pin input to read the voltage on an external thermistor to determine the pack/system temperature. The VTSB pin allows the IC to generate its own bias voltage to drive the thermistor. To save power, the VTSB bias supply is pulsed ON only when the temperature readings are being taken. The VTSB pin is powered by the LDO output (VREG) and with a maximum output impedance of 150 Ω.

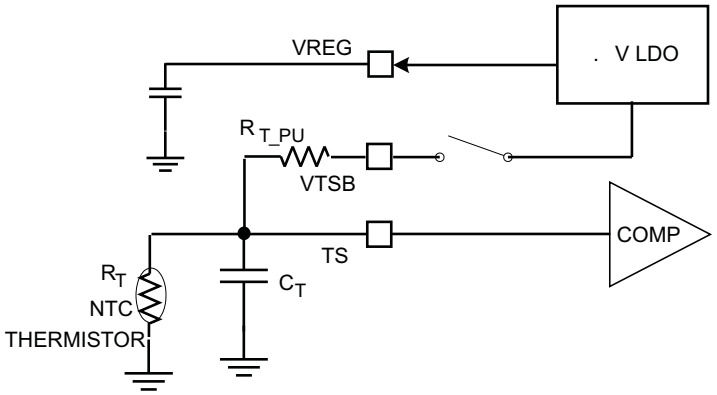


Figure 11. TS and VTSB Pin Interface

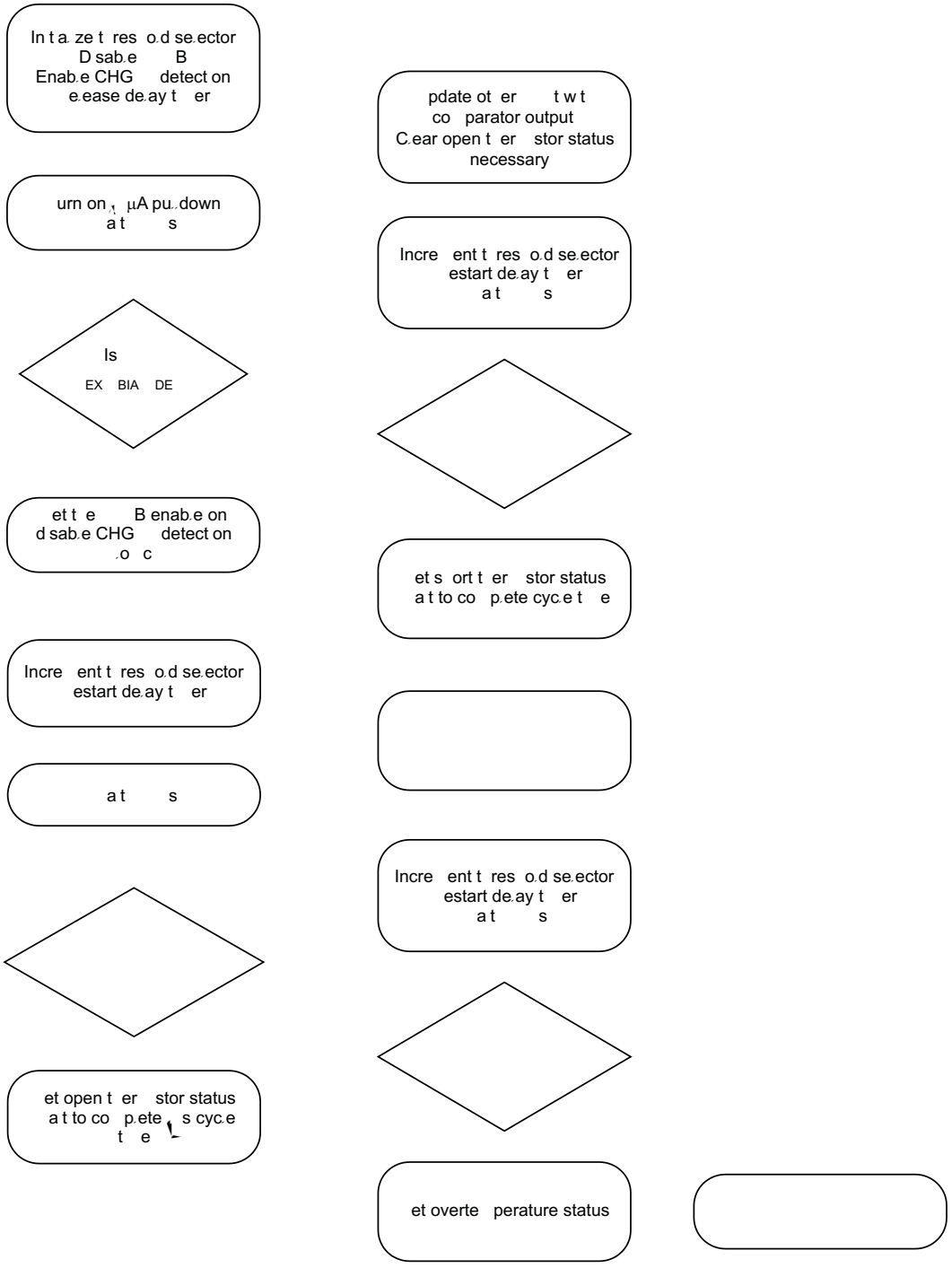
A negative-temperature-coefficient thermistor in the topology shown in Figure 11 is assumed. With this arrangement, the *voltage* at the TS will be lower for high temperature, and higher for low temperature. If the voltage measured at the TS pin is below the V_{HOT} threshold, a pack overtemperature condition is detected.

In the extreme fault cases, an open (disconnected) thermistor indicates a voltage at the TS pin equivalent to the VREG pullup voltage, and a shorted thermistor indicates a voltage close to 0 (VSS). An open-thermistor fault recovers within the fault filter time following removal of the open condition. Shorted-thermistor detection places the device into the low-power SHUTDOWN mode, requiring re-insertion into a charger for wakeup.

External Bias Supply Detection

During the time period in which the bq77908A checks the thermistor status, a weak (nominal 1-µA) current is applied from the TS pin to VSS. If V_TS > V_EXT_PU, then the IC operates as if an external supply is present and does not enable the VTSB internal supply. A sequence of operations is performed to determine the existence of shorted thermistor, open thermistor, or pack overtemperature faults as listed in the following section.

Temperature Measurement/Fault Detection Logic Flow Diagram



Battery Pack/Charger Shared-Thermistor Functionality

The pulsing of the VTSB pin is enabled ONLY when the IC determines that there is no external supply (e.g., from the charger) already driving the thermistor. This allows a single thermistor to be used by both the bq77908A and the external charger to measure pack temperature. This can also be used as a method of charger presence detection in case a dedicated charger-detect pin is not implemented in the end-equipment pack design.

By connecting the CHGST pin to the TS pin on the battery-pack internal circuit board, a three-terminal battery-pack design with (+), (–) and (T) (thermistor) contacts is compatible with the charger-detection mechanism of the bq77908A. Because the external charger normally applies a bias voltage to the TS pin from an external source, there is a voltage present on the CHGST pin whenever the pack is inserted into the charger.

NOTE

V_{TH_xxx} (thresholds) are ratiometric based upon VREG. Care should be taken if using an external pullup to a voltage other than the VREG voltage to account for the difference in these detection thresholds.

Depending on the arrangement of the power FETs within the pack, the sharing of a common thermistor between the BMU and the external charger may not be feasible. Applications which **do not** use a CHG disconnection FET are supported, because there is a common ground reference between the external charger and the internal IC ground.

In case of applications which **do** use a CHG FET, the following issues should be understood from the system point of view:

- When the CHG FET is disabled (as in a fault condition), the internal reference (VSS pin of the IC) is disconnected from the external reference (CPCKN connected to charger return path).
- When a charger is connected and powered on, the CPCKN voltage is negative, and it is possible that the CHGST pin is negative with respect to the IC VSS pin.
- The CHGST and TS pins are not internally protected from negative voltages.
- If an external clamp circuit is used to prevent the CHGST voltage from going below 0 V with respect to VSS, and the CHGST/TS pins are connected within the pack, the TS pin indicates an invalid temperature range (or perceived thermistor-shorted fault) until the CHG FET is closed.
- If a charger is connected and not powered on, the CHGST pin may be pulled up to the PACK+ rail. This pin is internally clamped to a safe voltage; however, series resistance is required to avoid overcurrent damage to the internal clamping circuit. If the CHGST and TS pins are tied together within the pack, this resistance affects the reading of the pack internal thermistor by the external device.
- Ideally, the external charger should be designed such that a negative voltage (with respect to the pack internal VSS) cannot be imposed on the CHGST/TS pin when a charger is connected.
- In the case of the CHG FET ON and current flowing, the CPCKN potential may be a few hundred millivolts below the IC VSS pin (depending on charge current level and charge FET on-resistance). This also affects the accuracy of the thermistor voltage as read by the external charger. A suggested approach is for the external charger to momentarily interrupt charge current flow while taking the pack temperature reading when a CHG FET is implemented.

Charge/Discharge Enable Operating Thresholds

If the voltage measured at the TS pin is below V_{TH_HOT}, a pack overtemperature condition is detected. The bq77908A disables the charge and discharge FETs (but remains in the active mode). Using a standard 103AT thermistor and 10-kΩ pullup resistor, this corresponds to approximately 60°C. The temperature level is chosen to be slightly above the normal charge disable level implemented by an external charger, and would not normally activate during charge unless the charger's own overtemperature shutdown did not trigger before this level. The external charger typically also has a cold-temperature charge inhibit (roughly between 0°C and 10°C) as shown in Figure 12.

Figure 12. Typical Thermistor Response and Protection Thresholds (VTSB = 3.3 V, Pullup = 10 kΩ)

The

Additionally, if UV_REC_DLY = 1 and all the cell voltages remain $<V_{UV}$ + hysteresis for more than 8 seconds, then the bq77908A enters the SHUTDOWN mode.

If UV_REC_DLY = 0, the part does not enter SHUTDOWN mode from a UV fault condition.

Once in the SHUTDOWN mode, insertion into a charger is required to exit the SHUTDOWN mode.

When in the SHUTDOWN mode, the LDO turns off.

This recovery criterion is described in the fault summary of Table 2 and the *Cell Undervoltage Detection and Recovery* section.

Pack/System Connection Arrangements

The architecture and fault detection/recovery logic allows the system developer to implement multiple types of battery-pack topologies using the bq77908A. A few basic application cases are illustrated here; however, others are also possible as long as the external connections and host-equipment interface are compatible with the fault detection and recovery signaling methods.

Notes regarding the application schematics:

- A five-cell configuration is shown for simplicity. All unused cell inputs (not shown) are tied to the PACK(+) positive terminal.
- For configurations which do not implement a CHG FET, it is assumed that the CHGST pin (in bq77908A) is pulled up inside the charger equipment (nominally V_{CHG_DET1}).
- Gate-source pulldown resistances are recommended for the power FETs to prevent parasitic turnon when the bq77908A is in shutdown mode. This may have a slight impact on operating current when FETs are enabled; however, very large resistances (~ 5 MΩ) may be used to minimize this effect.
- Series resistance between the CHG/DSG pins and FET gates should be sized to assure quick turnoff of the FETs used.
- High-current (pack discharge/charge) flow paths are indicated by wide traces; low-current signal paths use narrow traces in the following schematics.

Series CHG and DSG FET Configuration

Use of a separate contact (i.e., CHGST) for charger detection is preferred if the cell-balancing function is used. This is to allow balancing to occur only while charging. Otherwise, if the part cannot detect the presence of a charger, balancing must be enabled to occur at all times or not at all. The CHGST pin should be protected from possible negative voltage inputs which may occur if connected to a charger with the CHG FET open.

NOTE

In shutdown with the LDO off, the specified shutdown currents require that the voltage at CPCKN with respect to VSS is controlled. In the parallel FET case, CPCKN is clamped through the body diode of the charge FET. In the series FET case, external circuitry is required to keep CPCKN from floating. Contact TI for recommended application circuits.

If current is able to flow from CPCKN through the charge FET (e.g., through the body diode), the resistor R_{LDRM_DET} is required to discharge DPCKN for proper detection of load removal. When the FETs are open and a load is present, the PACK– terminal and consequently DPCKN is pulled up to PACK+. When the load is removed, DPCKN is discharged through R_{LDRM_DET}. Detection of load removal occurs when the voltage at DPCKN (referenced to VSS) falls below 2 V (typical).

whenbe)

Figure 13. Example Series FET Configuration Using the CHGST Pin

Separate CHG(–) and DSG(–) Return Paths With Both FETs

In this configuration, if the charge current is typically much lower than the discharge current, a lower-cost component can be used for the charge control FET than in the series configuration previously shown.

Use of a separate contact (CHGST pin) is preferred if the cell balancing function is used. This is to allow balancing to occur only while charging. Otherwise, if the part cannot detect the presence of a charger, balancing must be enabled to occur at all times or not at all.

The CHGST pin should be protected from possible negative voltage inputs which may occur if connected to a charger with the CHG FET open.

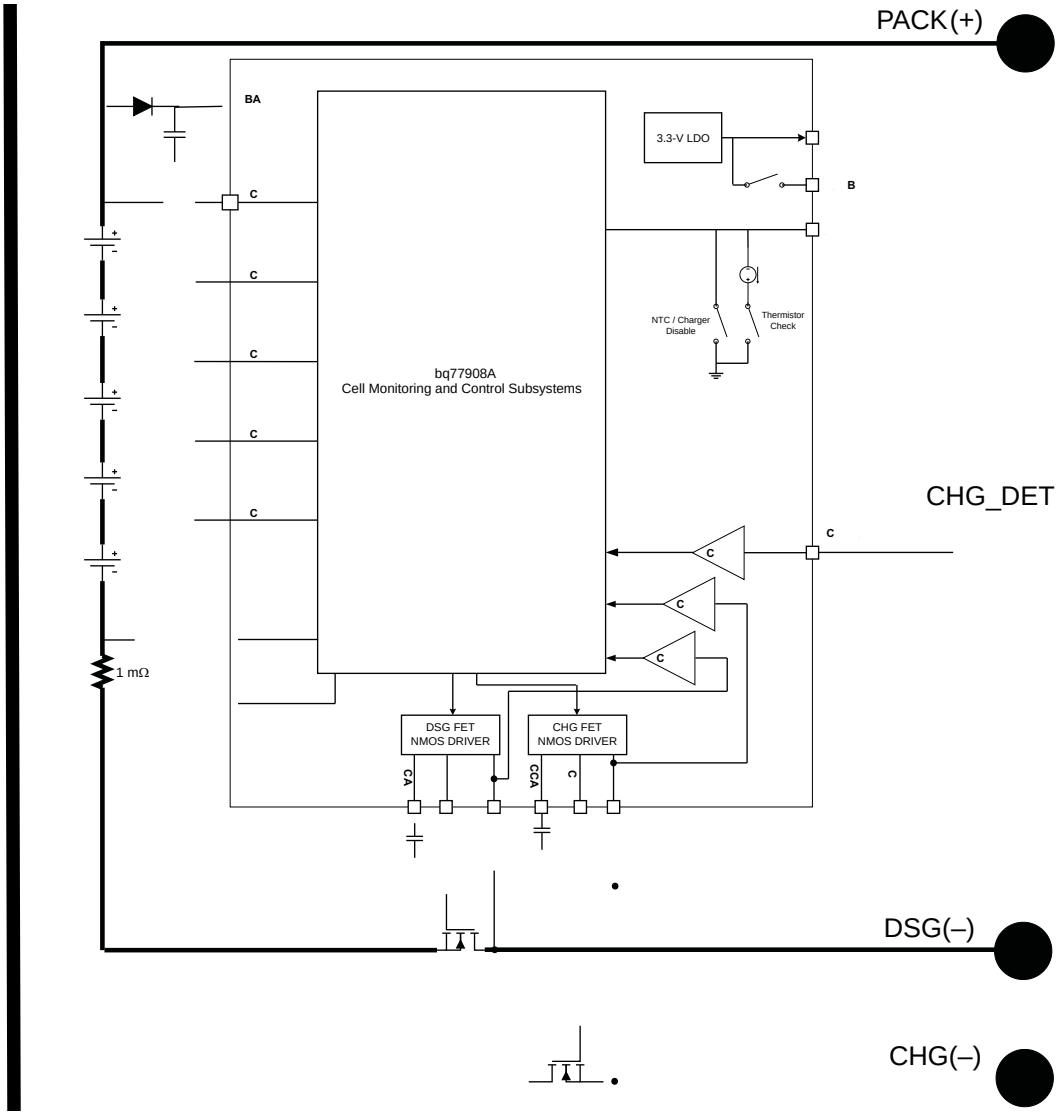


Figure 14. Example Parallel (Split) Power Path FET Configuration Using CHGST Pin

Separate CHG(–) and DSG(–) Return Paths With DSG FET Only

In this configuration, no charge-control FET is implemented. As a result, the bq77908A is unable to interrupt charge current when an overvoltage condition occurs. The suggested method to stop the charger in an overvoltage event is to use the thermistor signal to indicate a fault condition. The system should configure the OV_TS_CTRL bit high, so that when an overvoltage occurs, the charger detects that an overtemperature condition has occurred, and halts charging. (See the *OV_TS_CTRL (EEPROM Bit) Interface* section.)

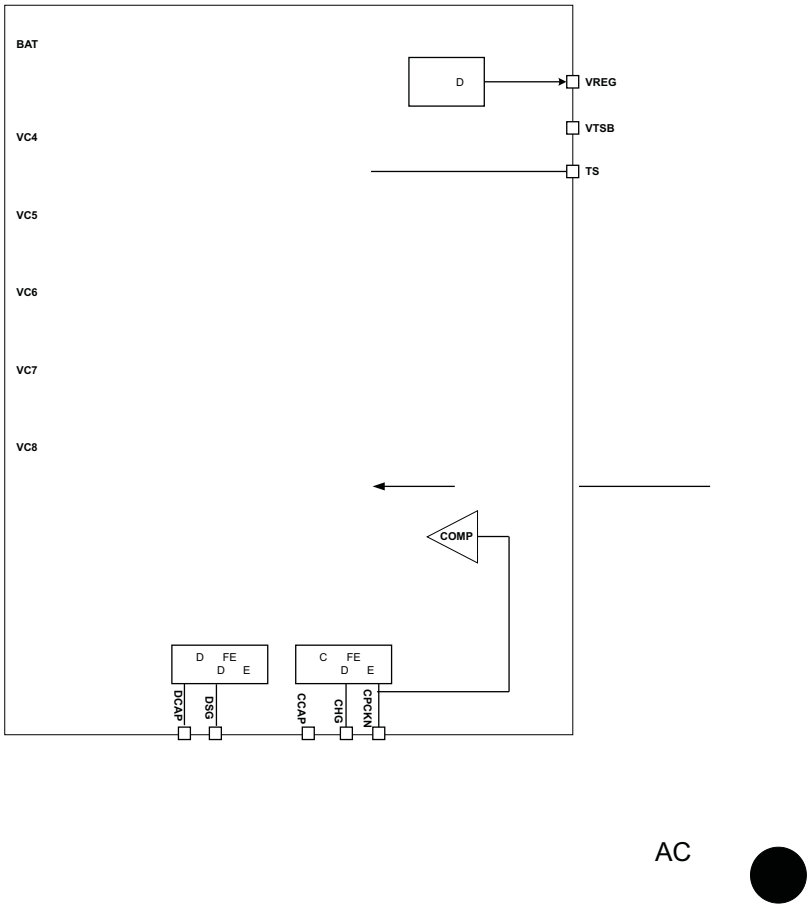


Figure 16. Single Power Path, No FETs

4- to 8-Series Cell Configuration

All cell input pins of the device are used for a 8-cell battery pack application. The bq77908A supports pack configurations ranging from 4- to 8-series cells. If fewer than 8 cells are used in an application, all unused VCx cell input pins should be tied together and pulled up to the most-positive cell input. Pullup resistance value is not critical; a 100 Ω–1000-Ω value is suggested. An example for a 5-cell application is shown here. Cell configuration is programmable by EEPROM, using the SYS_CFG register bits CNF[2:0].

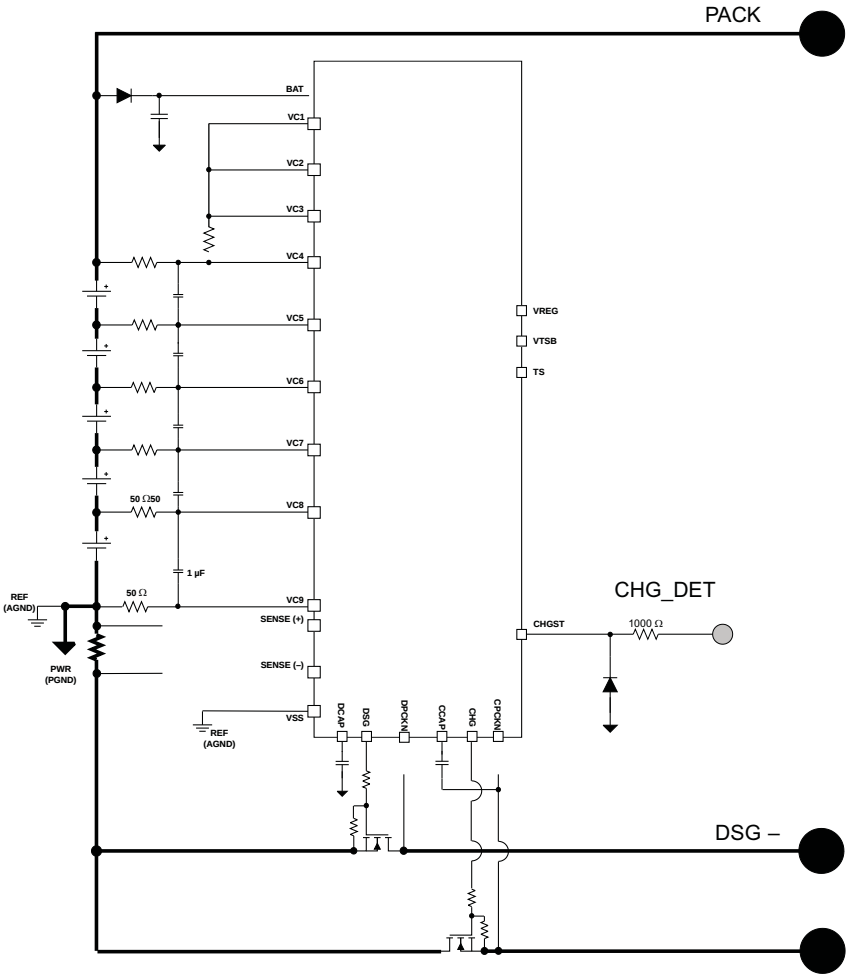


Figure 17. Unused VCELLx Pin Configuration

Delay Time Zero

The ZEDE pin enables the EEPROM-programmed detection-delay times when connected to VSS (normal operation). A strong pulldown to VSS is recommended to prevent external circuit noise from causing ZEDE to go high. The detection delay time is set to minimum when this pin is connected to VREG. This is used in battery manufacturing test. When programming the EEPROM, this pin should to be connected to VREG to enable the serial communication interface.

Ship-Mode Equivalent Functionality

Because the BMU is designed for standalone-mode operation, it does not incorporate a programmable-entry *ship mode*, which is intended for long-term storage of a battery pack after initial assembly.

The recommended method to allow an equivalent functionality is to cause the IC to enter into the low-power shutdown state with the LDO disabled. When the end-user first receives the battery and system, the pack must be (at least momentarily) inserted into a charger to wake up the BMU and allow normal operation. The following procedure can be used:

1. Simulate a fault condition by driving TS pin voltage < V_{TH_SHORT} by either method:
   (a) After pack assembly, connect the TS pin to VSS for > 8 seconds, or
   (b) Disable delay time (pull ZEDE to logic high) AND connect TS to VSS for > 1 second.
2. As shown in the fault detection/recovery table, the device goes into low-power shutdown mode due to a perceived shorted-thermistor fault.

For battery packs which allow the TS pin signal to be brought to an external contact, the above procedure can be implemented after final pack mechanical assembly. Use of the TS pin to simulate a fault avoids the risks associated with forcing a momentary cell UV condition after the pack has been fully or partially assembled.

SERIAL COMMUNICATION INTERFACE

Device Addressing and Protocol Overview

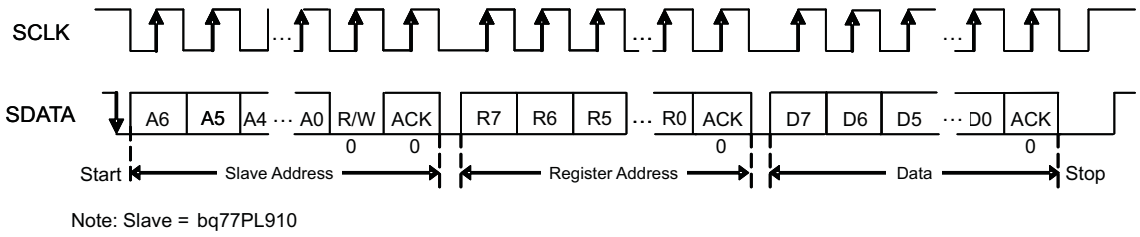
The bq77908A uses a subset of the I^2C communication protocol to allow programming and test of internal registers. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq77908A acts as a slave device and does not generate clock pulses; it must be addressed and controlled from an external I^2C bus master device. The slave address for the bq77908A has a 7-bit value of 0010 000.

The bq77908A communications protocol varies from the full I^2C standard as follows:

- The bq77908A is always regarded as a slave.
- The bq77908A does not support the general code of the I^2C specification.
- The bq77908A does not support address auto-increment, which allows continuous reading and writing.
- The bq77908A allows data to be written or read from the same location without re-sending the location address.

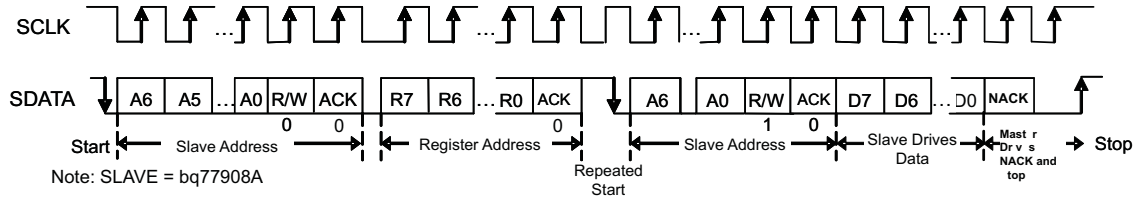
	(MSB)			I^2C Address +R/W bit				(LSB)
	(MSB)			I^2C Address			(LSB)	
Write	0	0	1	0	0	0	0	0
Read								1

Bus Write Command to bq77908A



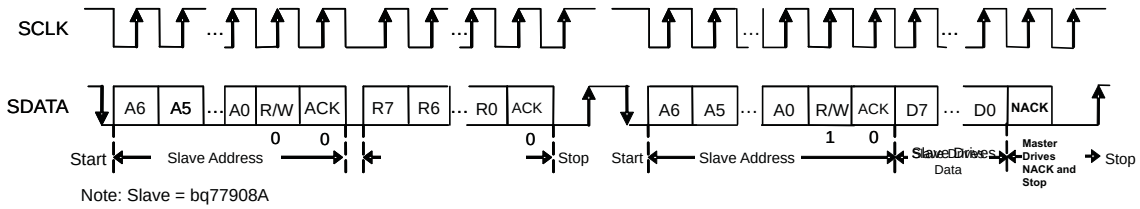
Note: Slave = bq77PL910

Bus Read Command from bq77908A (Protocol A)

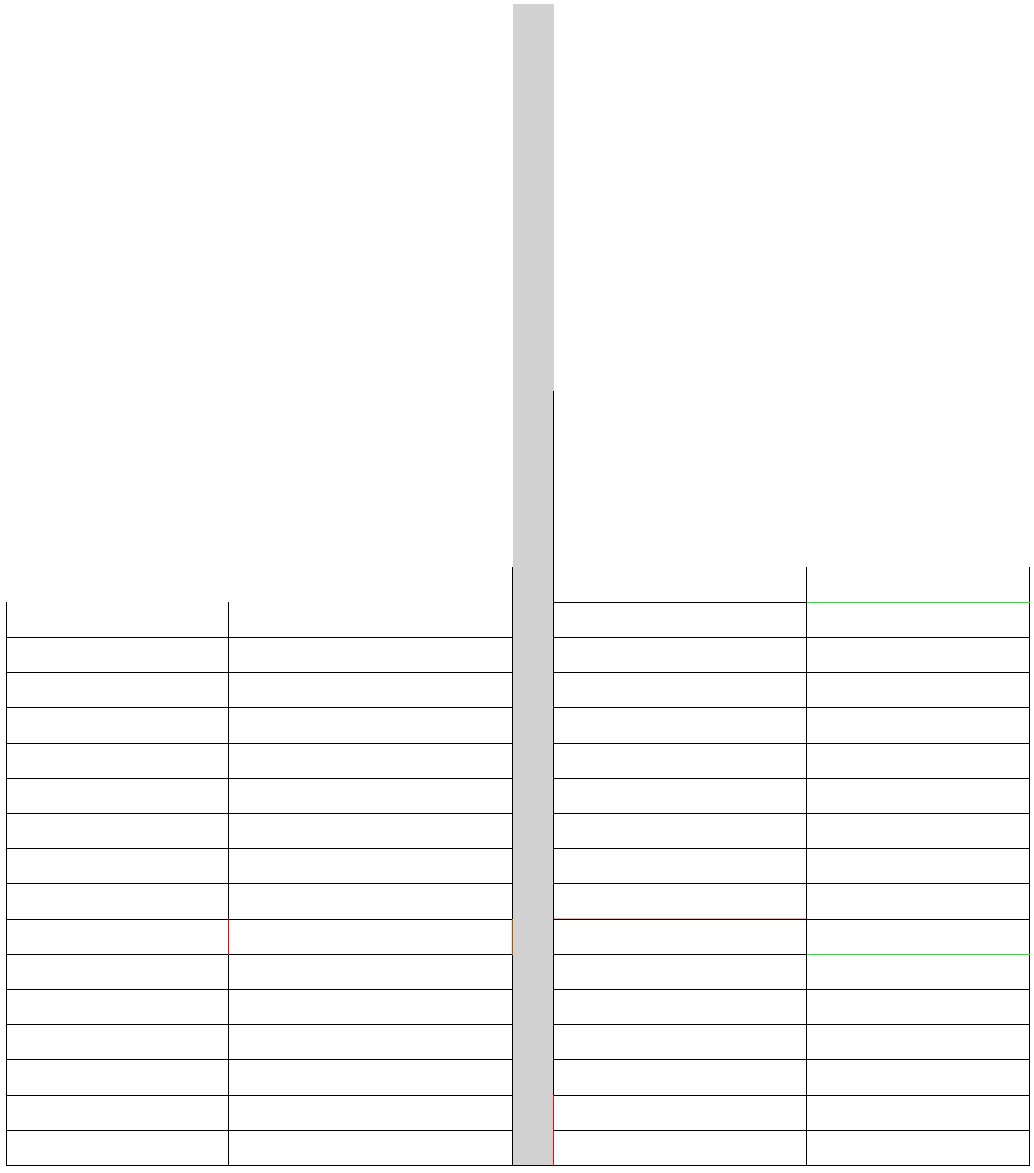


Note: SLAVE = bq77908A

Bus Read Command from bq77908A (Protocol B)



Note: Slave = bq77908A



OV Detection Configuration #2 (OV_CFG2, Address 0x03)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	OV_TS_CTRL	OVH2	OVH1	OVH0	OV_TSRSTB	OVD	OVD1	

UVT[3:0]	UV Trip Level (Volts)		UVT[3:0]	UV Trip Level (Volts)
0000	1.4		1000	2.2
0001	1.5		1001	2.3
0010	1.6		1010	2.4
0011	1.7		1011	2.5
0100	1.8		1100	2.6
0101	1.9		1101	2.7
0110	2.0		1110	2.8
0111	2.1		1111	2.9

UV Detection Configuration #2 (UV_CFG2, Address 0x05)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	**UV_REC**	**UV_REC_DLY**	**UVH1**	**UVH0**	**RSVD10**	**UVD2**	**UVD1**	**UVD0**
If 0	Recover from UV fault when all cell voltages increase above V_{UV} threshold+hyst. CHG FET enabled immediately if charger detected	Part does NOT enter SHUTDOWN mode from the UV fault state	1 of 4 possible values, see table below		NOT USED	1 of 8 possible values, binary spacing, see following table.		
If 1	Recover from UV fault only when all cell voltages increase above V_{UV} threshold+hyst *AND* load is removed.	Part *does* enter SHUTDOWN mode if any cell voltage remains <V_{UV}+hyst for >8 seconds in the UV fault state			NOT USED			

UV Hysteresis Level

The UV hysteresis is set using UVH[1:0] bits. Four possible values are available as shown; however, the maximum recovery level is set to 3.5 V in the case of a combination of high UV trip point plus high UV hysteresis values.

UVH[1:0]	Hysteresis (Volts)
00	0.4
01	0.8
10	1.2
11	1.6

Recovery Voltage (Combination of UVT + UVH settings)

UV Trip Level	Hysteresis			
	0.4 V	0.8 V	1.2 V	1.6 V
1.4	1.8	2.2	2.6	3.0
1.5	1.9	2.3	2.7	3.1
1.6	2.0	2.4	2.8	3.2
1.7	2.1	2.5	2.9	3.3
1.8	2.2	2.6	3.0	3.4
1.9	2.3	2.7	3.1	3.5
2.0	2.4	2.8	3.2	3.5
2.1	2.5	2.9	3.3	

UV Delay Time

Eight possible time delay settings for the UV trip delay are selectable using the UVD[2:0] bits as shown.

UVH[2:0]	Delay (Seconds)
000	0.5
001	1
010	2
011	4
100	8
101	16
110	32
111	OFF

Overcurrent in Discharge Delay Settings (OCD_DELAY, Address 0x06)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RSVD11	RSVD12	RSVD13	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0
If 0	NOT USED	NOT USED	NOT USED	One of 32 possible delay settings, see following table.				
If 1	NOT USED	NOT USED	NOT USED					

Discharge Overcurrent Detection Delay Settings

OCDD[4:0] (HEX)	OC Detection Delay (ms)		OCDD[4:0] (HEX)	OC Detection Delay (ms)
0x00	20		0x10	500
0x01	40		0x11	600
0x02	60		0x12	700
0x03	80		0x13	800
0x04	100		0x14	900
0x05	120		0x15	1000
0x06	140		0x16	1100
0x07	160		0x17	1200
0x08	180		0x18	1300
0x09	200		0x19	1400
0x0A	220		0x1A	1500
0x0B	240		0x1B	1600
0x0C	260		0x1C	1700
0x0D	280		0x1D	1800
0x0E	300		0x1E	1900
0x0F	400		0x1F	2000

Short Circuit in Discharge Delay Settings (SCD_DELAY, Address 0x07)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RSVD14	RSVD15	ISNS_RNG	SCDD_RNG	SCDD3	SCDD2	SCDD1	SCDD0
If 0	NOT USED	NOT USED	Use lower range of values for all short-circuit and overcurrent-trip thresholds	Use fast delay settings	One of 16 possible delay settings in each range, see following table.			
If 1	NOT USED	NOT USED	Use higher range of values for all short-circuit and overcurrent-trip thresholds	Use slow delay settings				

SCD Delay Settings

Two separate ranges of 16 possible delay time values are selectable as shown here.

Fast Range (SCDD_RNG = 0)			Slow Range (SCDD_RNG = 1)	
SCDD[3:0]	SC Detection Delay (μs)		SCDD[3:0]	SC Detection Delay (ms)
0x00	60		0x00	50
0x01	120		0x01	100
0x02	180		0x02	200
0x03	240		0x03	300
0x04	300		0x04	400
0x05	360		0x05	500
0x06	420		0x06	600
0x07	480		0x07	700
0x08	540		0x08	800
0x09	600		0x09	900
0x0A	660		0x0A	1000
0x0B	720		0x0B	1100
0x0C	780		0x0C	1200
0x0D	840		0x0D	1300
0x0E	900		0x0E	1400
0x0F	960		0x0F	1500

Discharge Overcurrent/Short-Circuit Trip Levels (OCD_SCD_TRIP, Address 0x08)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	SCDT3	SCDT2	SCDT1	SCDT0	OCDT3	OCDT2	OCDT1	OCDT0
If 0	One of 16 possible SC trip settings (sense resistor voltage), see following table.				One of 16 possible OC trip settings (sense resistor voltage), see following table.			
If 1								

NOTE: SCD and OCD trip levels are controlled by current-sense gain-control bit ISNS_RNG located in register 0x07. Trip levels measured at SENSE– are referenced to SENSE+.

Discharge Short-Circuit Trip-Level Settings (Sense-Resistor Voltage)

SCDT[3:0]	Discharge Short-Circuit Trip Level, mV at SENSE (–), With ISNS_RNG = 0	Discharge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	40	200
0001	50	250
0010	60	300
0011	70	350
0100	80	400
0101	90	450
0110	100	500
0111	110	550
1000	120	600
1001	130	650
1010	140	700
1011	150	750
1100	160	800
1101	170	850
1110	180	900
1111	190	950

Discharge Overcurrent Trip-Level Settings (Sense-Resistor Voltage)

OCDT[3:0]	Discharge Overcurrent Trip Level, mV at SENSE(–), With ISNS_RNG = 0	Discharge Overcurrent Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	25	125
0001	30	150
0010	35	175
0011	40	200
0100	45	225
0101	50	250
0110	55	275
0111	60	300
1000	65	325
1001	70	350
1010	75	375
1011	80	400
1100	85	425
1101	90	450
1110	95	475
1111	100	500

Charge Short-Circuit Threshold and Delay Settings (SCC_CFG, Address 0x09)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	SCCD3	SCCD2	SCCD1	SCCD0	SCCT3	SCCT2	SCCT1	SCCT0
If 0	One of 16 possible charger short-circuit sensing delay settings, see following table.				One of 16 possible charger short-circuit sensing threshold settings (sense resistor voltage), see following table.			
If 1								

NOTE: SCC trip-level range is controlled by current-sense gain-control bit ISNS_RNG, located in register 0x07. Trip levels measured at SENSE– are referenced to SENSE+.

Charge Short-Circuit Delay-Time Settings

SCCD[3:0]	Charge Short-Circuit Delay (µs)		SCCD[3:0]	Charge Short-Circuit Delay (µs)
0000	60		1000	540
0001	120		1001	600
0010	180		1010	660
0011	240		1011	720
0100	300		1100	780
0101	360		1101	840
0110	420		1110	900
0111	480		1111	960

Charge Short-Circuit Trip-Level Settings

SCCT[3:0]	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 0	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	–10	–50
0001	–15	–75
0010	–20	–100
0011	–25	–125

SCCT[3:0]	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 0	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0100	–30	–150
0101	–35	–175
0110	–40	–200
0111	–45	–225
1000	–50	–250
1001	–55	–275
1010	–60	–300
1011	–65	–325
1100	–70	–350
1101	–75	–375
1110	–80	–400
1111	–85	–425

Cell-Balancing Configuration (CELL_BAL_CFG, Address 0x0A)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	CB_EN1	CB_EN0	CBT1	CBT0	CBV3	CBV2	CBV1	CBV0
If 0	See 4 possible values following		See 4 possible values following		One of 16 possible settings for cell-balance threshold (highest cell voltage to initiate balance action)			
If 1								

Cell-Balance Enable Control

CB_EN[1:0]	Cell Balance Function
00	Disable cell-balance function
01	Enable cell-balance function(1) at all times – start balancing (timer counting) whenever CBV threshold is reached, terminate when timer expires. Balancing restarts once all cells have first fallen below the CBV threshold and then at least one cell again reaches the CBV threshold.
10	Enable cell balance function(1) when charger detected, terminate when charger removed. *(Note: This is recommended only with chargers that keep the battery topped-off, i.e., maintenance charge implemented after regular charge completion.)*
11	Enable cell-balance function(1) when charger is detected, terminate when charger is removed OR when timer expires. Following timer expiration, the charger must be disconnected then reconnected to restart balancing.

(1) *Enable cell balance function* means that the logic checks cell voltages to decide if balancing action (current bleed/bypass) should occur. *Start balancing* is defined as the time when the algorithm is active, i.e. actually diverting current around a cell. Timer initiation begins when balancing action starts, not when charger is detected.

Cell-Balance Timer

Cell balancing, if enabled, begins when the charger is present and the first cell exceeds the CBV start threshold. Cell balancing is terminated when the charger is removed, or after CBT timeout interval regardless of charger-removal detection. This method is used to prevent continuous drain of the cells in the case where the battery pack is stored in the charger after charge termination.

CBT[1:0]	Timeout Length (Hours)
00	1
01	2
10	4
11	8

Cell Balance Voltage Threshold Settings

When any cell reaches the programmed setting, the cell balance algorithm begins as discussed previously in the operation/applications section. Cell balancing must be enabled via the CB_EN control bit, and in some cases (see the *Cell-Balance Enable Control* section) the charger must be detected for the algorithm to initiate.

CBV[3:0]	Cell Voltage
0000	3.9
0001	3.8
0010	3.7
0011	3.6
0100	3.5
0101	3.4
0110	3.3
0111	3.2
1000	3.1
1001	3.0
1010	2.9
1011	2.8
1100	2.7
1101	2.6
1110	2.5
1111	2.4

EEPROM Control Register (EEPROM, Address 0x0B)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	EEPROM7	EEPROM6	EEPROM5	EEPROM4	EEPROM3	EEPROM2	EEPROM1	EEPROM0

These bits enable data write to EEPROM locations (0x01–0x0A) when written with data 0100 0001 (0x41). Pre-read of EEPROM data is available by setting these bits with 0110-0010 (0x62). Default is 0000-0000 (0x00).

EEPROM Write Sequence

EEPROM is written by I^2C command. When ZEDE = H, the SCLK and SDATA lines are enabled to allow I^2C communication.

	(MSB)			I^2C Address +R/W bit				(LSB)
	(MSB)			I^2C Address			(LSB)	
Write	0	0	1	0	0	0	0	0
Read								1

The bq77908A has integrated configuration EEPROM for OV, UV, OCD, SCD, and SCC thresholds and delays. The appropriate configuration data is programmed to the configuration registers and then 0x41 is sent to the EEPROM register to enable programming. By driving the EEPROM pin (set high and then low), the data is written to the EEPROM. The recommended voltage at BAT for EEPROM writing is >7 V. A flowchart showing the EEPROM write/check sequence is shown in Figure 18.

Parity Check

The bq77908A uses EEPROM for storage of protection thresholds and delay times as previously described. Additional EEPROM is also used to store internal trimming data. For safety reasons, the bq77908A uses a column-parity error-checking scheme. If the column-parity bit is changed from the written data, both DSG and CHG FETs are forced OFF as a fail-safe mechanism.

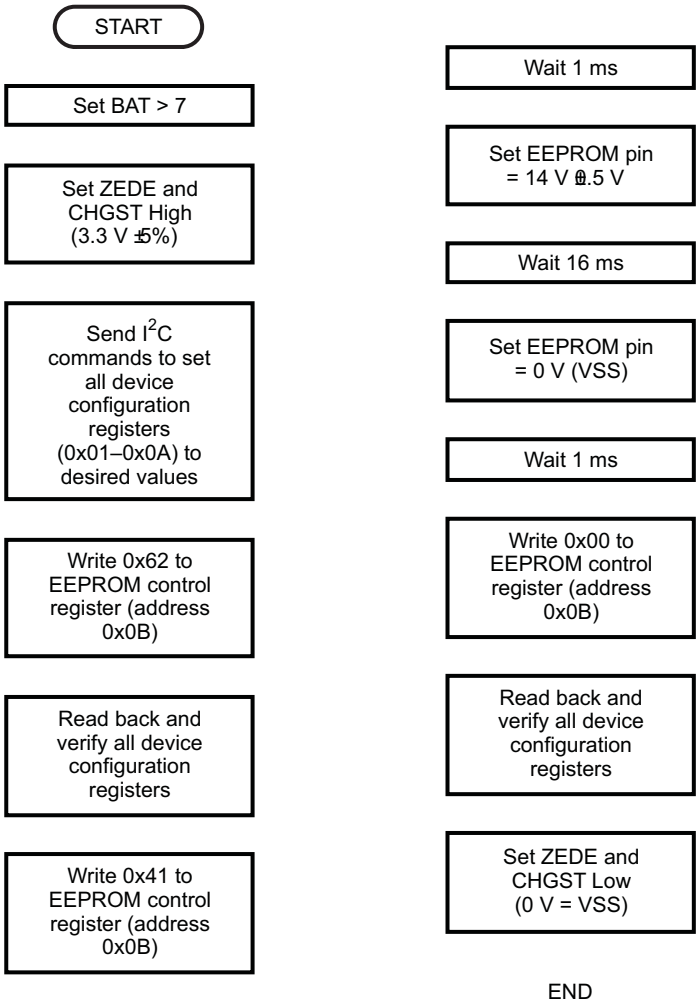
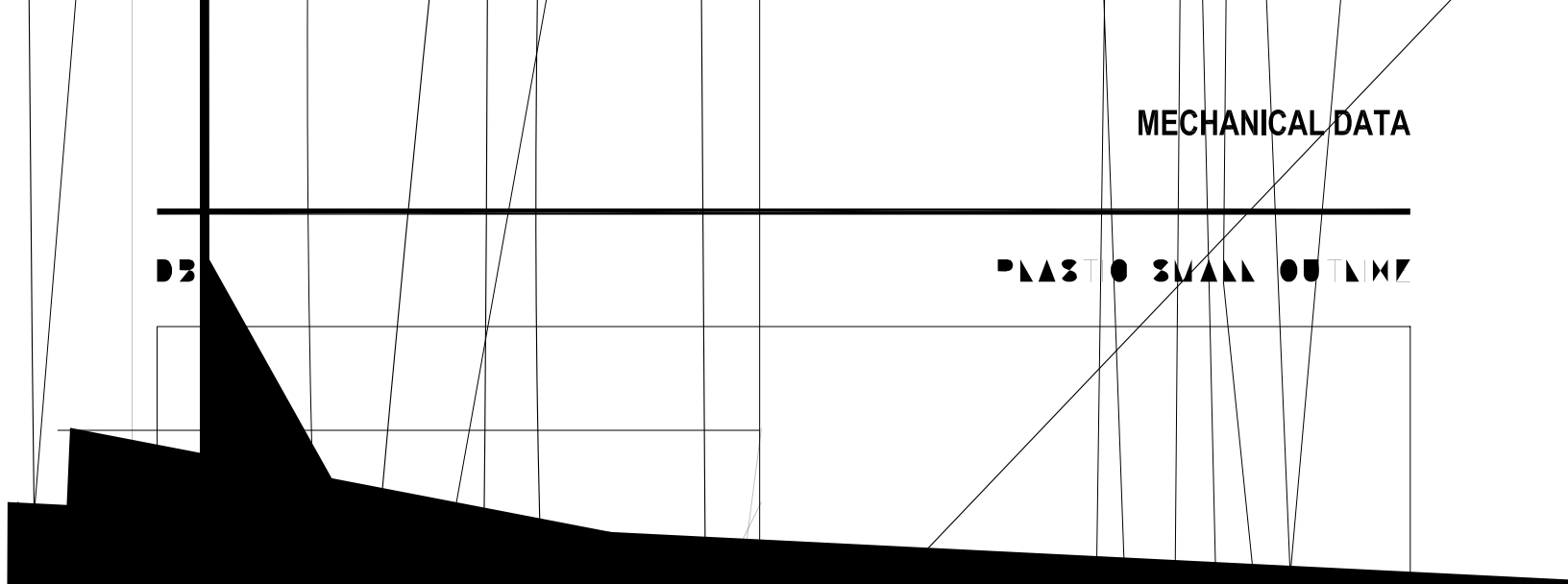


Figure 18. EEPROM Programming Flow Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ77908ADBT	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)					

D2 PLASTIC SMALL OUTLINE



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