

INTEGRATED PHOTO FLASH CHARGER AND IGBT DRIVER

FEATURES

- High Integrated Solution to Reduce Components
- Integrated Voltage Reference
- Integrated 50-V Power Switch
- Integrated Insulated Gated BiPolar Transistor (IGBT) Driver
- High Efficiency
- Programmable Peak Current, 0.9 A ~ 1.8 A
- Input Voltage of 1.6 V to 12 V
- Optimized Control Loop for Fast Charge Time
- Isolate IGBT VCC from VCC
- Output Voltage Feedback From Primary Side
- 16-pin QFN Package
- Protection
 - MAX On Time
 - MAX Off Time
 - Over Current Shutdown to Monitor VDS at SW Pin (OVDS)
 - Thermal Disable

APPLICATIONS

- Digital Still Cameras
- Optical Film Cameras

DESCRIPTION/ORDERING INFORMATION

This device offers a complete solution for charging photo flash capacitor from battery input, and subsequently discharging the capacitor to a xenon flash tube. This device has an integrated voltage reference, power switch, IGBT driver, and control logic blocks for charging applications and driving IGBT application. Compared with discrete solutions, this device reduces the component count, shrinks the solution size, and eases designs for xenon tube application. Additional advantages are a fast charging time and high efficiency from an optimized pulse width modulation (PWM) control algorithm.

Other provisions of the device includes sensing the output voltage from the primary side, programmable peak current, thermal shutdown, an output pin for charge completion, and input pins for charge enable and flash enable.

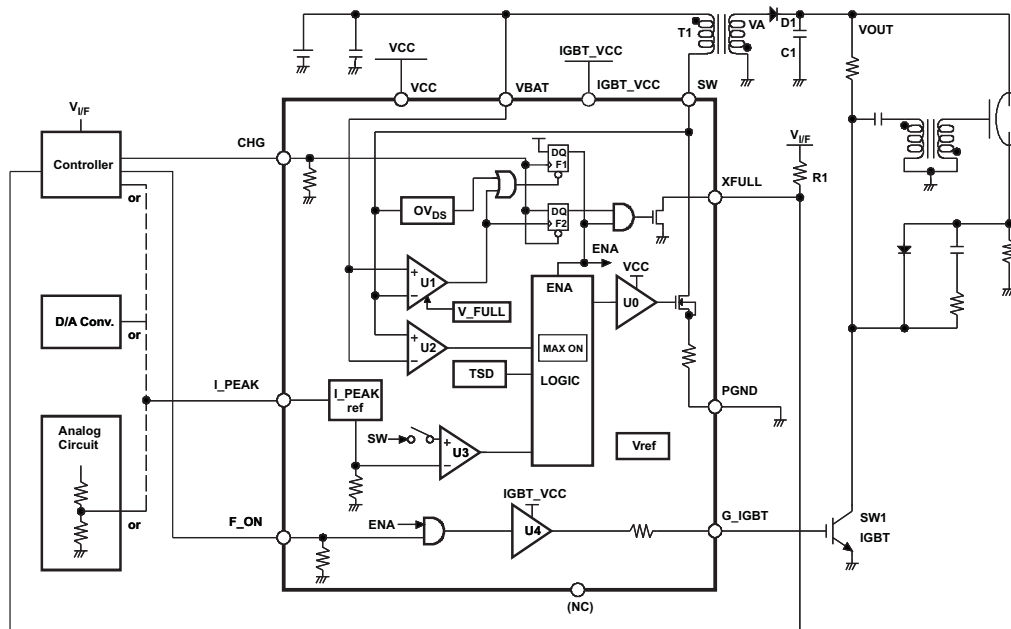


Figure 1. Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–35°C to 85°C	CAH	16-pin QFN	TPS65562RGT

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			UNIT
Supply voltage	VCC, IGBT_VCC	–0.6 to 6	V
	VBAT	–0.6 to 13	
V _{SW}	Switch terminal voltage	–0.6 to 50	V
I _{SW}	Switch current between SW and PGND	3	A
V _I	Input voltage of CHG, I_PEAK, F_ON	–0.3 to V _{CC}	V
T _{stg}	Storage temperature	–40 to 150	°C
T _J	Maximum junction temperature	125	°C
ESD rating	HBM (Human Body Model) JEDEC JES22-A114	1	kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage	VCC	2.7	4	V
	IGBT_VCC	2.7	5.5	
	VBAT	1.6	12	
V _{SW}	Switch terminal voltage	–0.3	45	V
I _{SW}	Switch current between SW and PGND		2	A
Operating free-air temperature range		–35	85	°C
V _{IH}	High-level digital input voltage at CHG and F_ON	2		V
V _{IL}	Low-level digital input voltage at CHG and F_ON		0.5	V

DISSIPATION RATINGS

PACKAGE	R _{θJA} ⁽¹⁾	POWER RATINGS T _A < 25°C	POWER RATINGS RATE T _A = 70°C	POWER RATINGS RATE T _A = 85°C
QFN	47.4°C/W	2.11 W	1.16 W	844 mW

(1) The thermal resistance, R_{θJA}, is based on a soldered PowerPAD™ package on 2S2P JEDEC board using thermal vias.

ELECTRICAL CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, $V_{BAT} = 4.2\text{ V}$, $V_{CC} = 3\text{ V}$, $I_{GBT_VCC} = 3\text{ V}$, $V_{(SW)} = 4.2\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ONL}	ON resistance of XFULL	$I_{XFULL} = -1\text{ mA}$		1.5	3	$k\Omega$
$V_{PKH}^{(1)}$	Upper threshold voltage of I_{PEAK}	$V_{CC} = 3\text{ V}$	2.4			V
$V_{PKL}^{(1)}$	Lower threshold voltage of I_{PEAK}	$V_{CC} = 3\text{ V}$			0.6	V
I_{CC1}	Supply current from VBAT	CHG = H, $V_{SW} = 0\text{ V}$ (free run by t_{MAX})		17	50	μA
I_{CC2}	Supply current from VCC	CHG = H, $V_{SW} = 0\text{ V}$ (free run by t_{MAX})		1.3	3	mA
I_{CC3}	Supply current from VCC and VBAT	CHG = L			1	μA
I_{LKG1}	Leakage current of SW terminal				2	μA
I_{LKG2}	Leakage current of XFULL terminal	$V_{XFULL} = 5\text{ V}$			1	μA
I_{sink}	Sink current at I_{PEAK}	$V_{I_PEAK} = 3\text{ V}$, CHG: High			2	μA
		$V_{I_PEAK} = 3\text{ V}$, CHG: Low			0.1	
R_{ONSW}	SW ON resistance between SW and PGND	$I_{SW} = 1\text{ A}$, $V_{CC} = 3\text{ V}$		0.4	0.9	Ω
R_{IGBT1}	G_IGBT pull up resistance	$V_{G_IGBT} = 0\text{ V}$, $I_{GBT_VCC} = 3\text{ V}$	8	12	19.4	Ω
R_{IGBT2}	G_IGBT pull down resistance	$V_{G_IGBT} = 3\text{ V}$, $I_{GBT_VCC} = 3\text{ V}$	36	53	70	Ω
I_{PEAK1}	Upper peak of ISW	$V_{I_PEAK} = 3\text{ V}$	1.58	1.68	1.78	A
I_{PEAK2}	Lower peak of ISW	$V_{I_PEAK} = 0\text{ V}$	0.7	0.8	0.9	A
V_{FULL}	Charge completion detect voltage at V(SW)	$V_{BAT} = 1.6\text{ V}$, $V_{CC} = 3\text{ V}$	28.0	28.7	29.4	V
		$V_{CC} = 3\text{ V}$	28.6	29.0	29.4	V
V_{ZERO}	Zero current detection at VSW		1	20	60	mV
$T_{SD}^{(1)}$	Thermal shutdown temperature		150	160	170	$^\circ\text{C}$
O_{VDS}	Over current detection at VSW		0.95	1.2	1.45	V
T_{MIX}	MAX OFF time		25	50	80	μs
T_{MAX}	MAX ON time		50	100	160	μs
R_{INPD}	Pull down resistance of CHG, F_ON	$V_{CHG} = V_{F_ON} = 4.2\text{ V}$		100		$k\Omega$

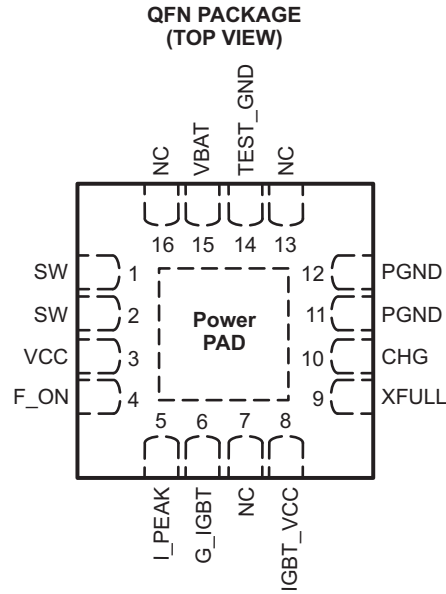
(1) Specified by design

SWITCHING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$, $V_{BAT} = 4.2\text{ V}$, $V_{CC} = 3\text{ V}$, $I_{GBT_VCC} = 3\text{ V}$, $V_{SW} = 4.2\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}^{(1)}$	Propagation delay	$F_ON \uparrow \downarrow$, $G_IGBT \uparrow \downarrow$		50		ns
		SW ON after VSW dips from V_{ZERO}		500		ns
		SW OFF after ISW exceeds I_{PEAK}		270		ns
		XFULL \downarrow after VSW exceeds V_{Full}		400		ns
		SW ON after CHG \uparrow		12		μs
		SW OFF after CHG \downarrow		20		ns

(1) Specified by design



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SW	1, 2	O	Primary side switch. Connect SW to the switched side of the transformer
VCC	3	I	Power supply input. Connect VCC to an input supply from 2.7 V to 4.0 V. Bypass VCC to GND with a 1 μ F ceramic capacitor as close as possible to the IC.
F_ON	4	I	G_IGBT control input. Drives F_ON with the flash discharge signal. A logic high on F_ON drives G_IGBT high when CHG is Low. See the <i>IGBT driver control</i> section for details.
I_PEAK	5	I	Primary side Peak current control input. The voltage at I_PEAK sets the peak current into SW. See the <i>Programming Peak Current</i> section for details on selecting V_{I_PEAK} .
G_IGBT	6	O	IGBT gate driver output. G_IGBT swings from PGND to VCC to drive external IGBT devices.
NC	7, 13, 16		No internal connection
IGBT_VCC	8	I	Power supply input for IGBT Driver output. Connect IGBT_VCC to an input supply from 2.7 V to 5.5 V.
XFULL	9	O	Charge completion indicator output. XFULL is an open-drain output that pulls low once the output is fully charged. XFULL is high impedance during charging and all fault conditions. XFULL is reset when CHG turns Low from High. See the <i>Indicating Charging status</i> section for details.
CHG	10	I	Charge control input. Drive CHG high to initiate charging of the output. Drive CHG low to terminate charging.
PGND	11, 12		Power ground. Connect to the ground plane.
TEST_GND	14		Used by TI, should be connected to PGND and ground plane.
VBAT	15	I	Battery voltage monitor input. Connect VBAT to an input supply from 1.6 V to 12 V. Bypass VBAT to GND with a 10 μ F ceramic capacitor (C1 in Figure 1 as close as possible to the battery) and a 1 μ F ceramic capacitor (C2 in Figure 1 , as close as possible to the IC). It is no problem to input VBAT before VCC input.

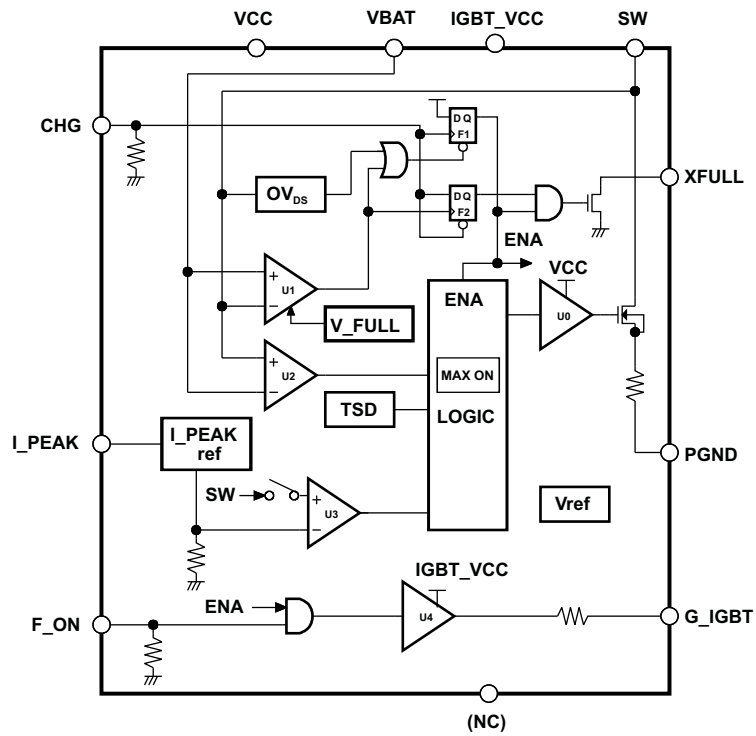


Figure 2. Block Diagram

I/O Equivalent Circuits

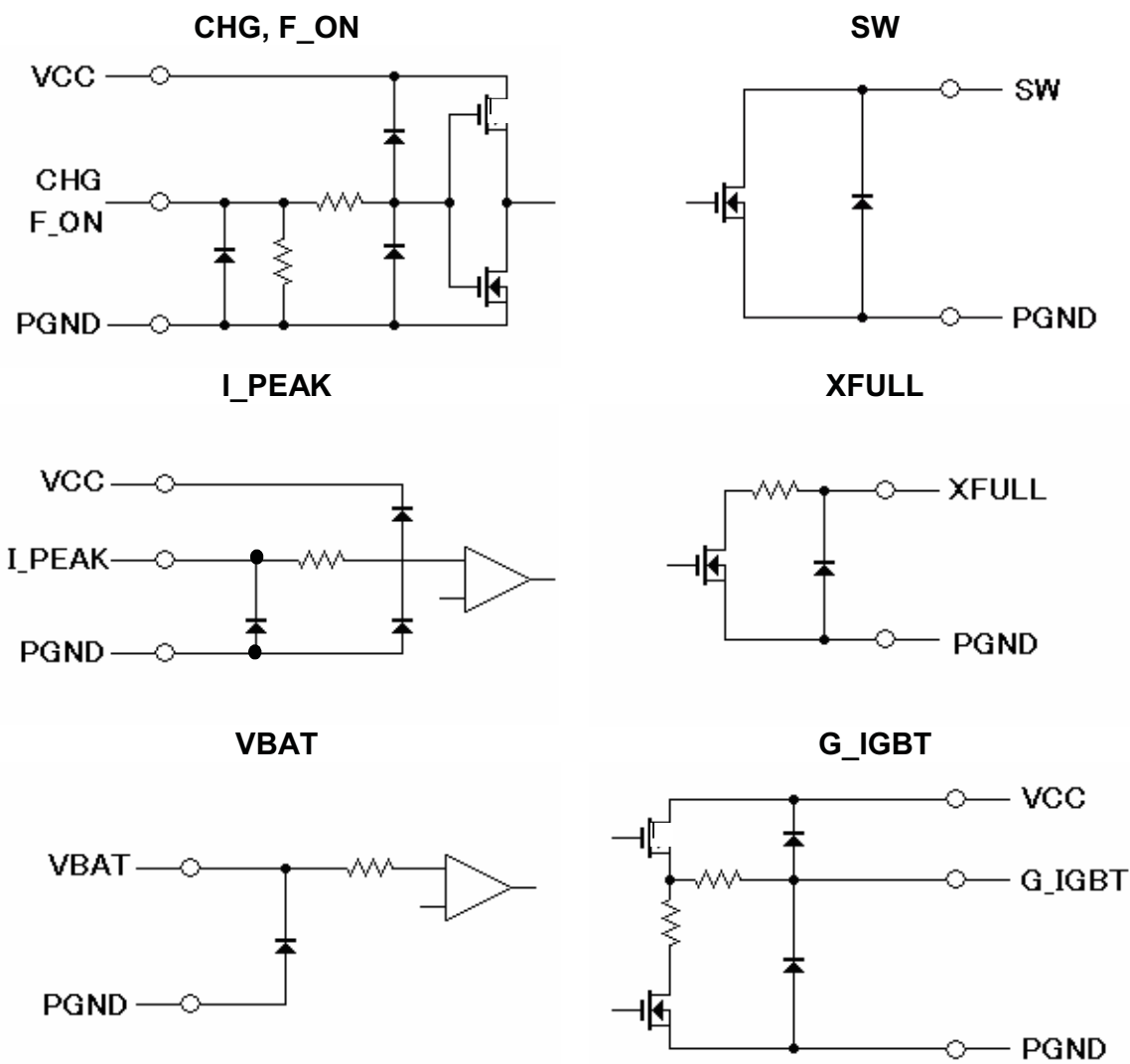


Figure 3. I/O Equivalent Circuits

PRINCIPLES OF OPERATION

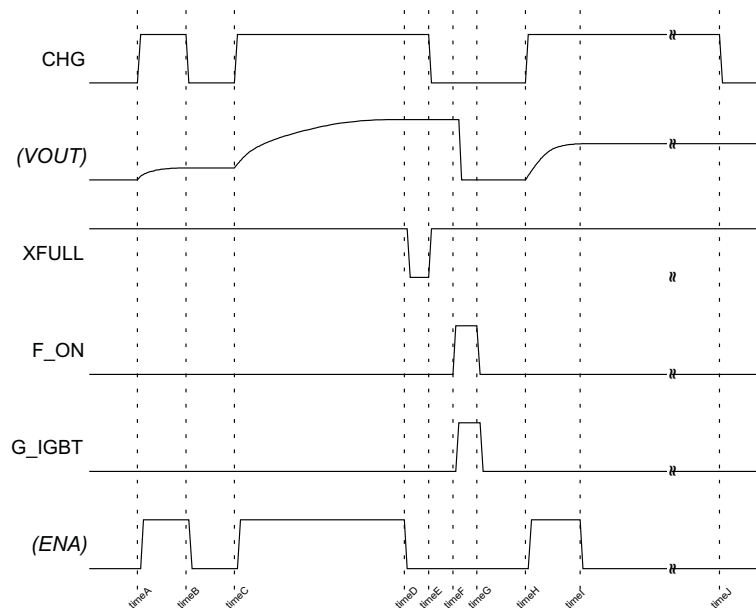


Figure 4. Whole Operation Sequence Chart

Start/Stop Charging

TPS65562 has one internal enable latch, F1, that holds the charge enable (ON/OFF status) of the device (see [Figure 4](#)).

The only way to start charging is to input $CHG\uparrow$ (see time A/C/H in [Figure 4](#)). Each time $CHG\uparrow$ is applied, the TPS65562 starts charging.

There are three trigger events to stop charging:

1. Forced stop by inputting $CHG = L$ from the controller (see timeB in [Figure 4](#)).
2. Automatic stop by detecting a full charge. $VOUT$ reaches the target value (see TimeD in [Figure 4](#)).
3. Protected stop by detecting an overcurrent function (OVDS) trigger at SW pin (see TimeI in [Figure 4](#)).

Indicate Charging Status

When the charging operation is complete, the TPS65562 drives the charge completion indicator pin, XFULL, to GND. A controller can detect the status of the device as a logic signal when connected through a pullup resistor, R1 (see [Figure 1](#)).

The XFULL output enables the controller to detect the OVDS protection status. If OVDS protection occurs, XFULL never goes L during $CHG = H$. Therefore, the controller detects OVDS protection by measuring the time from CHG high to XFULL low. If the time to XFULL low is longer than the maximum designed charge time, then an OVDS protection occurred.

The device starts charging at timeH, and OVDS protection occurs at TimeI (see [Figure 5](#)). At TimeI, XFULL stays H. At TimeJ, the controller detects OVDS protection through the expiration of a timer ends and then sets CHG to low to terminate the operation.

PRINCIPLES OF OPERATION (continued)

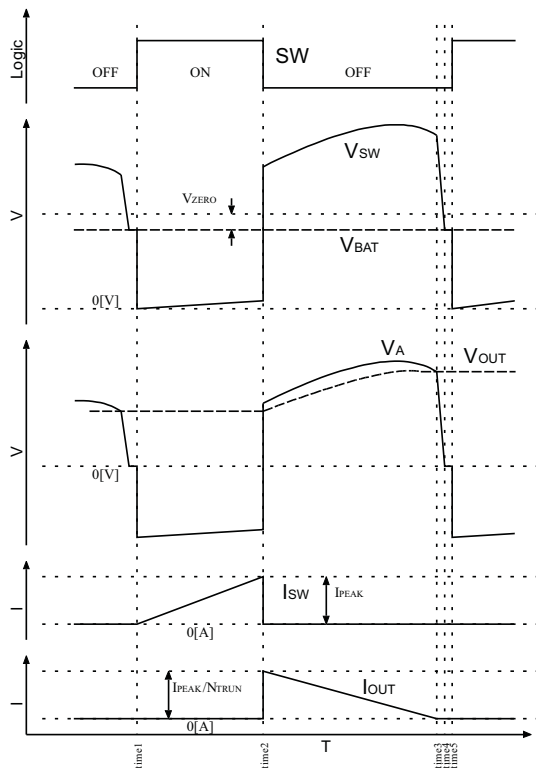


Figure 5. Timing Diagram at One Switching

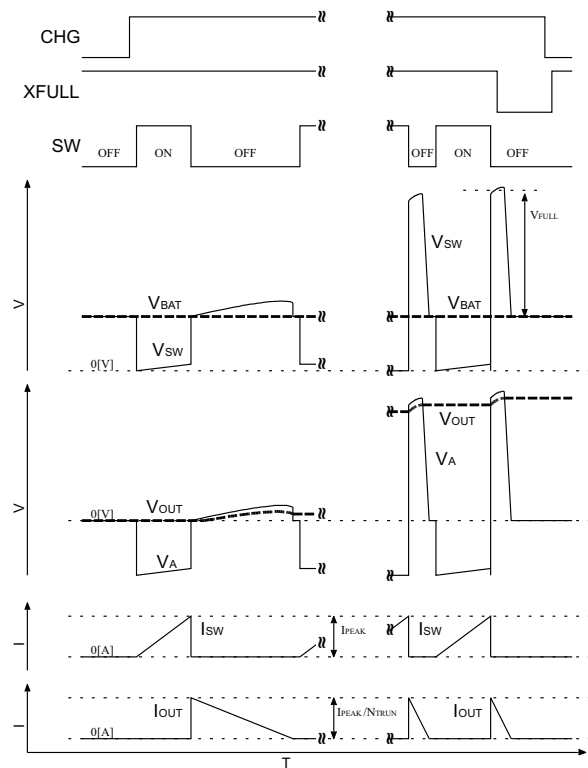


Figure 6. Timing Diagram at Beginning/Ending

Control Charging

The TPS65562 provides three comparators to control charging. Figure 2 shows the block diagram of TPS65562, and Figure 5 shows a timing diagram of one switch cycle. Note that emphasis is placed on Time1 and Time3 of the waveform in Figure 5.

While SW is ON (Time1 to Time2 in Figure 5), U3 monitors current flow through the integrated power switch from SW pin to GND. When I(SW) exceeds I(PEAK), SW turns OFF (Time2 in Figure 5).

When SW turns OFF (Time2 in Figure 5), the magnetic energy in the transformer starts discharging. Meanwhile, U2 monitors the kickback voltage at the SW terminal. As the energy is discharging, the kickback voltage is increasing according to the increase of VO (Time2 to Time3 in Figure 5). When almost all energy is discharged, the system cannot continue rectification via the diode, and the charging current of IO goes to zero (Times3 in Figure 5). After rectification stops, the small amount of energy left in the transformer is released via parasitic paths, and the kickback voltage reaches zero (Time3 to Time4 in Figure 5). During this period, U2 makes SW turn ON when (V(SW) - VBAT) dips from V(ZERO) (Time5 in Figure 5). In the actual circuit, the period between Time4 and Time5 in Figure 5 is small or does not appear dependent on the delay time of the U2 detection to SW ON.

U1 also monitors the kickback voltage. When (V(SW) - VBAT) exceeds V(FULL), the TPS65562 stops charging (see Figure 6).

In Figure 5 and Figure 6, ON time is always the same period in every switch cycle. The ON time is calculated by Equation 1. L and IPEAK are selected to ensure that tON does not exceed the MAX ON time (tMAX).

$$T_{ON} = L \frac{I_{PEAK}}{V_{BAT}} \tag{1}$$

The OFF time is dependant on output voltage. As the output voltage gets higher, the OFF time gets shorter (see Equation 2).

PRINCIPLES OF OPERATION (continued)

$$T_{\text{OFF}} = N_{\text{TURN}} \times L \frac{I_{\text{PEAK}}}{V_{\text{OUT}}} \quad (2)$$

Programming Peak Current

The TPS65562 provides a method to program the peak primary current with a voltage applied to the I_PEAK pin. Figure 7 shows how to program I_{PEAK}.

The I_PEAK input is treated as a logic input below V_{PKL} (0.6 V) and above V_{PKH} (2.4 V). Between V_{PKL} and V_{PKH}, I_PEAK input is treated as an analog input. Using this characteristic, I_{PEAK} can be set by a logic signal or by an analog input.

Typical usages of this function are:

1. Setting the peak charging currents based on the battery voltage. Larger I_{PEAK} for a fully charged battery and lower I_{PEAK} for a discharged battery.
2. Reducing I_{PEAK} when powering a zooming lens motor. This avoids inadvertent shutdowns due to large current from the battery.

In Figure 1, three optional connections to I_PEAK are shown.

1. Use the controller to treat I_PEAK as the logic input pin. This option is the easiest.
2. Use a D/A converter to force I_{PEAK} to follow analog information, such as battery voltage.
3. Use an analog circuit to achieve the same results as the D/A converter.

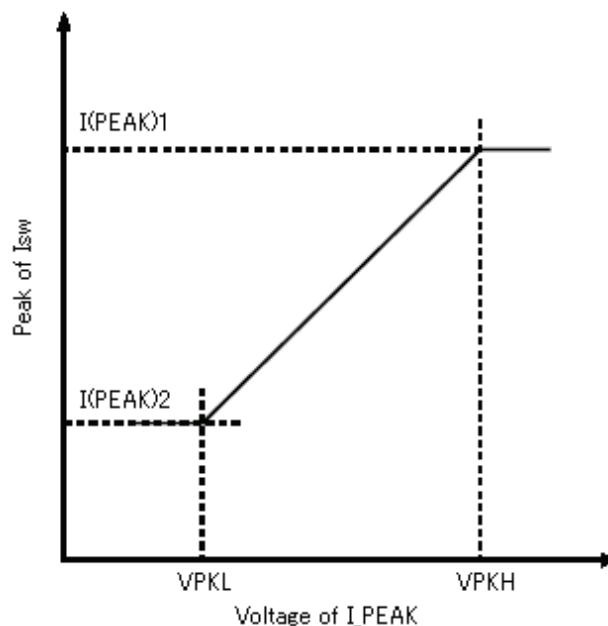


Figure 7. I_{PEAK} vs I_{sw}

IGBT Driver Control

The IGBT driver is provided by the TPS65562. The driver voltage depends on VCC. TPS65562 has a mask filter as shown in Figure 8. The mask does not have hysteresis; therefore, there is no wait time from CHG forcing Low after FULL CHARGE to F_ON turning High.

PRINCIPLES OF OPERATION (continued)

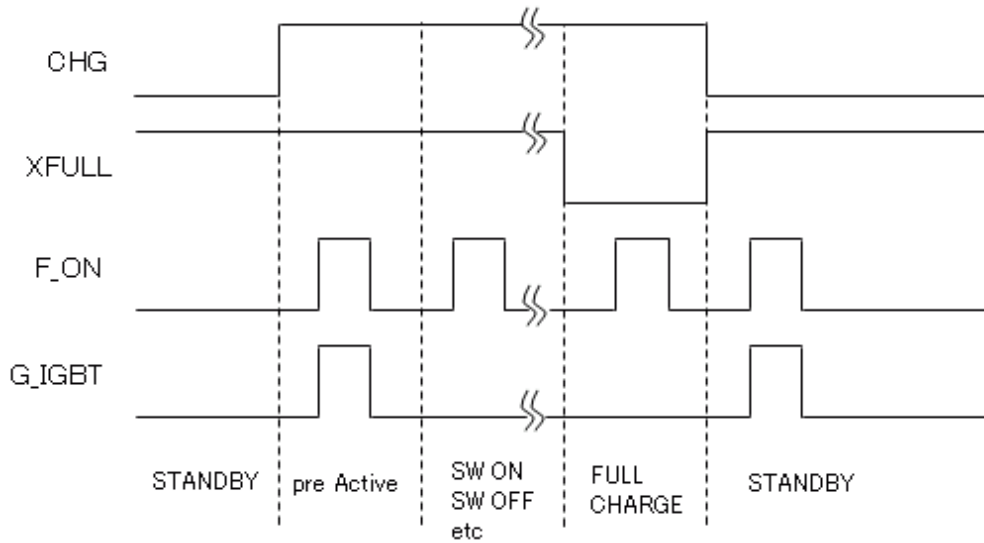


Figure 8. Relationships Between F_ON and CHG

Protections

TPS65562 provides four protection mechanisms: max on time, max off time, thermal disable, and over current shutdown.

MAX ON TIME

To prevent a condition such as pulling current from a poor power source (i.e., an almost empty battery), and never reaching peak current, the TPS65562 provides a maximum ON time function. If the ON time exceeds t_{MAX} , the TPS5562 is forced OFF regardless of I_{PEAK} detection.

MAX OFF TIME

To prevent a condition such as never increasing the voltage at the SW pin when the internal FET is OFF, the TPS65562 provides a maximum OFF time function. If the OFF time exceeds t_{MIN} , the TPS65562 is forced ON regardless of V_{ZERO} detection.

THERMAL DISABLE

Once the die temperature of the TPS65562, reaches 160°C, all functions stop. Once the die cools below 160°C, the TPS65562 restarts charging if CHG remains high during the entire over temperature condition.

OVER CURRENT SHUTDOWN

The TPS65562 provides an over voltage monitor function of the SW pin. The TPS65562 is latched off if the voltage on the SW pin is above OVDS during the switch ON time (see Figure 4 and its descriptions).

This function protects against short-circuits on the primary side of the transformer. A short-circuit of the primary side shorts the battery voltage to GND. SW pin can damage the device if not protected.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS65562RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-35 to 85	CAH	Samples
TPS65562RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-35 to 85	CAH	Samples
TPS65562RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-35 to 85	CAH	Samples
TPS65562RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-35 to 85	CAH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65562RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65562RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65562RGTR	QFN	RGT	16	3000	367.0	367.0	35.0
TPS65562RGTT	QFN	RGT	16	250	210.0	185.0	35.0

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203495/H 10/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGT (S-PVQFN-N16)

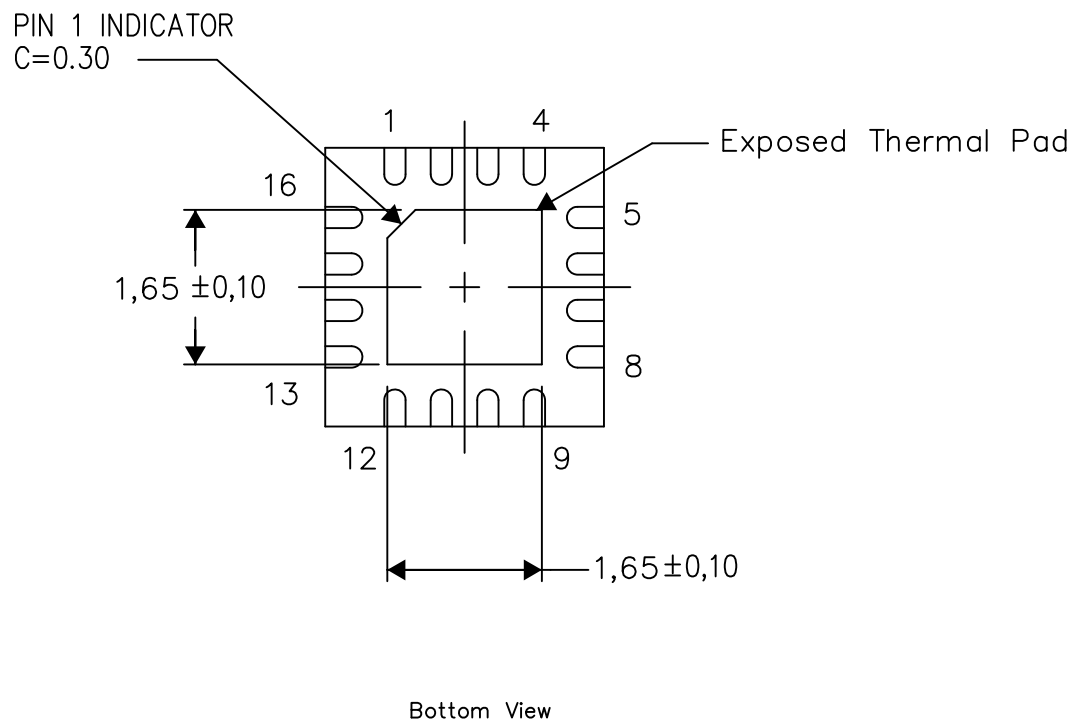
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



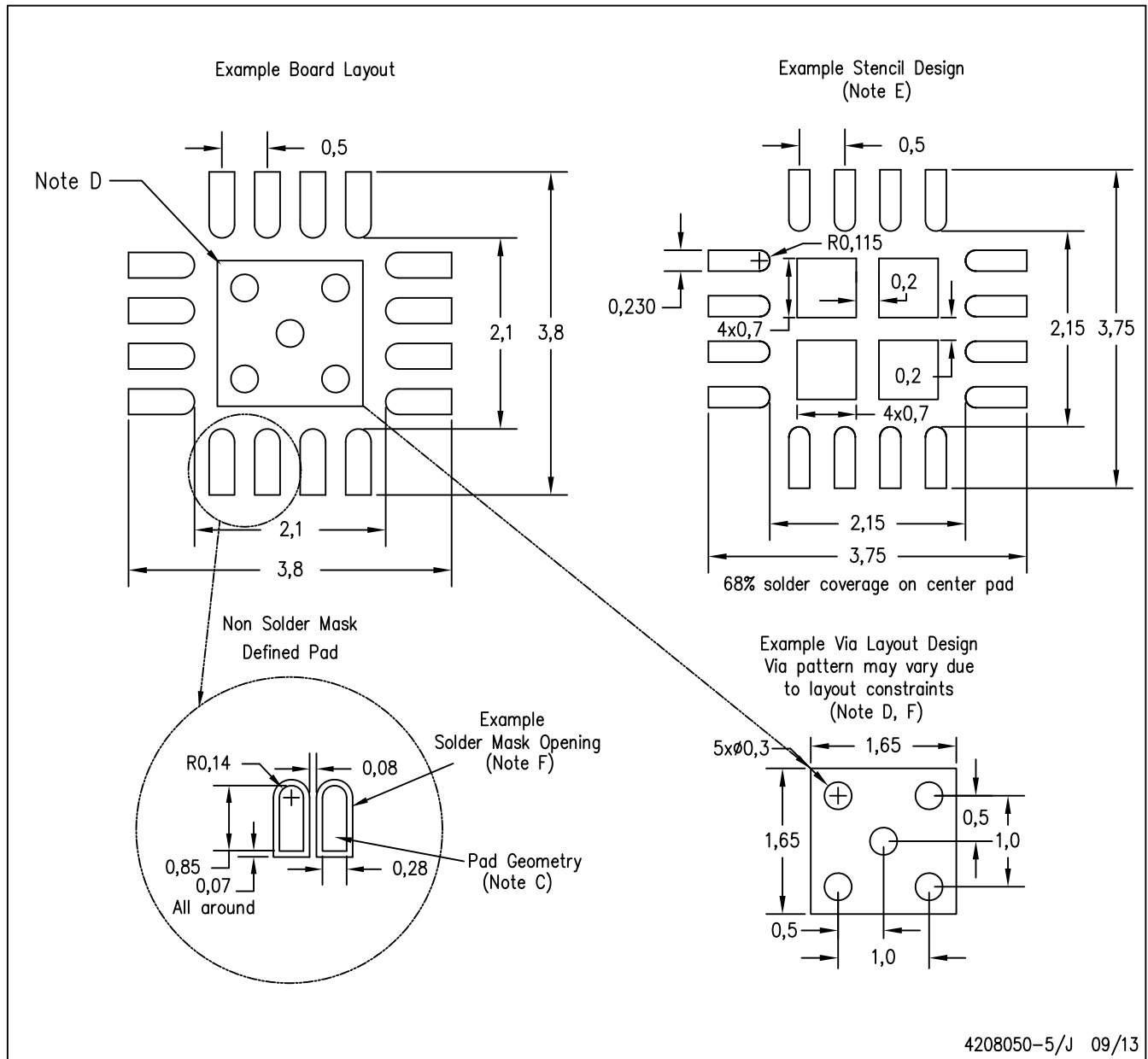
Exposed Thermal Pad Dimensions

4206349-7/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208050-5/J 09/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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