These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

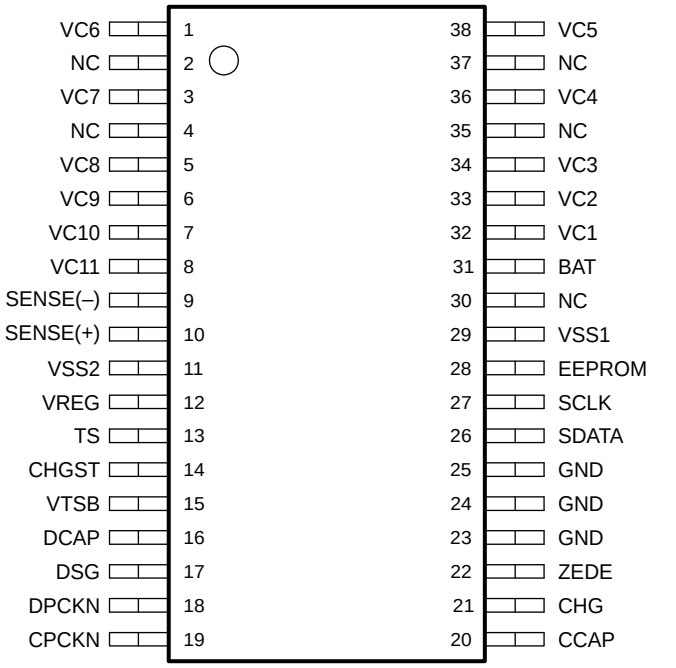
PIN DETAILS

PIN FUNCTIONS (38-Pin Package)

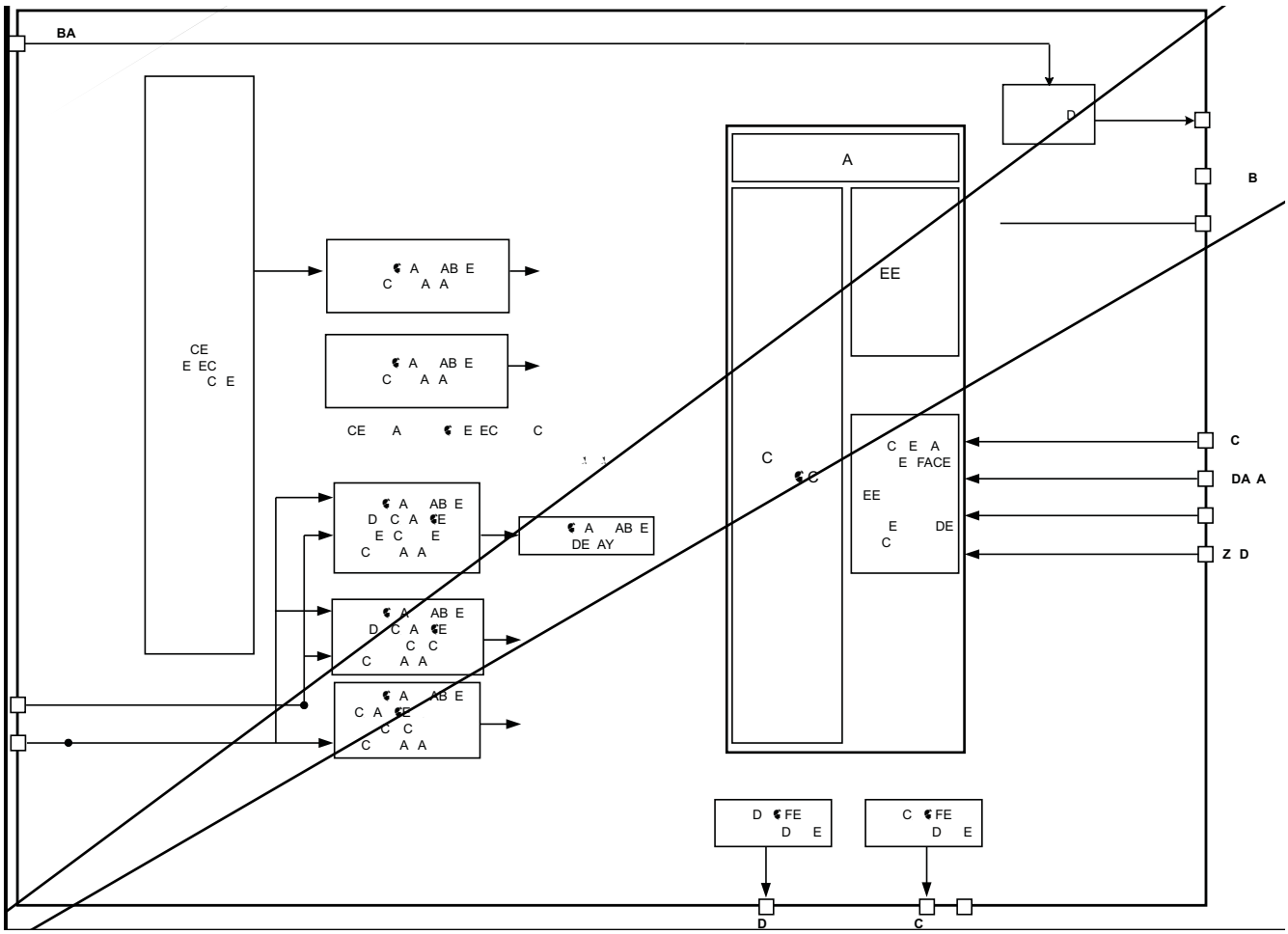
PIN		DESCRIPTION
NAME	NO.	
BAT	31	Power supply voltage, tied to highest cell(+)
CCAP	20	Energy storage capacitor for charge FET drive
CHG	21	Charge FET (n-channel) gate drive
CHGST	14	Charger-status input, used to detect charger connection/wakeup
CPCKN	19	Pack – charger negative terminal (charger return)
DCAP	16	Energy storage capacitor for discharge FET drive
DPCKN	18	Pack – discharge negative terminal (load return)
DSG	17	Discharge FET (n-channel) gate drive
EEPROM	28	EEPROM programming voltage input. Connect to VSS for normal operation.
GND	23, 24, 25	Logic ground (not for power return or analog reference). Tie to VSS.
NC	2, 4, 30, 35, 37	No connect (DO NOT CONNECT) externally. Failure to leave NC pins open can cause faulty operation.
SCLK	27	Serial-communication clock input used for EEPROM programming
SDATA	26	Serial-communication data input/output used for EEPROM programming (open-drain)
SENSE(+)	10	Current-sense input
SENSE(–)	9	Current-sense input
TS	13	Temperature sensing input
VC1	32	Sense-voltage input terminal for most-positive cell
VC2	33	Sense-voltage input terminal for second-most-positive cell
VC3	34	Sense-voltage input terminal for third-most-positive cell
VC4	36	Sense-voltage input terminal for fourth-most-positive cell
VC5	38	Sense-voltage input terminal for fifth-most-positive cell
VC6	1	Sense-voltage input terminal for sixth-most-positive cell
VC7	3	Sense-voltage input terminal for seventh-most-positive cell
VC8	5	Sense-voltage input terminal for eighth-most-positive cell
VC9	6	Sense-voltage input terminal for ninth-most-positive cell
VC10	7	Sense-voltage input terminal for tenthmost-positive (most-negative) cell
VC11	8	Most-negative cell(–) terminal (BAT–)
VREG	12	Integrated 3.3-V regulator output
VSS1	29	Analog ground (substrate reference)
VSS2	11	Analog ground (substrate reference)
VTSB	15	Thermistor bias supply (sourced from VREG)
ZEDE	22	*Zero Delay* test mode pin. Enables serial communications interface and minimizes protection delay times when connected to logic high. Connect to VSS for normal operation. A strong connection is recommended.

PIN DIAGRAM – bq77910 – 38-Pin SSOP DBT PACKAGE

DBT PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PACKAGING
bq77910DBT	TSSOP	50-piece tube
bq77910DBTR	TSSOP	2000-piece reel

THERMAL INFORMATION (continued)

THERMAL METRIC[1]		bq77910 DBT 38 PINS	UNIT
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[8]	N/A	°C/W

(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
Supply voltage		BAT[1]	5.6[2]		43.75[3]	V
V_I	Input voltage range	Cell differential, VCx to VC(x + 1), (x = 1 to 10)	1.4		4.375	V
		Cell input VCx, x = 1 – 10			(11 – x) × 4.375 V	
		Cell input VC11	–1		1	
V_{IH}	Logic-level input, high	SCLK, SDATA, EEPROM, ZEDE	0.8 × V_{REG}			V
V_{IL}	Logic-level input, low				0.2 × V_{REG}	V
VSENSE(+)	Voltage applied at SENSE(±) pins		VSS – 1		VSS + 1	V
VSENSE(–)			–0.2		BAT	V
R_{VCX}	Recommended VCx nominal input resistance		50	100	1000	Ω
I_{REG}	Regulator current				10	mA
I_{CB}	Cell balancing current				50	mA
C_{VCX}	Recommended VCx nominal input filter capacitance				1	µF
R_{CPCKN}, R_{DPCKN}	Recommended isolation-pin input resistance			100		Ω
R_{LDRM_DET}	Pulldown for load-removal detection			50		kΩ
C_{VREG}	External 3.3-V REG capacitor		1			µF
	EEPROM number of writes				3	times
T_{OPR}	Operating temperature	Meeting all specification limits	–25		85	°C
T_{FUNC}	Functional temperature	Operational but may be out of spec limits, no damage to part	–40		100	°C
C_{CCAP}, C_{DCAP}	External capacitance on CCAP and DCAP pins[4]		0.1	1		µF
R_P	Serial communication interface pullup resistance	SCLK, SDATA		2.2		kΩ

(1) The voltage rate of change at the BAT pin should be limited to a maximum of 1 V per µs in order to prevent unwanted device shutdown.
(2) Minimum voltage assumes 4-cell connection at 1.4 V/cell.
(3) Maximum voltage assumes 10-cell connection at 4.375 V/cell.
(4) C_{CCAP} and C_{DCAP} act as charge reservoirs for the CHG and DSG pins when driving large protection FETs. Minimum value is required for stability, independent of the CHG and DSG loading.

bq77910

ELECTRICAL CHARACTERISTICS (continued)

Vcell(n) = 1.4 to 4.375 for all cells, T_A = –25°C to 85ºC, BAT = 5.6 to 43.75 V; Typical values stated where T_A = 25°C and BAT = 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
TS TEMPERATURE SENSING							
$r_{DS(on)}$	VTSB pin pullup resistance	I_{OUT} = –1 mA at VTSB pin, $r_{DS(on)} = (V_{REG} – V_{VTSB}) / 1$ mA			50	150	Ω
	TS pin fault-signal pulldown resistance	OV_TS_CTRL = 1, Vcell > Vov			50	150	
I_{TS_PD}	TS pin thermistor check pulldown current	TS = 3.3 V (externally driven)		1	2	4	µA
t_{THERM_CHECK}	Thermistor fault sampling interval				4		s
$V_{EXT\_BIAS\_DET}$	Thermistor external-bias supply-detection threshold	Internal VTSB supply off		13	15	17	%VREG
V_{HOT}	Overtemperature-detection threshold (ratiometric to VTSB)	Internal VTSB supply on, no external bias		17		21	%VREG
V_{TH_SHORT}	Thermistor short-detection trip threshold (ratiometric to VTSB)	Internal VTSB supply on, no external bias		1		10	%VREG
V_{TH_HYST}	TS comparator hysteresis	Hysteresis for short, open, and overtemperature comparators		3		8	%VREG
V_{TH_OPEN}	Thermistor open detection (ratiometric to VTSB)	Internal VTSB supply on, no external bias		90		98	%VREG
CELL BALANCE							
R_{BAL}	Cell-balance internal resistance[7]	$r_{DS(on)}$ for internal FET switch, T_A = 0°C to 50°C	$V_{CELL} = CBV_{MAX}$ = 3.9	–50%	10	50%	Ω
			$V_{CELL} = CBV_{MAX}$ = 3.2	–50%	20	50%	
			$V_{CELL} = CBV_{MAX}$ = 2.5	–50%	30	50%	
$t_{CELL\_BAL\_CHECK}$	Cell balancing update interval				7.5		min
OPEN CELL CONNECTION							
$I_{LOAD\_OPEN\_CELL}$[8]	Cell loading during open-cell detect			75		450	µA
$t_{OPEN\_CELL\_CHECK}$	Open-cell fault-sampling interval **(N = total number of cells in pack)**				4 × N		s
R_{OPEN_CELL}	Minimum impedance from cell terminal to VCx input that is interpreted as an open condition					100	kΩ
BATTERY-PROTECTION-THRESHOLD TOLERANCES[9]							
ΔV_{OV}	OV detection threshold accuracy for V_{OV} = 4.2 V [10]	T_A = 0°C to 50°C		–25		25	mV
		T_A = –25°C to 85°C		–50		50	
	OV detection threshold accuracy for V_{OV} = 3.2 V [10]	T_A = 0°C to 50°C		–50		50	
		T_A = –25°C to 85°C		–75		75	
ΔV_{UV}	UV detection threshold accuracy	T_A = –25°C to 85°C		–100		100	mV
ΔV_{SCD} ΔV_{OCD}	OCC/SCD detection threshold accuracy	T_A = –25°C to 85°C		–20%		20%	
ΔV_{SCC}	SCC detection threshold accuracy	V_{SCC} from 10 mV to 15 mV		–3		3	mV
		V_{SCC} > 15 mV		–20%		20%	
BATTERY PROTECTION DELAY-TIME TOLERANCES[9]							
Δt_{OV}	OV detection delay time accuracy	Default EEPROM setting		–15%		15%	
Δt_{UV}	UV detection delay time accuracy			–15%		15%	
Δt_{SCD}	OCD/SCD detection delay time accuracy	t_{SCD} Max		–15%		15%	
Δt_{SCC}	SCD detection delay time accuracy			–15%		15%	

(7) Balance current is not internally limited. External series resistance must be used to ensure balance current is below *50 mA maximum* to limit IC internal power dissipation.

(8) This current is sufficient to detect an open-cell condition down to 100 kΩ

ELECTRICAL CHARACTERISTICS (continued)

Vcell(n) = 1.4 to 4.375 for all cells, T_A = –25°C to 85ºC, BAT = 5.6 to 43.75 V; Typical values stated where T_A = 25°C and BAT = 36 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGER DETECTION[11]						
V_{CHG_DET1}	Voltage at CHGST pin, referenced to VSS, to determine charger present (charger insertion detected when voltage at CHGST pin > V_{CHG_DET1})	5.6 V < BAT < 43.75 V	0.3	0.65	0.85	V
LOAD REMOVAL DETECTION						
V_{OPEN_LOAD}	Voltage at DPCKN, referenced to VSS, with DSG FET *disabled* to detect load removal (load removal detected when voltage at DPCKN < V_{OPEN_LOAD})	5.6 V < BAT < 43.75 V	1.5	2	2.5	V
R_{DSG_GND}	Internal resistance between DPCKN and VSS	5.6 V < BAT < 43.75 V	1000	1500	3000	kΩ
EEPROM LIFETIME						
T_{DR}	Data retention	5.6 V < BAT < 43.75 V	10			years

(11) Alternate charger detection options are available using the CPCKN pin. Contact TI for additional configuration versions.

SERIAL COMMUNICATION INTERFACE (for Configuration Only)

BAT = 5.6 V to 43.75 V, T_A = –25°C to 85°C

PARAMETER		MIN	MAX	UNIT
t_r	SCLK, SDATA rise time		1000	ns
t_f	SCLK, SDATA fall time		300	ns
$t_{w(H)}$	SCLK pulse duration, high	8		µs
$t_{w(L)}$	SCLK pulse duration, low	10		µs
$t_{su(STA)}$	Setup time for START condition	9.4		µs
$t_{h(STA)}$	START condition hold time after which first clock pulse is generated	8		µs
$t_{su(DAT)}$	Data setup time	250		ns
$t_{h(DAT)}$	Data hold time	0		µs
$t_{su(STOP)}$	Setup time for STOP condition	8		µs
$t_{su(BUF)}$	Time the bus must be free before new transmission can start	9.4		µs
t_V	Clock low to data out valid		900	ns
$t_{h(CH)}$	Data out hold time after clock low	0		ns
f_{SCL}	Clock frequency	0	50	kHz

GENERAL OPERATIONAL OVERVIEW

POWER MODES

The bq77910 has the following power modes: active and shutdown (LDO disabled). The following table outlines the operational functions in the different power modes.

POWER MODE	MODE DESCRIPTION
Active	The IC is operating with internal LDO enabled and battery monitoring functions available and operating. The active power

PROGRAMMABLE PROTECTION FUNCTIONS

The bq77910 provides the following types of protection functions:

- Cell overvoltage
- Cell undervoltage
- Discharge overcurrent
- Discharge-current short circuit
- Charge-current short circuit

All of the voltage/current and time-delay thresholds can be adjusted for a specific application by programming the EEPROM settings of the IC. The ranges available are shown in Table 1.

CAUTION

Only a maximum of three EEPROM write cycles per byte should performed to ensure long-term data retention stability. (For circuit development purposes, the EEPROM may be rewritten many times.)

Table 1. Detection Voltage, Detection Delay Time Summary

PARAMETER		RANGE (EEPROM Selected)	MIN	MAX	STEP
Overvoltage	Cell voltage		2.8 V	4.375 V	25 mV
	Delay		0.5 s	2.25 s	0.25 s
	Hysteresis		0 mV	300 mV	25 mV or 50 mV
Undervoltage	Cell voltage		1.4 V	2.9 V	100 mV
	Delay		500 ms	32 s	Binary spacing
	Hysteresis		400 mV	1600 mV	400 mV
Discharge overcurrent	SENSE(–) pin voltage with respect to SENSE(+)	Low	25 mV	100 mV	5 mV
		High	125 mV	500 mV	25 mV
	Delay		20 ms	300 ms	20 ms
			400 ms	2000 ms	100 ms
Discharge short circuit	SENSE(–) pin voltage with respect to SENSE(+)	Low	40 mV	190 mV	10 mV
		High	200 mV	950 mV	50 mV
	Delay	Fast	60 µs	960 µs	60 µs
		Slow	50 ms	1500 ms	50 ms or 100 ms
Charge short circuit	SENSE(–) pin voltage with respect to SENSE(+)	Low	–10 mV	–85 mV	5 mV
		High	–50 mV	–425 mV	25 mV
	Delay		60 µs	960 µs	60 µs

Cell Overvoltage Detection and Recovery

The CHG FET is turned off if any one of the cell voltages remains higher than V_{OV} for a period greater than t_{OV}. As a result, the cells are protected from an overcharge condition. After an overvoltage event occurs, the all cells must relax to less than ($V_{OV} – V_{HYST}$) to allow recovery.

The V_{OV}, t_{OV}, and V_{HYST} values can be set via the EEPROM bits OVT, OVD, and OVH.

Cell Undervoltage Detection and Recovery

When any one of the cell voltages falls below V_{UV}, for a period of t_{UV}, the bq77910 enters the undervoltage protection state. The DSG FET is turned off, and depending on configuration, the device could enter the SHUTDOWN mode. Both

If UV_REC = 0, the DSG FET is re-enabled when **all** the cell voltages increase back above the V_{UV} threshold level plus the hysteresis value; there is no time-delay part of the recovery. In this case, when UV_REC = 0 and under high load currents, the Vcell voltages could recover to >UV + hyst very quickly, re-enabling the FETs and allowing the high load current to persist. Care should be taken when using this UV_REC = 0 mode, as the power MOSFETs could oscillate rapidly.

CAUTION

Care should be taken to properly set overcurrent and cell undervoltage trip thresholds, because it is possible that a fully charged pack with a continuous high discharge load can oscillate in and out of the undervoltage condition. This may result in overheating of the cells or protection MOSFETs due to the potentially high-duty-cycle operation.

If UV_REC = 1, the DSG FET is re-enabled when **all** the cell voltages increase back above the V_{UV} threshold level plus the hysteresis value **AND** the load is removed.

Current is interrupted by opening the FETs, and at this point the cell voltages may quickly recover above the UV + hyst levels if the battery pack is not completely depleted. However, the external load may remain attached. When the external load is removed, the IC detects load removal and reconnects the DSG FET.

If UV_REC_DLY = 1 and any cell remains below the VUV threshold level plus the hysteresis for longer than 8 seconds, the device enters SHUTDOWN mode. If UV_REC_DLY = 0, the device does **not** enter the SHUTDOWN mode from the cell undervoltage fault condition.

The LDO is turned off during the SHUTDOWN mode. Insertion into a charger is required to recover from the SHUTDOWN mode.

Charger detection methods are discussed in later sections, such as *Application Information*.

Overcurrent in Discharge (OCD) Detection

The OCD detection feature senses an overload current by measuring the voltage across the sense resistor. When an overload condition is detected, both of the power FETS are disabled to prevent damage to the cells and FET components. Criteria for fault recovery depend on the state of the SOR (EEPROM bit). Overcurrent trip level (V_{OCD}) and blanking time delay (t_{OCD}) are programmable via EEPROM bits OCDT and OCDD to match individual application requirements.

Short Circuit in Discharge (SCD) Detection

The SCD detection function senses severe discharge current by measuring the voltage across the sense resistor. When a short circuit is detected, both of the power FETs are disabled to prevent damage to the cells and FET components. Criteria for fault recovery depend on the state of the of the SOR (EEPROM bit). Short-circuit trip level (V_{SCD}) and blanking time delay (t_{SCD}) are programmable via EEPROM bits SCDT and SCDD to match individual application requirements.

Load Removal Detection/OCD and SCD Fault Recovery

The part includes an internal high-impedance connection between the DPCKN and VSS pins of approximately 1.5 MΩ . An external load (for example power tool motor winding), if still connected to the pack terminals, would present a very low impedance relative to the high internal pulldown resistance.

NOTE

If the external load presents additional capacitance, then an external pulldown may be required between the DPCKN and VSS pins. This extra pulldown does not increase battery load current when the external load is removed.

If the DSG power FET is disabled after an overload or short-circuit event, the voltage at the DPCKN is

approximately equivalent to the BAT voltage potential while an external load (e.g., power tool motor) is present at the pack terminals. When the external load is removed, the high-value internal resistance pulls down the DPCKN potential to the internal VSS level. An internal comparator monitors the DPCKN terminal voltage during the protection state. When the DPCKN voltage falls to < V_{OPEN_LOAD} (approximately 2 V), the load removal is detected. Fault recovery from an OCD or SCD event depends on the state of the SOR EEPROM bit.

If SOR = 0, the FETs are re-enabled only after the external load removal is detected.

If SOR = 1, the FETs are re-enabled after the load is removed **and** a charger insertion is detected.

(Details of charger presence detection methods are discussed in later sections.)

Short Circuit in Charge (SCC) Detection

The SCC detection function senses severe charge current by measuring the voltage across the sense resistor. In this case, the voltage is negative (opposite polarity of OCD and SCD detection). When a short circuit is detected, both of the power FETS are disabled to prevent damage to the cells and FET components. Short-circuit trip level (V_{SCD}) and blanking time delay (t_{SCD}) are programmable via EEPROM bits SCCT and SCCD to match individual application requirements.

NOTE

The current sensing element must be located along a common charge and discharge path in order to protect against both charge and discharge current faults. This is particularly important to note for parallel FET configurations or configurations that combine the FET with the sense element.

Short Circuit in Charge Recovery

An SCC fault is cleared after charger removal is detected. (See later sections for details of charger insertion and removal detection methods).

FIXED HARDWARE FAULT-PROTECTION FUNCTIONS

The bq77910 provides a number of fixed protection settings for hardware faults as listed:

- Open cell connection
- Pack voltage *Brownout* condition – power FET protection
- Charger-enable temperature range
- Open thermistor connection
- Shorted thermistor connection
- Overtemperature protection

Open Cell Connection

A mechanical or assembly fault in the pack can cause a high-impedance or broken connection between the IC cell sense pins and the actual cells. During operation, the bq77910 periodically checks the validity of the individual cell voltage reading by applying a micropower pulsed load across each cell. If the connection between the pin and the cell is opened, the apparent cell voltage will collapse and a fault (permanent failure) condition is detected. The open cell detection reading is taken at a time interval of $t_{OPEN\_CELL\_CHECK}$, as specified in the parametric tables. Recommended external filter-capacitor maximum value is also listed in the *Recommended Operating Conditions*. Because an open-cell fault may be considered as a permanent failure, the fault detection logic must detect two consecutive open-cell conditions prior to activating the protection condition for an open-cell fault. Due to the nature of open-cell fault conditions, other *apparent* faults may be observed during an open-cell condition.

Summary of open-cell detection-logic operation:

- For an N-cell battery pack, the bq77910 always protects (by opening the FETs) in some manner within the 2 × N × $t_{OPEN\_CELL\_CHECK}$ time frame (sampling interval is $t_{OPEN\_CELL\_CHECK}$, and two successive open cell faults are required to avoid nuisance tripping).

- Because an open cell connection results in a floating VCx input, a UV or an OV fault may be detected before the open-cell fault due to their shorter fault filter times. Furthermore, the OV or UV condition may not be stable and the fault may recover during the open-cell check interval (i.e., the FETs may toggle). In all cases the open-cell fault is detected within the open-cell fault filter time and the FETs are shut off until the recovery conditions are satisfied. .
- The LDO shuts down following the detection of an open-cell fault, provided that a charger is not detected. When the pack is awakened following this, the open-cell fault is initially cleared (FETs closed) and must be re-evaluated over the filter time before the fault is again registered. Charger detection inhibits LDO shutdown; however, once the charger is disconnected, the LDO then shuts down, provided that the recovery conditions have not yet been satisfied.

Additional Fault Protection Functions

The brownout protection functionality is discussed in the *IC Internal Power Control* section of this document. Thermistor fault detection, charger/thermistor interface and control are discussed in the *Application Information* section.

IC INTERNAL POWER CONTROL

Power-On Reset/UVLO

On initial application of power to the BAT pin, the IC internal power supply rail begins to ramp up. The IC contains an internal undervoltage lockout (UVLO)/power-on reset (POR) circuit that prevents operation until the BAT voltage is sufficient to ensure predictable start-up and operation. All power for the IC internal circuitry is derived from the BAT pin. The UVLO/POR start-up threshold is specified in the parametric table as $V_{STARTUP}$. Once the BAT voltage has exceeded this level, the internal LDO regulator and control circuitry are enabled and continue to operate even if BAT falls below VSTARTUP. If the BAT pin falls below the operational range given under *Recommended Operating Conditions*, the device powers down.

On initial power up, the state of the output MOSFET drive pins (CHG and DSG) is indeterminate until the voltage on BAT reaches the $V_{STARTUP}$ threshold. No load should be applied during this period.

BAT Holdup/Brownout Protection Functionality

The BAT pin is used to power the IC internal circuitry, and should be supplied through a diode and held up with a capacitor(1) placed near the IC as shown in the application diagrams (see Figure 2 CELL BALANCING FUNCTION). The external diode prevents discharge of the IC power rail during external transients on the PACK(+) node.

This allows the bq77910 to maintain proper control of the pack and system during brownout conditions.

Brownout is defined as a situation during which the stack voltage collapses to a voltage below the minimum operating voltage of the IC (~5.6 V) for a short duration (~1 s). A typical application case is shown below. Additional examples are provided in the *Application Information* section later in this document.

If there are short-duration sags in the PACK(+) voltage (typically due to high load transients), the operating current for the IC is momentarily provided by the external capacitor. Assuming that there is no external load on the VREG (LDO output) pin, the IC draws approximately 50-µA average current from the capacitor. The holdup time before the IC goes into shutdown mode depends on the initial pack voltage. For a normal *low battery* initial condition using a 4-cell stack, the cells may be in the range of 3 V/cell or 12 V total for the pack voltage. If a load transient occurs at this point, and the pack voltage sags down to below the IC POR threshold, the voltage at the BAT pin is held above 5 V for slightly greater than one second using a 10-µF capacitor.

Waveforms typical of a load transient during low pack voltage conditions are shown as follows. In the first load transient, the PACK(+) rail momentarily collapses but the load is disconnected before the holdup time limit is exceeded. In the second load transient, the load is left on for a duration exceeding the holdup capability, so when the IC operating voltage reaches the gate-drive undervoltage limit, the external power FETs are disabled to disconnect the load.

(1) The capacitor should be sized according to the application requirements. A typical value would be 10 µF.

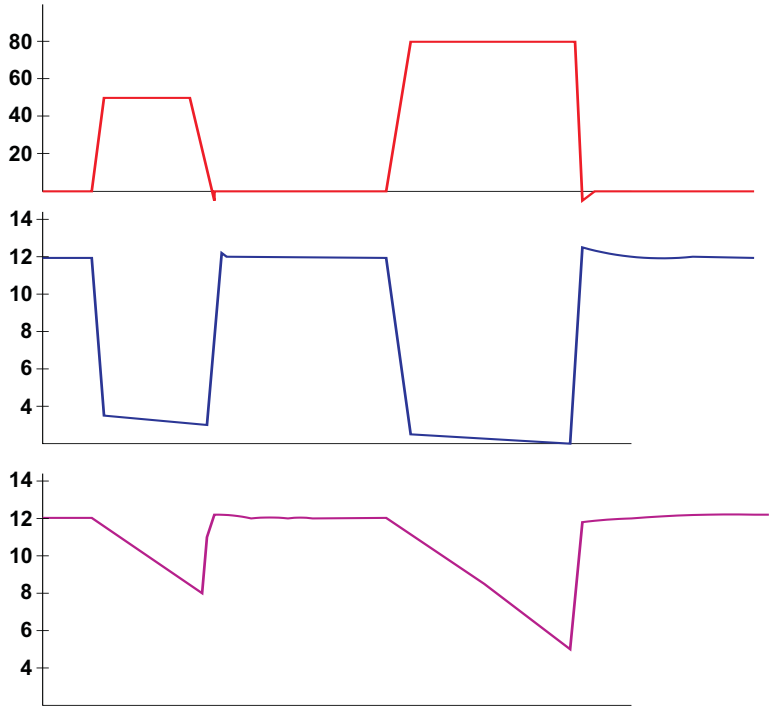


Figure 1. Load Transient Examples

BAT

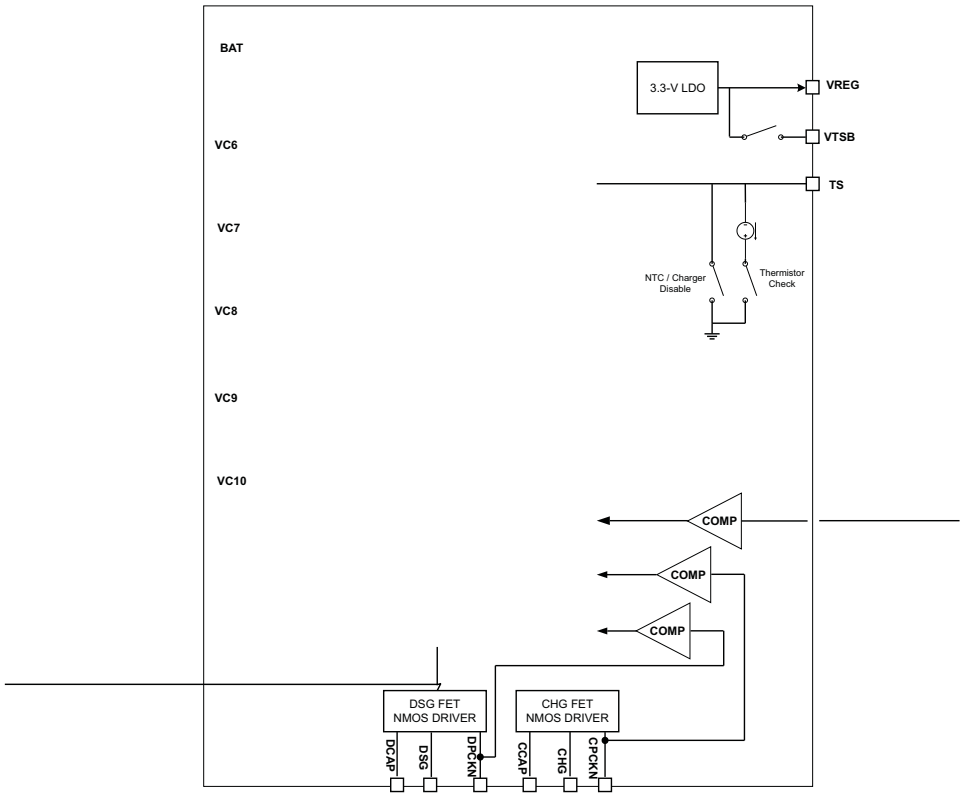


Figure 2. Example 5-Cell, Series FET Configuration Schematic Using bq77910

Waveforms illustrative of load transients during high pack voltage conditions are shown here.

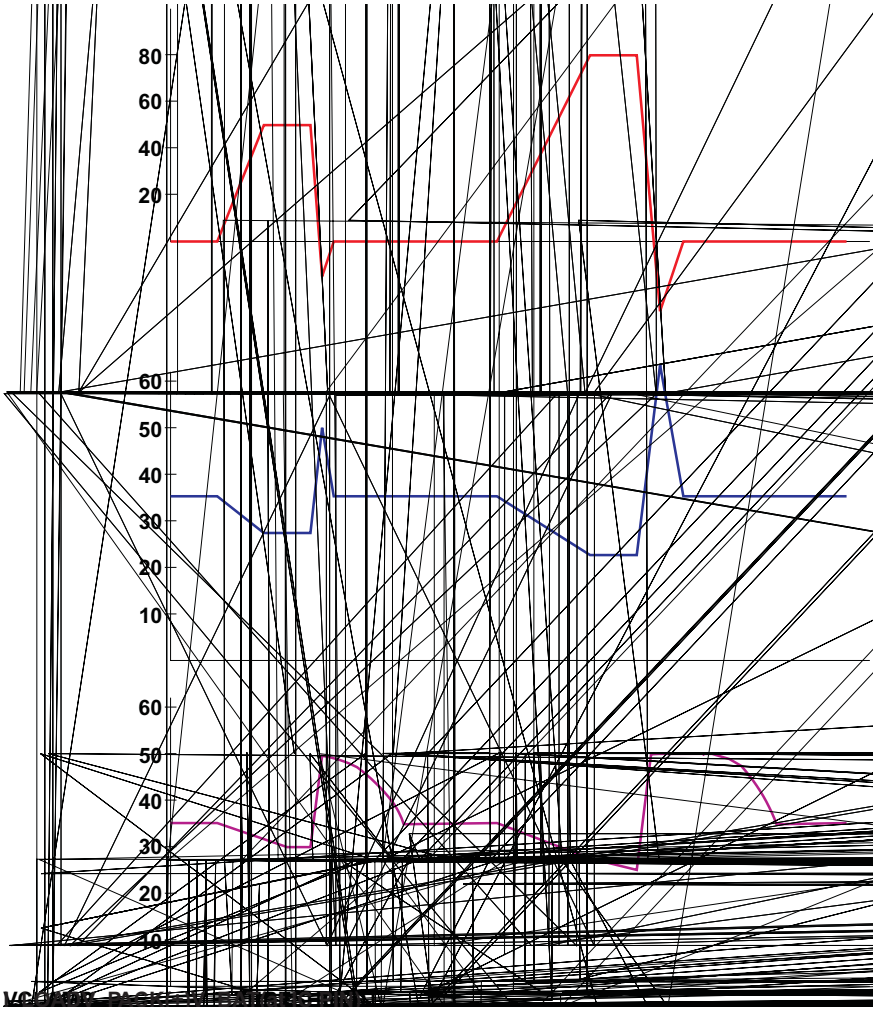


Figure 3. High-Voltage Load-Transient Waveforms

FET Gate Drive Control

As noted in the previous section, the BAT voltage at the IC pin is held up slightly longer than the external PACK(+) voltage using the external diode/capacitor to feed the BAT rail. Thus, if the BAT pin voltage at the IC sags, the external voltage sag will have exceeded the holdup time, and the IC is no longer able to operate for an extended period of time. At this point, the DSG and CHG gate drive outputs are actively driven low. The FET driver stages use two additional external capacitors (connected at the CCAP and DCAP pins) to maintain a local power reservoir dedicated to the gate drive circuitry, as the system (BAT) voltage may be collapsing during the time that the FETs are being turned off. The FETs are turned off when the voltage at the CCAP and/or DCAP pins falls below V_{GATE_UV}.

By turning off the FETs quickly, the system avoids the condition of insufficient gate drive due to low battery voltage. (If the FET gate drive is not high enough, the power components may not be in their linear operating region, and could overheat due to resistive losses at high load currents).

In the case of a system undervoltage condition, both FETs are disabled within 500 µs maximum; in all cases the FET fall time is less than fall time specified in the *Electrical Characteristics* section (FET Drive). During initial power up, once the UVLO threshold has been reached and the IC powers up fully, the rise time of the FET gate drive signal is also < 200 µs. This assumes a nominal gate capacitance of 50 nF as specified in the *Electrical Characteristics* tables.

NOTE

Selection of power FETs should consider the resistive losses that may occur during the undefined voltage range during power up from a complete collapse of battery voltage and holdup capacitance.

INITIAL POWER UP

Cell Connection

The IC design allows connection of the cells in any order. For EEPROM programming, only the VSS and BAT terminals must be connected to allow the device to communicate using the serial communication interface.

For normal pack assembly, the recommended connection procedure is to start with the VSS connection, followed by the (+) terminal of the lowest (most negative) cell, and continuing up the stack to the top (most positive) cell. The BAT voltage shown in Start-Up Timing assumes this connection sequence is used.

Power-Up Sequence and Continuous Fault-Detection Logic

The bq77910 goes through a fixed set of safety checks on each power-up sequence. The same checks are performed on each recovery cycle from the SHUTDOWN state (after a charger is detected).

For each power up, the following tests are made. If any of the conditions indicate a fault, the IC goes into the appropriate protection state. External connections may be required for fault recovery (such as load removal or insertion into charger). *The device goes through a power-up sequence in < 100 ms, assuming no faults exist.*

After the release of the internal digital reset, the logic begins a power-up safety check. Two internal signals, designated PWRUP_SAFE_CHK and PWRUP_DONE, control the sequence.

When PWRUP_DONE is low, the following conditions are forced:

1. CHG and DSG external pins / gate drive signals are low.
2. UV_HYST = HI (internal logic signal – use hysteresis level above UV threshold to clear fault)
3. OV_HYST = HI (internal logic signal – use hysteresis level below OV threshold to clear fault)

After 50 ms of time has elapsed, a pulse of PWRUP_SAFE_CHK performs a check of each of the following circuits (with all time delays disabled):

1. UV comparator
2. OV comparator
3. OCD comparator
4. SCD comparator

If a fault condition was found for any of the circuits, an internal fault status bit is set. For another 50 ms, the circuit has a chance to recover if the sample was corrupted. At the end of 100 ms, the PWRUP_DONE signal is released. If no faults exist, the CHG, DSG, UV_HYST, and OV_HYST return to their normal-mode state.

Several of the protection circuits were not included in the power-up sequence (SCC, OT, TS, TO, OC). These faults are checked after the power-up sequence is completed. **Note:** This check is only performed on a power up from LDO-off or a digital reset occurring (i.e., POR state).

Start-Up Timing

The following timing diagrams refer to signals at the device pins as well as to the following INTERNAL logic signals.

- BAT_UVLO = HI when the BAT pin is below the POR threshold (undervoltage lockout).
- WAKEUP = HI whenever a charger is attached.
- UV_STATUS = HI when n UV condition has been detected.
- OV_STATUS = HI when an OV condition has been detected.

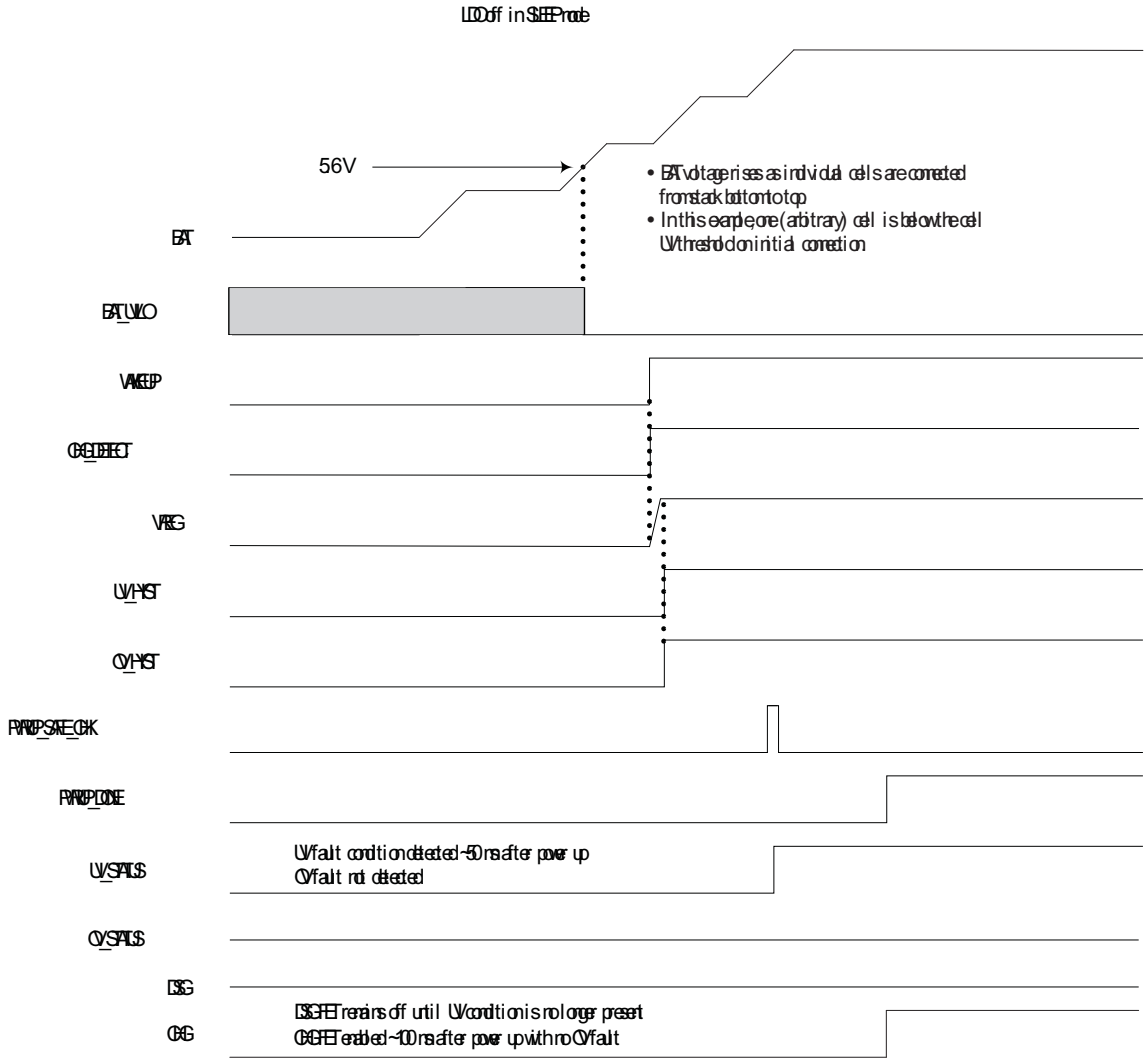


Figure 4. Initial Power Up With Single-Cell UV Fault

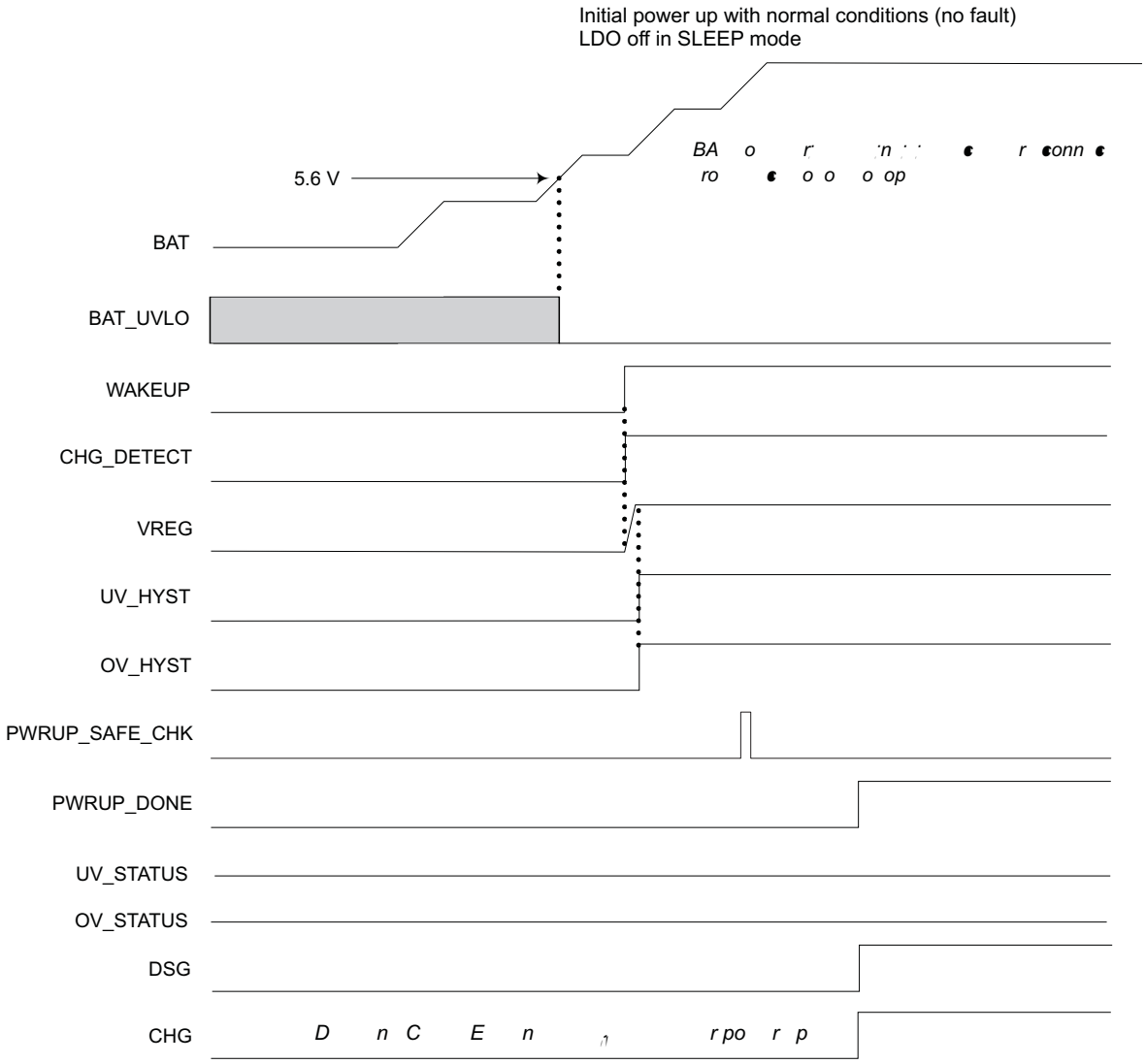


Figure 5. Initial Power Up With Normal Conditions (No Fault)

Table 2. Fault Detection, Action, and Recovery Condition Summary

Fault Condition	Fault Detection Parameter	Filter Time	Action Taken			EEPROM Config (if Applicable)	Recovery Conditions
			FET		MODE		
			CHG	DSG			
CELL OVERVOLTAGE	Any cell > V_{OV}	t_{OV}	OFF	ON	OV FAULT protection state	OV_TS_CTRL = 0	All cells < OV-hyst
					EXT CHGR DISABLE (TS pin→low)	OV_TS_CTRL = 1	
CELL UNDER-VOLTAGE	Any cell < V_{UV}	t_{UV}	OFF[1][2]	OFF	UV FAULT protection state[3]	UV_REC bit = 0	1) Both FETS ON when all cells >UV + hyst [4] 2) CHG FET enabled immediately if charger detected
			OFF[5][2]	OFF	UV FAULT protection state[3]	UV_REC bit = 1	1) Both FETs enabled when all cells >UV + hyst AND load removed 2) CHG FET enabled immediately if charger detected
PACK OVER-TEMPERATURE	Pack temperature out of range, 5 0 Td (state)Tj ET BT /F2 6 Tf 100 Tz 0 0 0 rg 450.1 60 0 0 r Td (0)j ET BT /F2 6 Tf 100 Tz 0 0384Td (+)Tj 5 Tc 0 0 1 0 r Td T /F1 6 Tf 100 Tz 7.13 0 Td (CHG)Tj 15.13 0 Td (FET)Tjte	(1-2) × t_{THERM_CHECK}	OFF	OFF	OT FAULT protection state	TMP_REC bit = 0	V_{TS} > VHOT + hysteresis[6]
			OFF	OFF		TMP_REC bit = 1	V_{TS} > VHOT + hysteresis[6] and load

V_{OV}

CELL-BALANCING FUNCTION

The bq77910 implements an internal cell-balance control circuit and power FET structure. Because no CPU is available to manage a complex algorithm, a simple and robust hardware algorithm is implemented.

Overview

- Uses a separate comparator to check if cells have reached the balancing threshold to start balancing (i.e., does not use the OV trip comparator)
- Balance and charge can run concurrently – no charge-time extension
- Compare cell voltages – cell with highest voltage is bled off for time $t_{CELL\_BAL\_CHECK}$.
- Balancing current set by R_{VCX} – effect of balancing current on cell-to-cell voltage differential depends on cell capacity and $t_{CELL\_BAL\_CHECK}$.
- Cell-balancing options programmable – balancing threshold, when to balance (always, only during charge, or never), and how long to balance

Control Algorithm Description

- **Potential balancing action is updated (latched) every *minimum dwell time* $t_{CELL\_BAL\_CHECK}$**
  1. Action = bleed highest cell above cell-balance start voltage [Note: no hysteresis]
  2. Only one cell is bled at a time
  3. A minimum dwell time of 7.5 minutes equates to <0.5% capacity at 2 Ah and 50 mA balancing current)
  4. Calculation of potential balancing action is reset/inhibited when timer is expired to minimize current draw on the cell stack in case of charger termination
- **Balancing action is suppressed if any of the following are true:**
  1. Highest cell voltage < cell-balance start voltage
  2. Balance timer has expired (when configured for balancing time-out)
  3. Charger is not detected when configured to balance only in charger
  4. Cell-voltage measurement is active
- **Balancing action inhibited during cell measurement**
  1. Measure for 50 ms, balance for 200 ms per each 250-ms cycle (80% utilization)
  2. Cell measurements are *frozen* when balancing output is asserted
  3. OV, UV protection delay time is constrained to be 500 ms or longer
  4. Cell balancing is suspended when an OV/UV condition is present and is being timed for fault determination (maximum time for OV = 2.25 s; UV = 32 s).
  5. Cell balancing is resumed after the fault checking has been completed, whether faults are cleared or latched
- **Recommended system design – charger continues to *top up* the pack when connected**
  1. This may not be the case with certain chargers which shut down once charge current taper limit is reached.
  2. Timer should be enabled to prevent balancing from discharging the pack (maximum balance time is limited).
  3. Timer value is selectable via EEPROM (1, 2, 4, or 8 hours).
  4. Timer value of 4 hours limits discharge of 4-cell pack to ~2.5% at 2 Ah and 50-mA balance current; 10-cell pack to ~1% at 2 Ah and 50-mA balance current. (1 C12-0 TdS 4. Timer=
  5. Ini72 1259.0 Td (paused (during)Tj ET BT /F1 10 Tf 100 Tz (discharge)Tj (14.90 0 Td 0 Tc 24 balance)Tj 56.35 0 Tf 100 Tz 0 0 0 rg 8.

External Connections for Cell Balancing

Multiple options are supported for different cell-balancing requirements. These are summarized in the following sections. These diagrams do NOT show the other external connections such as BAT, TS, CHGST, or power FET arrangements. See subsequent sections for more complete application diagrams showing all external connections.

Normal Configuration – Balancing With Internal FETs

The basic cell balancing-configuration is shown here. Balance current must be limited using external resistance. Resistive component sizes limit the balance current as the return current flows through the VCx pins. Because resistor values are relatively low (to allow sufficient balance current), it may be necessary to maximize external capacitor sizes, depending on the filtering requirements.

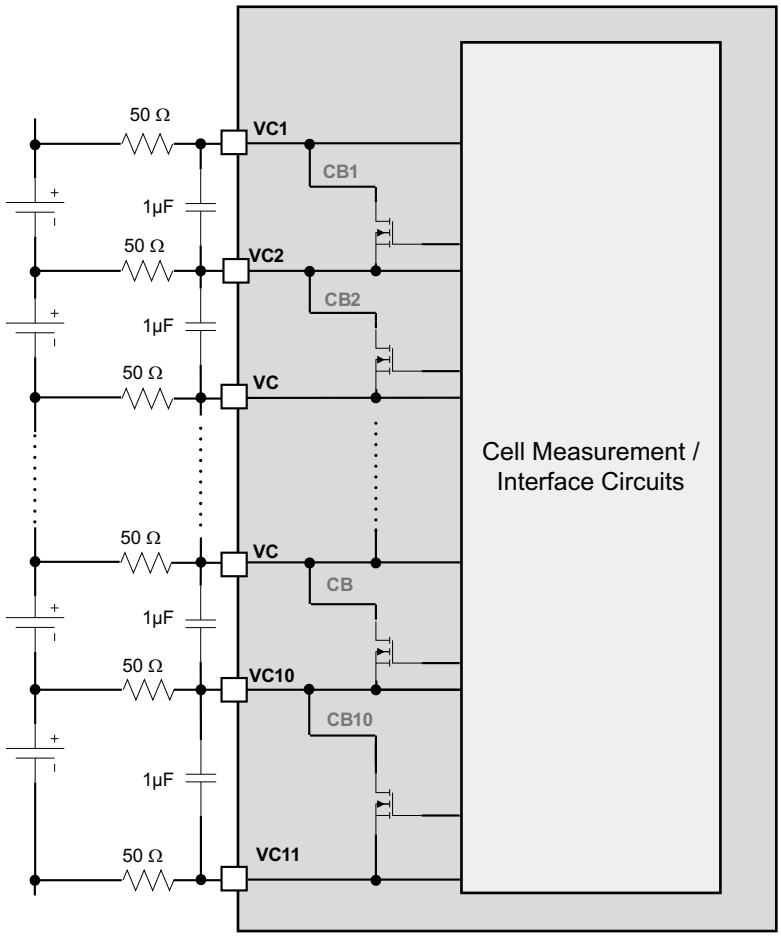


Figure 6. Typical Balancing Configuration (~50 mA)

Low-Current Cell Balancing – External Filtering for Cell-Voltage Readings

To limit balancing current further, the external series resistance can be increased as shown. Balancing can be fully disabled by setting EEPROM bit CB_EN = 0 if desired.

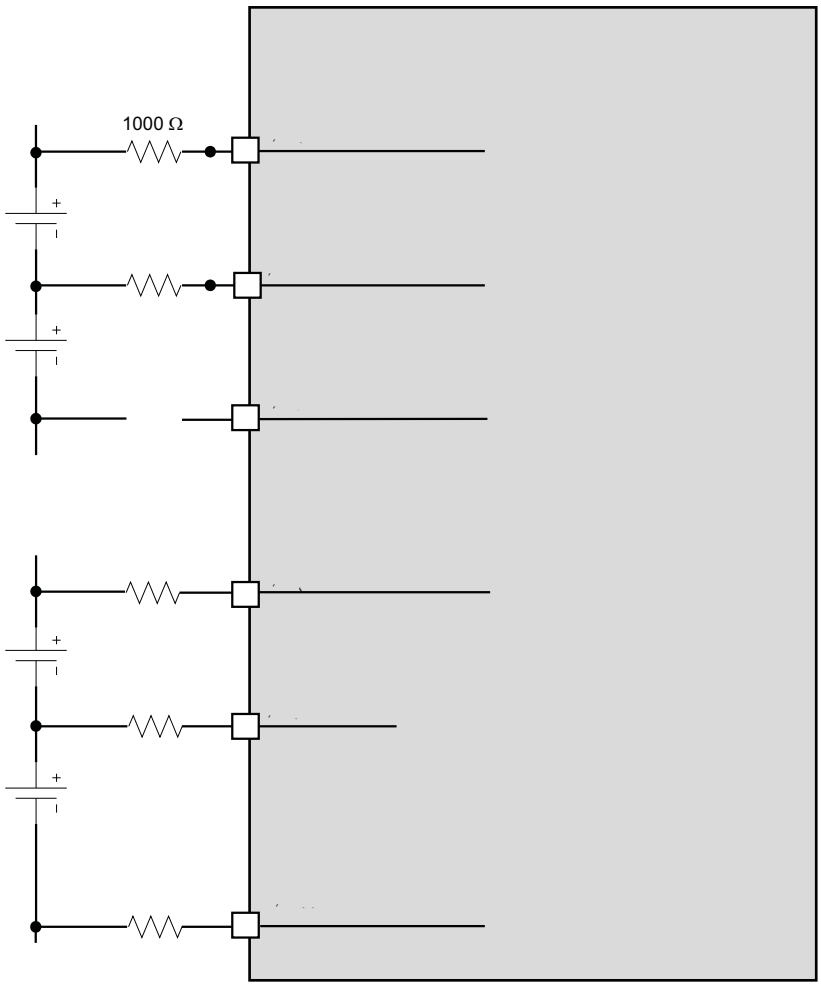


Figure 7. Typical Low-Current Balancing Configuration (~2 mA)

High-Current (Approximately 100-mA to 150-mA) Balancing Using External Power FETs

In this example, external PMOS devices are driven from the IC internal NMOS balance FETs. Current limiting is controlled by the external resistors and is on the order of 100 mA to 150 mA, depending on cell voltage. Contact TI for application example.

APPLICATION INFORMATION

Internal Voltage Regulator

The bq77910 has an integrated low-power linear regulator that provides power to both internal and any optional user-defined external circuitry. The input for the regulator is derived from the BAT terminals. VREG nominal output value is 3.3 V and is also internally current-limited. The minimum output capacitance for stable operation is 1 µF.

The regulator (and the IC internal circuitry) is disabled during the SHUTDOWN mode. When the regulator circuit is disabled (including the time during the power-up sequence of the IC) the DSG and CHG FETs are driven OFF.

Charger Detection and Wake-Up

The bq77910 contains a mechanism to detect the presence of an external charger and allow the device to wake up from the low-power shutdown mode when the LDO has been turned off. A low-power wake-up circuit monitors the CHGST pin to determine the charger connection event.

CHGST Pin Detection

Because the bq77910 is designed to use low-side NMOS FETs to control current flow to / from the battery pack, charger presence detection cannot be determined simply by checking the positive terminal voltage. To allow detection of the presence / absence of an external charger under any operating conditions, the bq77910 implements a charger sense pin, designated CHGST. If a voltage of greater than (nominally) 0.5 V is detected at the CHGST pin, the bq77910 logic assumes that a charger has been connected. *The voltage monitoring circuit at the CHGST pin is an always-on subsystem within the chip. When the proper voltage appears at the CHGST pin, the IC wakes up from the SHUTDOWN mode after a charger is connected.* If fault conditions exist, the part may re-enter a low-power or SHUTDOWN state, depending on the configuration.

The means of connecting the CHGST pin is user- and application-dependent, and may vary with the external contact structure of the battery pack.

For example, a dedicated CHARGER(+) contact with attenuating resistors can be used such that the CHGST pin is pulled high whenever the pack is inserted into a charger.

For a system/application which uses a charge-protection FET to disconnect the charger (–) during a fault condition, it is recommended that the connection to the CHGST pin be pulled up to the charger (+) potential (using a pullup resistor) on the charger side to prevent this signal from going negative with respect to the pack internal reference (VSS pin) when the charge FET in the battery pack may be open.

If the system does not use a charge FET within the battery pack, the VSS (internal) reference and CPCKN (charger reference) are the same, which allows CHGST to be pulled up to any logic-high level above V_{CHG_DET1} to detect charger insertion.

A timing diagram corresponding to the UV fault/recovery condition using the CHGST signal is shown in Figure 8.

CPCKN Pin Detection

When the device is shut down with LDO off, a potential less than approximately VSS – 2 V applied to CPCKN causes the LDO to turn on and the power-up sequence to commence. However, the power-up state is not latched, and if CPCKN falls above the VSS – 2 V threshold, the device again shuts down.

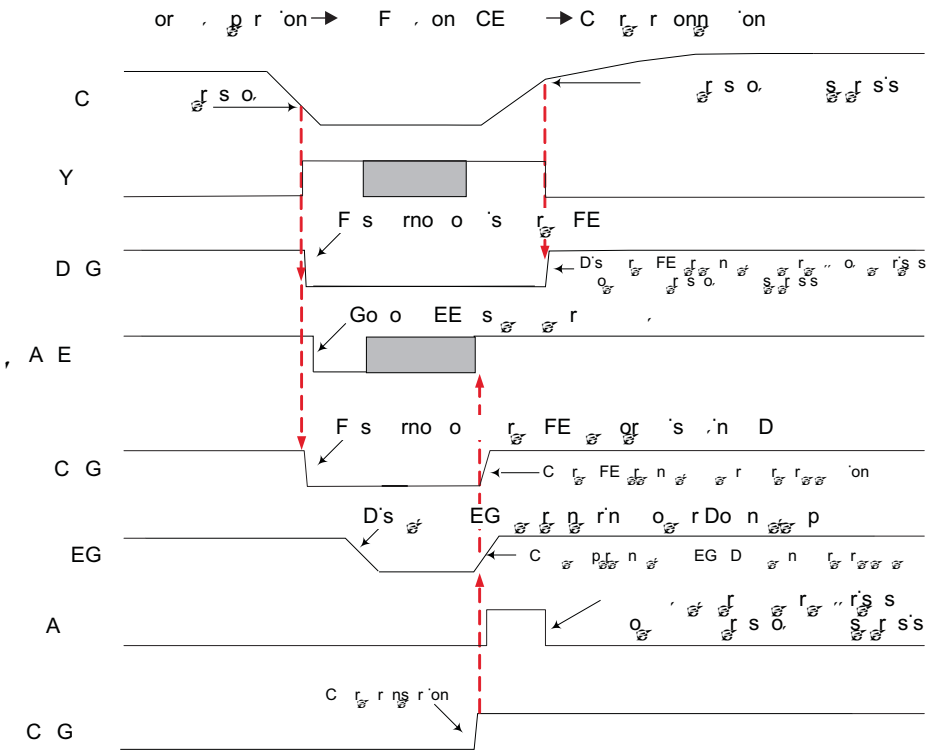


Figure 8. Normal Operation, UV Fault on VCELLx, Then Charger Connection

Temperature Sensing

TS and VTSB Pin Interface

The bq77910 uses the TS pin input to read the voltage on an external thermistor to determine the pack/system temperature. The VTSB pin allows the IC to generate its own bias voltage to drive the thermistor. To save power, the VTSB bias supply is pulsed ON only when the temperature readings are being taken. The VTSB pin is powered by the LDO output (VREG) and with a maximum output impedance of 150 Ω.

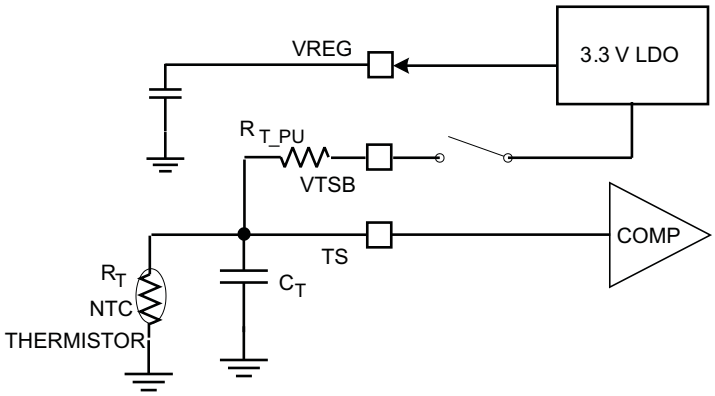


Figure 9. TS and VTSB Pin Interface

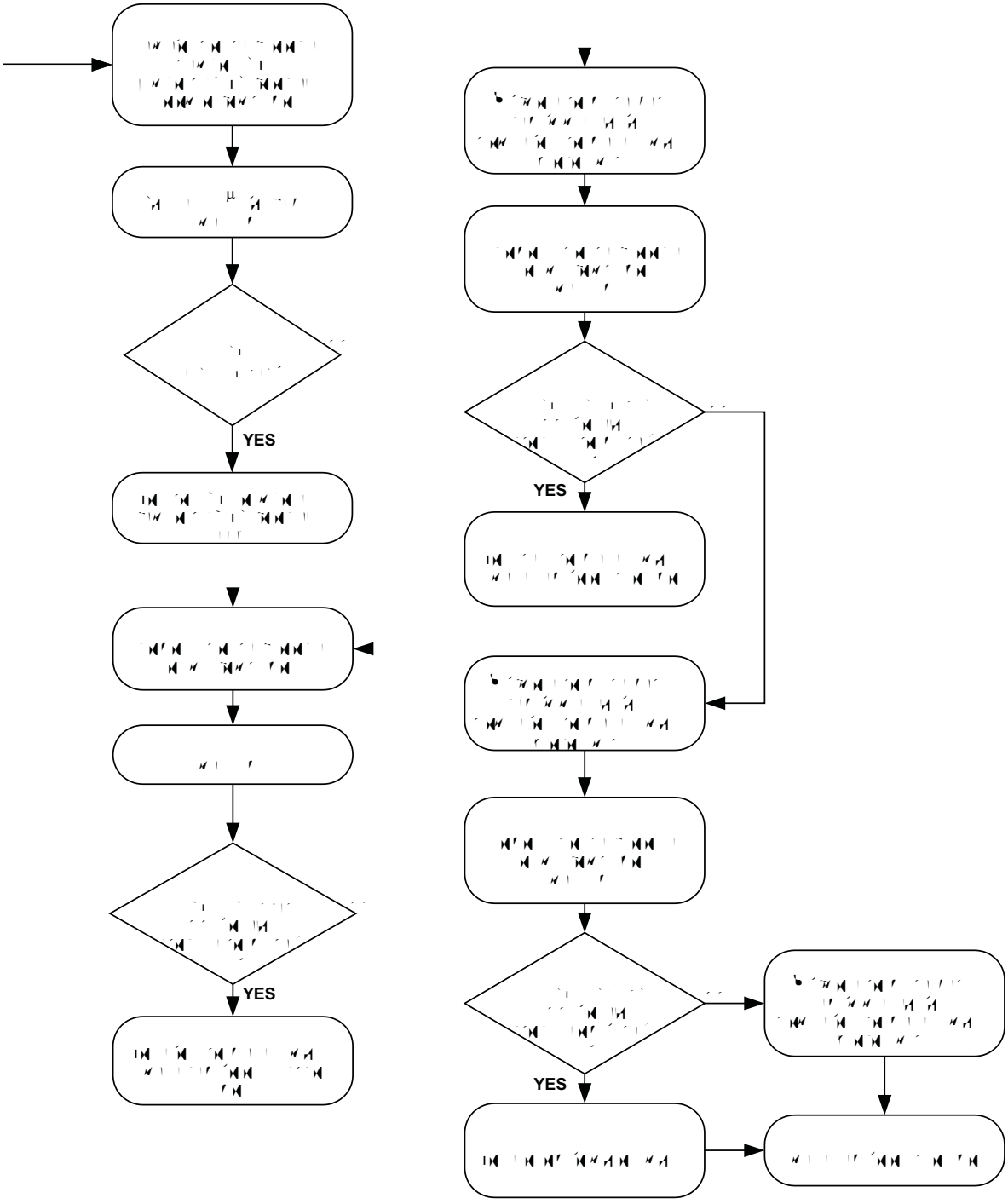
A negative-temperature-coefficient thermistor in the topology shown in Figure 9 is assumed. With this arrangement, the *voltage* at the TS will be lower for high temperature, and higher for low temperature. If the voltage measured at the TS pin is below the V_{HOT} threshold, a pack overtemperature condition is detected.

In the extreme fault cases, an open (disconnected) thermistor indicates a voltage at the TS pin equivalent to the VREG pullup voltage, and a shorted thermistor indicates a voltage close to 0 (VSS). An open-thermistor fault recovers within the fault filter time following removal of the open condition. Shorted-thermistor detection places the device into the low-power SHUTDOWN mode, requiring re-insertion into a charger for wakeup.

External Bias Supply Detection

During the time period in which the bq77910 checks the thermistor status, a weak (nominal 1-µA) current is applied from the TS pin to VSS. If V_TS > V_EXT_PU, then the IC operates as if an external supply is present and does not enable the VTSB internal supply. A sequence of operations is performed to determine the existence of shorted thermistor, open thermistor, or pack overtemperature faults as listed in the following section.

Temperature Measurement / Fault Detection Logic Flow Diagram



Battery Pack / Charger Shared-Thermistor Functionality

The pulsing of the VTSB pin is enabled ONLY when the IC determines that there is no external supply (e.g., from the charger) already driving the thermistor. This allows a single thermistor to be used by both the bq77910 and the external charger to measure pack temperature. This can also be used as a method of charger presence detection in case a dedicated charger-detect pin is not implemented in the end-equipment pack design.

By connecting the CHGST pin to the TS pin on the battery-pack internal circuit board, a three-terminal battery-pack design with (+), (–) and (T) (thermistor) contacts is compatible with the charger-detection mechanism of the bq77910. Because the external charger normally applies a bias voltage to the TS pin from an external source, there is a voltage present on the CHGST pin whenever the pack is inserted into the charger.

NOTE

V_{TH_xxx} (thresholds) are ratiometric based upon VREG. Care should be taken if using an external pullup to a voltage other than the VREG voltage to account for the difference in these detection thresholds.

Depending on the arrangement of the power FETs within the pack, the sharing of a common thermistor between the BMU and the external charger may not be feasible. Applications which **do not** use a CHG disconnection FET are supported, because there is a common ground reference between the external charger and the internal IC ground.

In case of applications which **do** use a CHG FET, the following issues should be understood from the system point of view:

- When the CHG FET is disabled (as in a fault condition), the internal reference (VSS pin of the IC) is disconnected from the external reference (CPCKN connected to charger return path).
- When a charger is connected and powered on, the CPCKN voltage is negative, and it is possible that the CHGST pin is negative with respect to the IC VSS pin.
- The CHGST and TS pins are not internally protected from negative voltages.
- If an external clamp circuit is used to prevent the CHGST voltage from going below 0 V with respect to VSS, and the CHGST/TS pins are connected within the pack, the TS pin indicates an invalid temperature range (or perceived thermistor-shorted fault) until the CHG FET is closed.
- If a charger is connected and not powered on, the CHGST pin may be pulled up to the PACK+ rail. This pin is internally clamped to a safe voltage; however, series resistance is required to avoid overcurrent damage to the internal clamping circuit. If the CHGST and TS pins are tied together within the pack, this resistance affects the reading of the pack internal thermistor by the external device.
- Ideally, the external charger should be designed such that a negative voltage (with respect to the pack internal VSS) cannot be imposed on the CHGST/TS pin when a charger is connected.
- In the case of the CHG FET ON and current flowing, the CPCKN potential may be a few hundred millivolts below the IC VSS pin (depending on charge current level and charge FET on-resistance). This also affects the accuracy of the thermistor voltage as read by the external charger. A suggested approach is for the external charger to momentarily interrupt charge current flow while taking the pack temperature reading when a CHG FET is implemented.

Charge / Discharge Enable Operating Thresholds

If the voltage measured at the TS pin is below V_{TH_HOT}, a pack overtemperature condition is detected. The bq77910 disables the charge and discharge FETs (but remains in the active mode). Using a standard 103AT thermistor and 10-kΩ pullup resistor, this corresponds to approximately 60°C. The temperature level is chosen to be slightly above the normal charge disable level implemented by an external charger, and would not normally activate during charge unless the charger's own overtemperature shutdown did not trigger before this level. The external charger typically also has a cold-temperature charge inhibit (roughly between 0°C and 10°C) as shown in Figure 10.

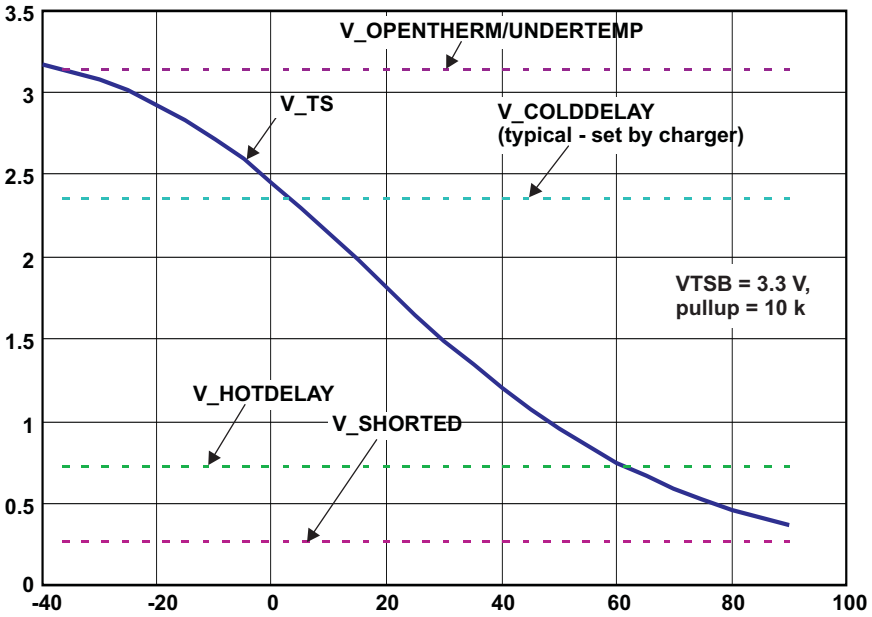


Figure 10. Typical Thermistor Response and Protection Thresholds (VTSB = 3.3 V, Pullup = 10 kΩ)

The bq77910 limits pack operation in the case of an overtemperature, undertemperature, open, or shorted thermistor. An overtemperature fault opens the protection FETs only; a shorted-thermistor fault also puts the device into low-power / fault protection mode. Due to the range of resistance values available with a typical thermistor, an undertemperature fault is indistinguishable from an open-thermistor fault and has the same protection mechanism (enter protection state, but device stays awake). The V_{TH_OPEN}, V_{HOT}, and V_{TH_SHORT} thresholds are ratiometric to the VTSB pin bias voltage. Typical values are shown; see the parametric tables for details.

OV_TS_CTRL (EEPROM Bit) Interface

In the case of a battery pack which implements a CHG pass FET, the charging function can be disabled by opening the FET

Additionally,

Series CHG and DSG FET Configuration

Use of a separate contact (i.e., CHGST) for charger detection is preferred if the cell-balancing function is used. This is to allow balancing to occur only while charging. Otherwise, if the part cannot detect the presence of a charger, balancing must be enabled to occur at all times or not at all. The CHGST pin should be protected from possible negative voltage inputs which may occur if connected to a charger with the CHG FET open.

Note that in shutdown with the LDO off, the specified shutdown currents require that the voltage at CPCKN with respect to VSS is controlled. In the parallel FET case, CPCKN is clamped through the body diode of the charge FET. In the series FET case, external circuitry is required to keep CPCKN from floating. Contact TI for recommended application circuits.

If current is able to flow from CPCKN through the charge FET (e.g., through the body diode), the resistor R_{LDRM_DET} is required to discharge DPCKN for proper detection of load removal. When the FETs are open and a load is present, the PACK– terminal and consequently DPCKN is pulled up to PACK+. When the load is removed, DPCKN is discharged through R_{LDRM_DET}. Detection of load removal occurs when the voltage at DPCKN (referenced to VSS) falls below 2 V (typical).

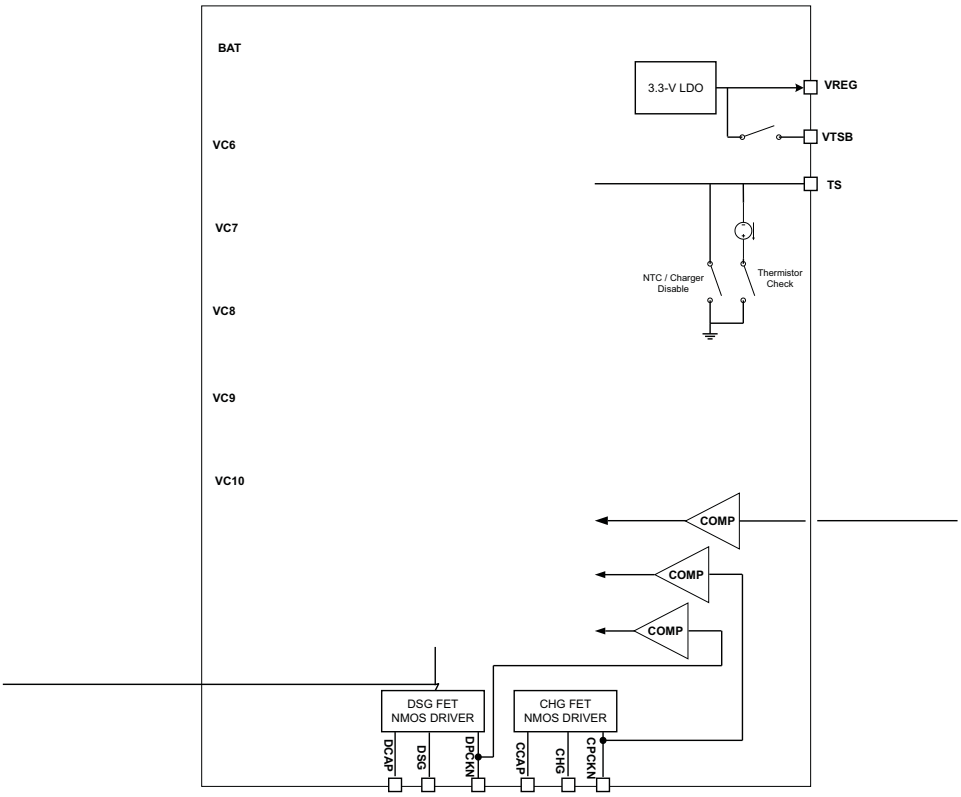


Figure 11. Example Series FET Configuration Using the CHGST Pin

Separate CHG(–) and DSG(–) Return Paths With Both FETs

In this configuration, if the charge current is typically much lower than the discharge current, a lower-cost component can be used for the charge control FET than in the series configuration previously shown.

Use of a separate contact (CHGST pin) is preferred if the cell balancing function is used. This is to allow balancing to occur only while charging. Otherwise, if the part cannot detect the presence of a charger, balancing must be enabled to occur at all times or not at all.

The CHGST pin should be protected from possible negative voltage inputs which may occur if connected to a charger with the CHG FET open.

Figure 12. Example Parallel (Split) Power Path FET Configuration Using CHGST Pin

Separate CHG(–) and DSG(–) Return Paths With DSG FET Only

In this configuration, no charge-control FET is implemented. As a result, the bq77910 is unable to interrupt charge current when an overvoltage condition occurs. The suggested method to stop the charger in an overvoltage event is to use the thermistor signal to indicate a fault condition. The system should configure the OV_TS_CTRL bit high, so that when an overvoltage occurs, the charger detects that an overtemperature condition has occurred, and halts charging. (See the *OV_TS_CTRL (EEPROM Bit) Interface* section.)

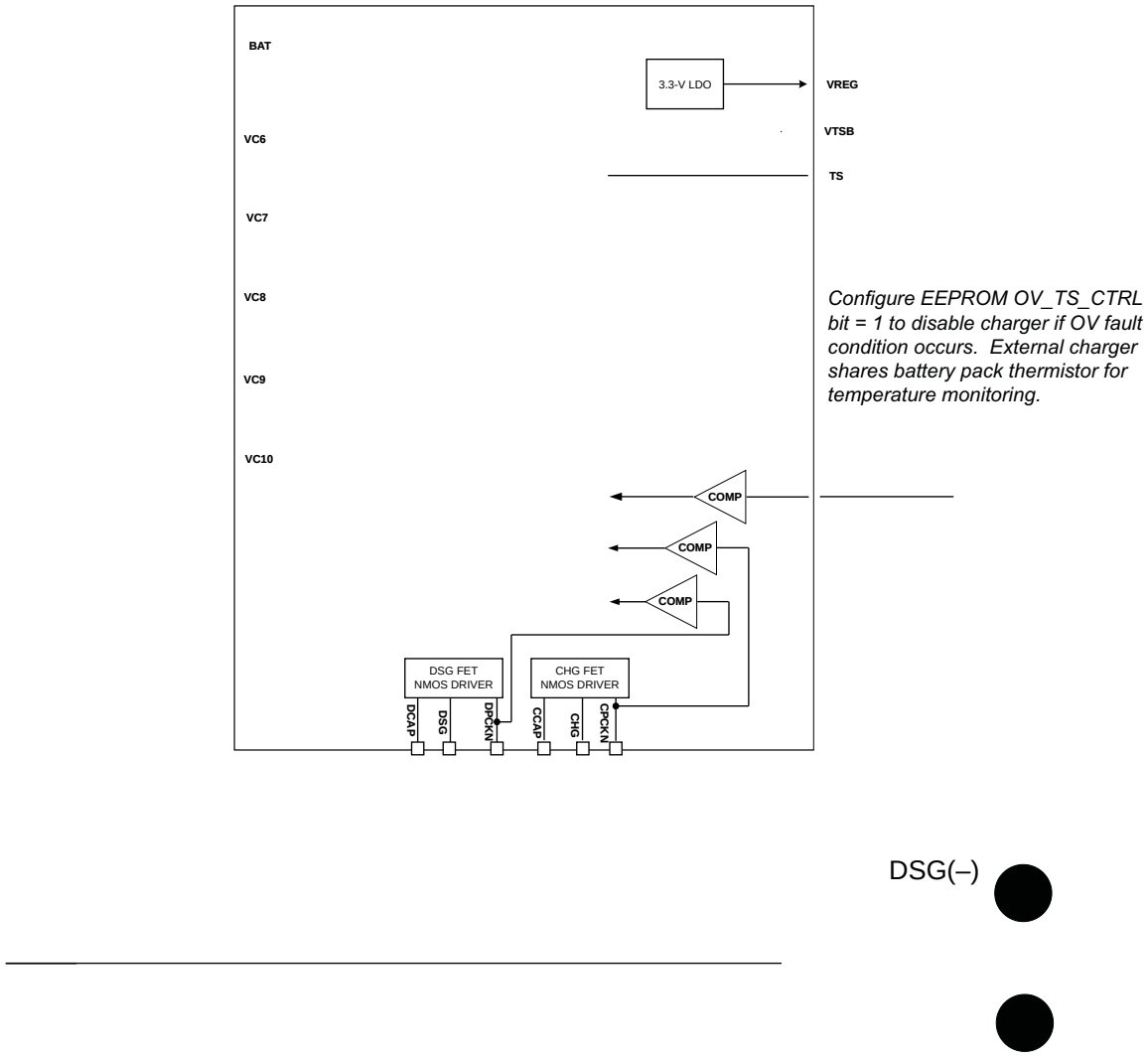


Figure 13. Example Split Power Path With No Charge FET Using the CHGST Pin

Common Return Path With No FETs

If no internal FETs are implemented inside the battery pack, the only means of protection available is for the bq77910 control signals to be used as signals to the external device (tool or charger). These signals must be used by the external equipment to control the interruption of current flow in case of a fault condition. When no charge FET is implemented, the CHGST signal interface must be used to indicate to the battery pack that a charger has been connected.

In this configuration, an overvoltage fault is distinguished from an undervoltage fault by observing that during an overvoltage fault only the DSG control switches low, while during an undervoltage fault, both the DSG and CHG controls switch low.

If the OCD/SCD/SCC (overcurrent/short-circuit) protections are used in this configuration, the part cannot interrupt current flow. The fault detection *auto-recovers* because the DPCKN pin is seen at ground potential (which is the normal indication that the external load has been disconnected). The system may cycle into and out of fault protection mode depending on external conditions, so the host-equipment designer should be aware of this potential situation.

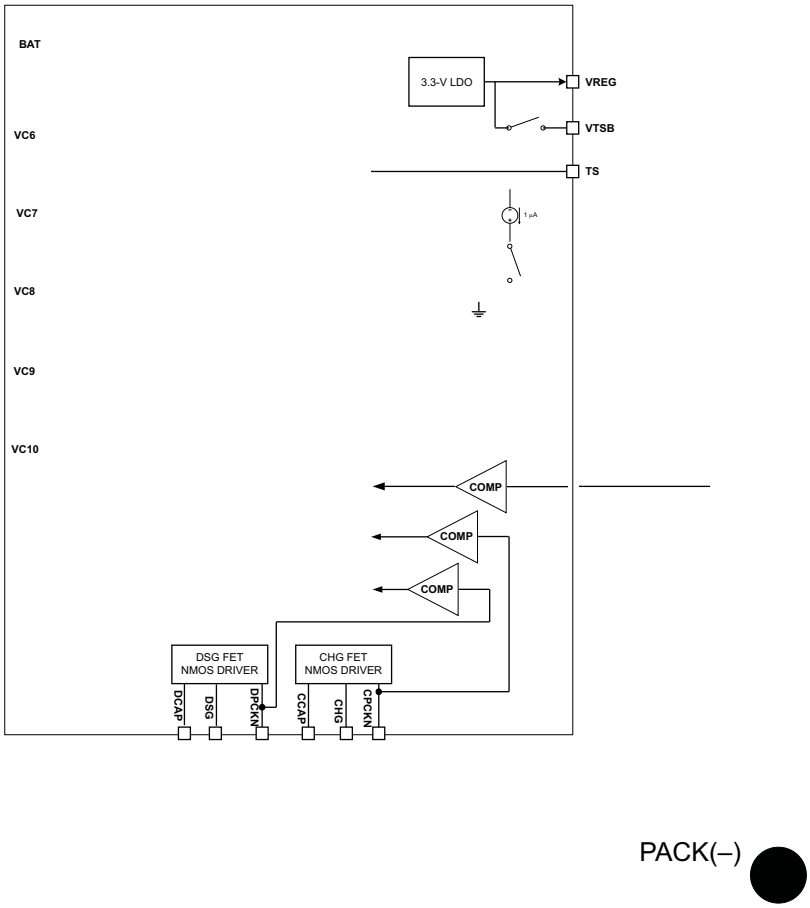


Figure 14. Single Power Path, No FETs

4 to 10 Series Cell Configuration

All cell input pins of the device are used for a 10-cell battery pack application. The bq77910 supports pack configurations ranging from 4 to 10 series cells. If fewer than 10 cells are used in an application, all unused VCx cell input pins should be tied together and pulled up to the most-positive cell input. Pullup resistance value is not critical; a 100 Ω–1000-Ω value is suggested. An example for a 5-cell application is shown here. Cell configuration is programmable by EEPROM, using the SYS_CFG register bits CNF[2:0].

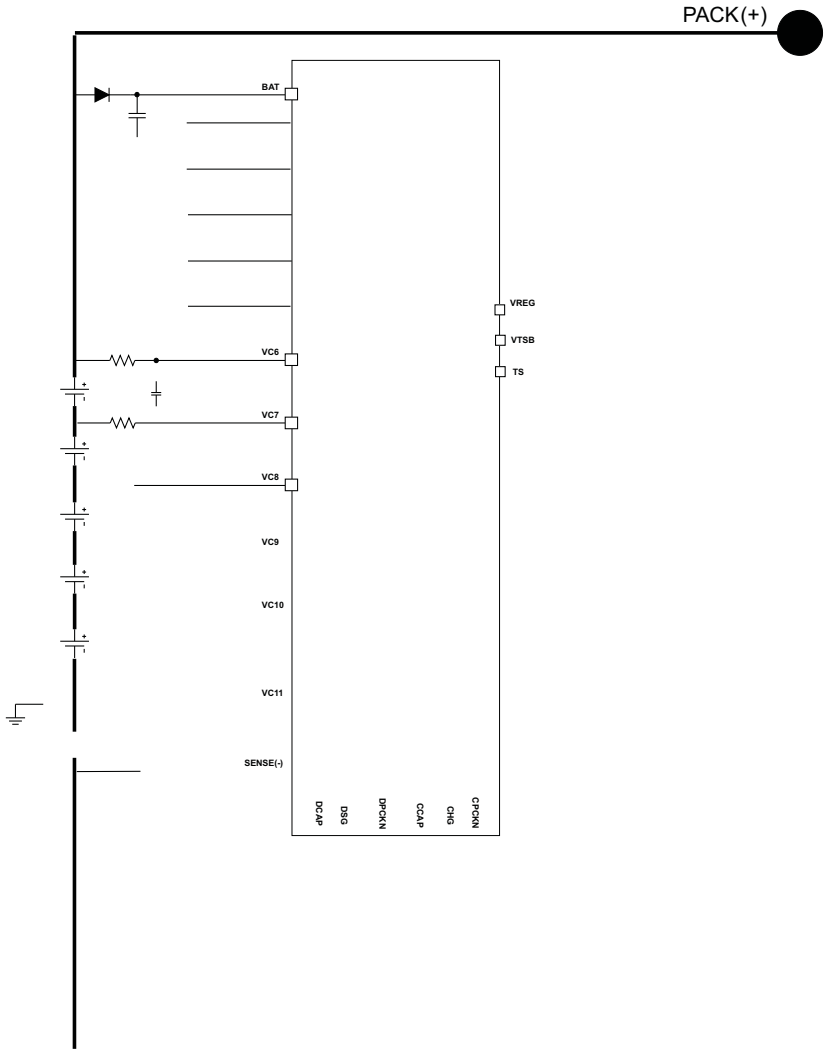


Figure 15. Unused VCELLx Pin Configuration

Delay Time Zero

The ZEDE pin enables the EEPROM-programmed detection-delay times when connected to VSS (normal operation). A strong pulldown to VSS is recommended to prevent external circuit noise from causing ZEDE to go high. The detection delay time is set to minimum when this pin is connected to VREG. This is used in battery manufacturing test. When programming the EEPROM, this pin should to be connected to VREG to enable the serial communication interface.

Ship-Mode Equivalent Functionality

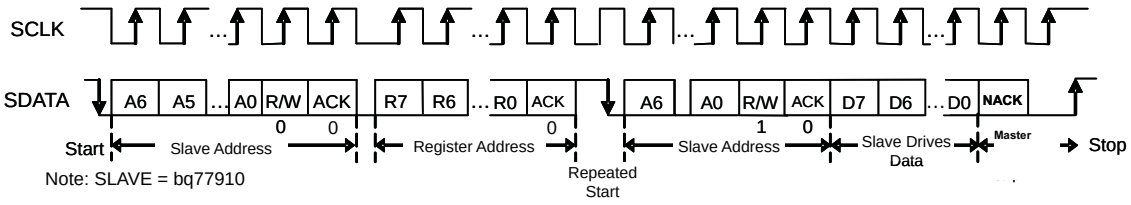
Because the BMU is designed for standalone-mode operation, it does not incorporate a programmable-entry *ship mode*, which is intended for long-term storage of a battery pack after initial assembly.

The recommended method

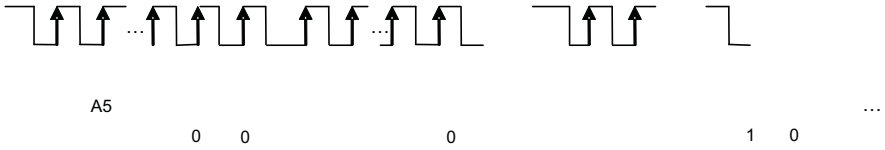
Bus Write Command to bq77910

A5

Bus Read Command from bq77910 (Protocol A)



Bus Read Command from bq77910 (Protocol B)



REGISTER SET AND PROGRAMMING

Memory Map

The bq77910 has 10 programmable EEPROM registers and one RAM register used to access / write the EEPROM data. The EEPROM bits are used to program the various threshold, delay, configuration, and recovery control settings. The address, register names, and individual control bit names are shown in the following table. Descriptions of each individual register and available programming options are provided in the subsequent sections. Bits labeled RSVDx (gray) are unused and left for future options.

WARNING

For RSVD1, SERIOUS SAFETY RISK MAY APPLY to battery monitoring features of BQ77910DBT, BQ77910DBTR, BQ77908DBT, and BQ77908DBTR if RSVD1 is not set to 0. Some uses of these components could present serious risk of fire, explosion, battery rupture, serious injury, or death if RSVD1 is not set to 0.

Address	Register Name	7	6	5	4	3	2	1	0
0x00	EE_PROG(1)								VGOOD(1)
0x01	SYS_CFG	CNF2	CNF1	CNF0	CHG_TMP_DIS	TMPEN	OT_REC	RSVD1	SOR
0x02	OV_CFG1	RSVD2	RSVD3	OVT5	OVT4	OVT3	OVT2	OVT1	OVT0
0x03	OV_CFG2	OV_TS_CTRL	OVH2	OVH1	OVH0	RSVD4	OVD2	OVD1	OVD0
0x04	UV_CFG1	UV_HYST_INH	RSVD6	RSVD7	RSVD8	UVT3	UVT2	UVT1	UVT0
0x05	UV_CFG2	UV_REC	UV_REC_DLY	UVH1	UVH0	RSVD10	UVD2	UVD1	UVD0
0x06	OCD_DELAY	RSVD11	RSVD12	RSVD13	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0
0x07	SCD_DELAY	RSVD14	RSVD15	ISNS_RNG	SCDD_RNG	SCDD3	SCDD2	SCDD1	SCDD0
0x08	OCD_SCD_TRIP	SCDT3	SCDT2	SCDT1	SCDT0	OCDT3	OCDT2	OCDT1	OCDT0
0x09	SCC_CFG	SCCD3	SCCD2	SCCD1	SCCD0	SCCT3	SCCT2	SCCT1	SCCT0
0x0A	CELL_BAL_CFG	CB_EN1	CB_EN0	CBT1	CBT0	CBV3	CBV2	CBV1	CBV0

(1) Read-only bit.

System Configuration (SYS_CFG, Address 0x01)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	CNF2	CNF1	CNF0	CHG_TMP_DIS(1)(2)	TMPEN	OT_REC	RSVD1(3)	SOR
If 0	8 possible settings to determine pack configuration (4 to 10 cells); see following table			Default value – thermal protection active in all modes	Disable temperature sensing	Recover from OT fault when pack has cooled below limit (incl. hysteresis)	This bit must be set to 0.	Recover from OCD/SCD when load removed
If 1				Thermal protection enabled only when no charger detected; thermal protection DISABLED when CHARGER PRESENT	Enable temperature sensing	Recover from OT fault when pack has cooled below limit (incl. hysteresis) *AND LOAD REMOVED*		Recover from OCD/SCD when load removed and charger attached

(1) If CHG_TMP_DIS = 1, all thermal faults are cleared when a pack is inserted into a charger.
(2) CHG_TMP_DIS takes priority over OT_REC. If both are = 1, then thermal faults are cleared whenever inserted into a charger.
(3) SERIOUS SAFETY RISK MAY APPLY to battery monitoring features of BQ77910DBT, BQ77910DBTR, BQ77908DBT, and BQ77908DBTR if RSVD1 is not set to 0. Some uses of these components could present serious risk of fire, explosion, battery rupture, serious injury, or death if RSVD1 is not set to 0.

Pack Configuration (Number of Cells)

Various pack sizes between 4 and 10 series cells are configured using the CNF[2:0] bits as shown.

CNF[2:0]	Pack Configuration (# Cells)
000	10
001	9
010	8
011	7

OV Detection Configuration #1 (OV_CFG1, Address 0x02)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RSVD2	RSVD3	OVT5	OVT4	OVT3	OVT2	OVT1	OVT0
If 0	NOT USED	NOT USED	Overvoltage trip threshold (64 possible values); see following table.					
If 1	NOT USED	NOT USED						

Programmable Overvoltage Threshold Settings

Using the 5 bits OVT[5:0], up to 64 possible set points for overvoltage trip are possible, as shown. OVT setting is chosen to match the cell type and application requirements.

OVT[5:0]	OV Trip (Volts)	OVT[5:0]	OV Trip (Volts)
0x00	2.800	0x20	3.600
0x01	2.825	0x21	3.625
0x02	2.850	0x22	3.650
0x03	2.875	0x23	3.675
0x04	2.900	0x24	3.700
0x05	2.925	0x25	3.725
0x06	2.950	0x26	3.750
0x07	2.975	0x27	3.775
0x08	3.000	0x28	3.800
0x09	3.025	0x29	3.825
0x0A	3.050	0x2A	3.850
0x0B	3.075	0x2B	3.875
0x0C	3.100	0x2C	3.900
0x0D	3.125	0x2D	3.925
0x0E	3.150	0x2E	3.950
0x0F	3.175	0x2F	3.975
0x10	3.200	0x30	4.000
0x11	3.225	0x31	4.025
0x12	3.250	0x32	4.050
0x13	3.275	0x33	4.075
0x14	3.300	0x34	4.100
0x15	3.325	0x35	4.125
0x16	3.350	0x36	4.150
0x17	3.375	0x37	4.175
0x18	3.400	0x38	4.200
0x19	3.425	0x39	4.225
0x1A	3.450	0x3A	4.250
0x1B	3.475	0x3B	4.275
0x1C	3.500	0x3C	4.300
0x1D	3.525	0x3D	4.325
0x1E	3.550	0x3E	4.350
0x1F	3.575	0x3F	4.375

OV Detection Configuration #2 (OV_CFG2, Address 0x03)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	OV_TS_CTRL	OVH2	OVH1	OVH0	RSVD4	OVD2	OVD1	OVD0
If 0	Do not use TS line for external charger control	8 possible settings to control OV hysteresis (see following table)			NOT USED	8 possible settings to control OV sense delay (see following table)		
If 1	Use TS line for external charger control (if OV event, pull TS = low)				NOT USED			

OV Hysteresis Settings

Eight possible hysteresis settings are selectable using the bits OVH[2:0] as shown in the following table.

OVH[2:0]	OV Hysteresis (mV)
000	300
001	250
010	200
011	150
100	100
101	50
110	25
111	0

OV Delay Settings

Eight possible OV trip time delay settings are selectable using the bits OVD[2:0]

OVH[2:0]	OV Delay (Seconds)
000	0.50
001	0.75
010	1.00
011	1.25
100	1.50
101	1.75
110	2.00
111	2.25

UV Detection Configuration #1 (UV_CFG1, Address 0x04)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	UV_HYST_INH	**RSVD6**	**RSVD7**	**RSVD8**	**UVT3**	**UVT2**	**UVT1**	**UVT0**
If 0	Use hysteresis threshold to allow recovery after UV condition (DEFAULT)	NOT USED	NOT USED	NOT USED	Set one of 16 possible values; see following table.			
If 1	Do not use (inhibit) hysteresis threshold to allow recovery from UV threshold	NOT USED	NOT USED	NOT USED				

Undervoltage Trip Threshold Settings

The specific undervoltage trip point required by the cell type and application can be set using the UVT[3:0] bits as shown here:

UVT[3:0]	UV Trip Level (Volts)		UVT[3:0]	UV Trip Level (Volts)
0000	1.4		1000	2.2
0001	1.5		1001	2.3
0010	1.6		1010	2.4
0011	1.7		1011	2.5
0100	1.8		1100	2.6
0101	1.9		1101	2.7
0110	2.0		1110	2.8
0111	2.1		1111	2.9

UV Detection Configuration #2 (UV_CFG2, Address 0x05)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	**UV_REC**	**UV_REC_DLY**	**UVH1**	**UVH0**	**RSVD10**	**UVD2**	**UVD1**	**UVD0**
If 0	Recover from UV fault when all cell voltages increase above V_{UV} threshold+hyst. CHG FET enabled immediately if charger detected	Part does NOT enter SHUTDOWN mode from the UV fault state	1 of 4 possible values, see table below		NOT USED	1 of 8 possible values, binary spacing, see following table.		
If 1	Recover from UV fault only when all cell voltages increase above V_{UV} threshold+hyst *AND* load is removed.	Part *does* enter SHUTDOWN mode if any cell voltage remains <V_{UV}+hyst for >8 seconds in the UV fault state			NOT USED			

UV Hysteresis Level

The UV hysteresis is set using UVH[1:0] bits. Four possible values are available as shown; however, the maximum recovery level is set to 3.5 V in the case of a combination of high UV trip point plus high UV hysteresis values.

UVH[1:0]	Hysteresis (Volts)
00	0.4
01	0.8
10	1.2
11	1.6

Recovery Voltage (Combination of UVT + UVH settings)

UV Trip Level	Hysteresis			
	0.4 V	**0.8 V**	**1.2 V**	**1.6 V**
1.4	1.8	2.2	2.6	3.0
1.5	1.9	2.3	2.7	3.1
1.6	2.0	2.4	2.8	3.2
1.7	2.1	2.5	2.9	3.3
1.8	2.2	2.6	3.0	3.4
1.9	2.3	2.7	3.1	3.5

Overcurrent in Discharge Delay Settings (OCD_DELAY, Address 0x06)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RSVD11	RSVD12	RSVD13	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0
If 0	NOT USED	NOT USED	NOT USED	One of 32 possible delay settings, see following table.				
If 1	NOT USED	NOT USED	NOT USED					

Discharge Overcurrent Detection Delay Settings

OCDD[4:0] (HEX)	OC Detection Delay (ms)		OCDD[4:0] (HEX)	OC Detection Delay (ms)
0x00	20		0x10	500
0x01	40		0x11	600
0x02	60		0x12	700
0x03	80		0x13	800
0x04	100		0x14	900
0x05	120		0x15	1000
0x06	140		0x16	1100
0x07	160		0x17	1200
0x08	180		0x18	1300
0x09	200		0x19	1400
0x0A	220		0x1A	1500
0x0B	240		0x1B	1600
0x0C	260		0x1C	1700
0x0D	280		0x1D	1800
0x0E	300		0x1E	1900
0x0F	400		0x1F	2000

Short Circuit in Discharge Delay Settings (SCD_DELAY, Address 0x07)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	**RSVD14**	**RSVD15**	**ISNS_RNG**	SCDD_RNG	SCDD3	SCDD2	SCDD1	SCDD0
If 0	NOT USED	NOT USED	Use lower range of values for all short-circuit and overcurrent-trip thresholds	Use fast delay settings	One of 16 possible delay settings in each range, see following table.			
If 1	NOT USED	NOT USED	Use higher range of values for all short-circuit and overcurrent-trip thresholds	Use slow delay settings				

SCD Delay Settings

Two separate ranges of 16 possible delay time values are selectable as shown here.

Fast Range (SCDD_RNG = 0)			Slow Range (SCDD_RNG = 1)	
SCDD[3:0]	**SC Detection Delay (µs)**		**SCDD[3:0]**	**SC Detection Delay (ms)**
0x00	60		0x00	50
0x01	120		0x01	100
0x02	180		0x02	200
0x03	240		0x03	300
0x04	300		0x04	400
0x05	360		0x05	500
0x06	420		0x06	600
0x07	480		0x07	700
0x08	540		0x08	800
0x09	600		0x09	900
0x0A	660		0x0A	1000
0x0B	720		0x0B	1100
0x0C	780		0x0C	1200
0x0D	840		0x0D	1300
0x0E	900		0x0E	1400
0x0F	960		0x0F	1500

Discharge Overcurrent/Short-Circuit Trip Levels (OCD_SCD_TRIP, Address 0x08)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	SCDT3	SCDT2	SCDT1	SCDT0	OCDT3	OCDT2	OCDT1	OCDT0
If 0	One of 16 possible SC trip settings (sense resistor voltage), see following table.				One of 16 possible OC trip settings (sense resistor voltage), see following table.			
If 1								

NOTE: SCD and OCD trip levels are controlled by current-sense gain-control bit ISNS_RNG located in register 0x07. Tripcurrent-sense

Charge Short-Circuit Threshold and Delay Settings (SCC_CFG, Address 0x09)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	SCCD3	SCCD2	SCCD1	SCCD0	SCCT3	SCCT2	SCCT1	SCCT0
If 0	One of 16 possible charger short-circuit sensing delay settings, see following table.				One of 16 possible charger short-circuit sensing threshold settings (sense resistor voltage), see following table.			
If 1								

NOTE: SCC trip-level range is controlled by current-sense gain-control bit ISNS_RNG, located in register 0x07. Trip levels measured at SENSE– are referenced to SENSE+.

Charge Short-Circuit Delay-Time Settings

SCCD[3:0]	Charge Short-Circuit Delay (µs)		SCCD[3:0]	Charge Short-Circuit Delay (µs)
0000	60		1000	540
0001	120		1001	600
0010	180		1010	660
0011	240		1011	720
0100	300		1100	780
0101	360		1101	840
0110	420		1110	900
0111	480		1111	960

Charge Short-Circuit Trip-Level Settings

SCCT[3:0]	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 0	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	–10	–50
0001	–15	–75
0010	–20	–100
0011	–25	–125
0100	–30	–150
0101	–35	–175
0110	–40	–200
0111	–45	–225
1000	–50	–250
1001	–55	–275
1010	–60	–300
1011	–65	–325
1100	–70	–350
1101	–75	–375
1110	–80	–400
1111	–85	–425

Cell-Balancing Configuration (CELL_BAL_CFG, Address 0x0A)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	CB_EN1	CB_EN0	CBT1	CBT0	CBV3	CBV2	CBV1	CBV0
If 0	See 4 possible values		See 4 possible values		One of 16 possible settings for cell-balance			

CBV[3:0]	Cell Voltage
1110	2.5
1111	2.4

EEPROM Control Register (EEPROM, Address 0x0B)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	EEPROM7	EEPROM6	EEPROM5	EEPROM4	EEPROM3	EEPROM2	EEPROM1	EEPROM0

These bits enable data write to EEPROM locations (0x01–0x0A) when written with data 0100 0001 (0x41). Pre-read of EEPROM data is available by setting these bits with 0110-0010 (0x62). Default is 0000-0000 (0x00).

EEPROM Write Sequence

EEPROM is written by I^2C command. When ZEDE = H, the SCLK and SDATA lines are enabled to allow I^2C communication.

	(MSB)			I^2C Address +R/W bit				(LSB)
	(MSB)			I^2C Address			(LSB)	
Write	0	0	1	0	0	0	0	0
Read								1

The bq77910 has integrated configuration EEPROM for OV, UV, OCD, SCD, and SCC thresholds and delays. The appropriate configuration data is programmed to the configuration registers and then 0x41 is sent to the EEPROM register to enable programming . By driving the EEPROM pin (set high and then low), the data is written to the EEPROM. The recommended voltage at BAT for EEPROM writing is >7 V. A flowchart showing the EEPROM write / check sequence is shown in Figure 16.

Parity Check

The bq77910 uses EEPROM for storage of protection thresholds and delay times as previously described. Additional EEPROM is also used to store internal trimming data. For safety reasons, the bq77910 uses a column-parity error-checking scheme. If the column-parity bit is changed from the written data, both DSG and CHG FETs are forced OFF as a fail-safe mechanism.

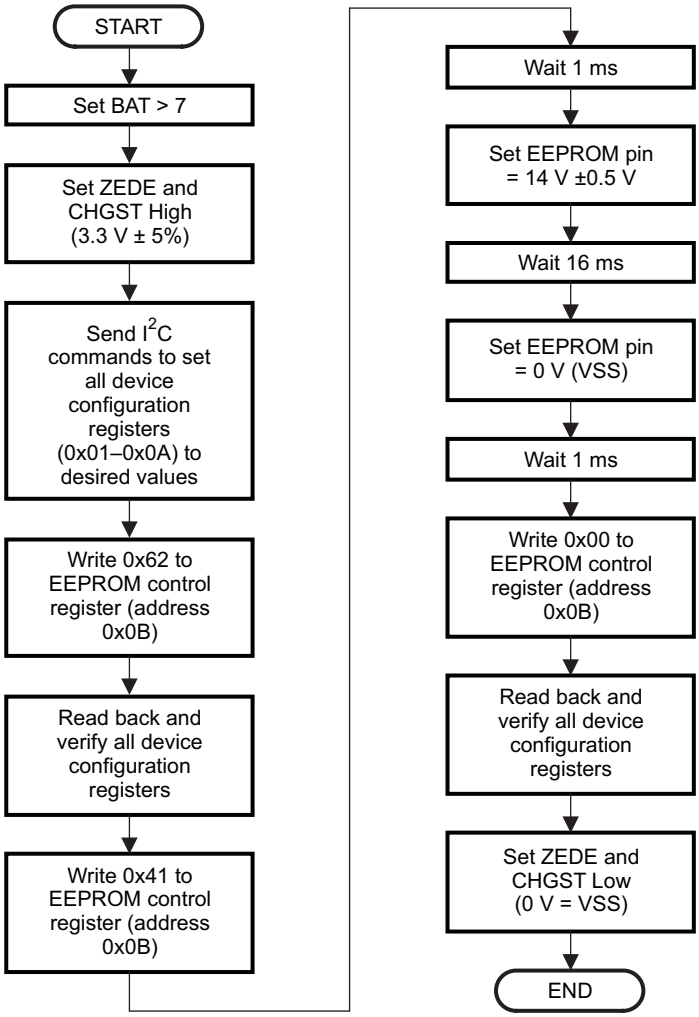


Figure 16. EEPROM Programming Flow Diagram

REVISION HISTORY

Changes from Revision B (May 2011) to Revision C **Page**

- Deleted $I_{SHUTDOWN\_1}$ row from Electrical Characteristics table 7
- Changed text and table of *Power Modes* section 10
- Deleted text from next-to-last paragraph of Power

Changes from Revision C (November 2011) to Revision D **Page**

- Added RSVD1 WARNING 39

Changes from Revision A (October 2010) to Revision B **Page**

- Deleted a Features bullet under Low Supply Current 1
- Changed high end of cell-to-cell differential to 9 V 5
- Added cell input rows to Absolute Maximum Ratings table 5
- Added lower bound to maximum ratings for output voltage on pins CHG and DSG 5
- Added row for regulator current 5
- Deleted row "VC10 to VC1" from Recommended Operating Conditions input voltage range 6
- Changed MAX value 6
- Added cell input rows to Recommended Operating Conditions table 6
- Added VSENSE(+) and (–) rows to Recommended Operating Conditions table 6
- Added "nominal" to parameter descriptions for R_{VCX} and C_{VCX} in Recommended Operating Conditions table 6
- Added I_{REG} and I_{CB} rows to Recommended Operating Conditions table 6
- Changed CREG to CVREG in Recommended Operating Conditions table 6
- Added 0.1 minimum value for CCCAP, CDCAP in Recommended Operating Conditions table 6
- Changed C_{CCAP} and C_{DCAP} note following Recommended Operating Conditions table 6
- Changed I_{CC} from supply current to average supply current and added "(no load)" to test conditions 7
- Changed values for V_{GATE_UV} and $V_{GATE\_UV\_H}$ in Electrical Characteristics 7
- Added "no dc load" to test condition for $V_{(FETON)}$ in Electrical Characteristics 7
- Changed values in Electrical Characteristics for t_f with test condition BAT = 6.4 7
- Changed values for I_{SC} in Electrical Characteristics 7
- Changed values for V_{HOT} in Electrical Characteristics 8
- Changed values for V_{TH_HYST} in Electrical Characteristics 8
- Deleted Current-Sense Amplifier Inputs row from Electrical Characteristics 8
- Changed description of R_{OPEN_CELL} in Electrical Characteristics from "Impedance..." to "Minimum impedance..." and changed value 8
- Changed maximum ΔV_{OV} threshold accuracies from 40 mV to 50 mV and from 65 mV to 75 mV 8
- Changed text of "This current is sufficient..." note following Electrical Characteristics 8
- Changed values for V_{CHG_DET1} 9
- Deleted Internal Oscillator section 10
- Changed fir9.7 0 Td (3)Tj 0 0...OPEN_CELLsectio 63.72 0 T22 0 TdF2 6 Tf

- Minor text changes to Separate CHG(–) and DSG(–) Return Paths With Both FETs section 33
- Changed "PACK(+) positive terminal" to "most-positive cell input" in the 4 to 10 Series Cell Configuration section 36
- Deleted a phrase from the last paragraph of the Ship-Mode Equivalent Functionality section 37
- Deleted text from second bullet in list of Device Addressing and Protocol Overview section 37
- Deleted text from note following Memory Map table 39
- Corrected Charge Short-Circuit Delay for SCCD[3:0] = 0010 48
- Deleted text in the paragraph following the table in the EEPROM Write Sequence section 50

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp

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