Single-Cell Protector for Li-Ion Batteries

Check for Samples: bq294602, bq294604

FEATURES

- **Single-Cell Monitor for Secondary Protection**
- **Fixed Programmable Delay Timer**
- **Fixed OVP Threshold**
  - **bq294602 = 4.35 V with 4-s Delay Timer**
  - **bq294604 = 4.35 V with 6.5-s Delay Timer**
  - **bq294622 = 4.45 V with 4-s Delay Timer**
  - **bq294624 = 4.45 V with 6.5-s Delay Timer**
  - **bq294682 = 4.225 V with 4-s Delay Timer**
  - **bq294684 = 4.225 V with 6.5-s Delay Timer**
- **High-Accuracy Overvoltage Protection: ± 10 mV**
- **Low Power Consumption I_{CC} 1 µA ($V_{CELL(ALL)} < V_{PROTECT}$)**
- **Low leakage current per cell input < 100 nA**
- **Small package footprint**
  - **6-pin SON**

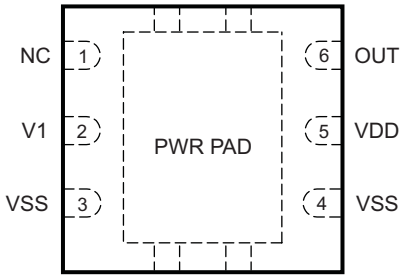
APPLICATIONS

- **2nd-Level Protection in Li-Ion Battery Packs in:**
  - **Tablets**
  - **Slates**
  - **Portable Equipment and Instrumentation**

DESCRIPTION

The bq2946xy family of products is a secondary level voltage monitor and protector for Li-Ion battery pack systems. The cell is monitored for over voltage condition and triggers an internal counter once the OVP threshold is exceeded and after a fixed set delay the out is transitioned to a high level. The output is reset (goes low) if the cell voltage drops below the set threshold minus the hysteresis.

DRV Package
(Top View)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS

PIN FUNCTIONS

bq2946xy	Pin Name	Type I/O	Description
1	NC	—	No Connection
2	V1	IA	Sense input for positive voltage of the cell
3	VSS	P	Electrically connected to IC ground and negative terminal of the cell
4	VSS	P	Electrically connected to IC ground and negative terminal of the cell
5	VDD	P	Power supply
6	OUT	OA	Output drive for external N-Channel FET
Thermal Pad	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed circuit board for proper operation

PIN DETAILS

Description

The method of overvoltage detection is comparing the cell voltage to an overvoltage protection threshold voltage V_{OV}. Once the cell voltage exceeds the programmed fixed value V_{OV}, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for 4 s for the bq294602 device. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if the cell input (V1) is below the OVP threshold minus the V_{HYS}.

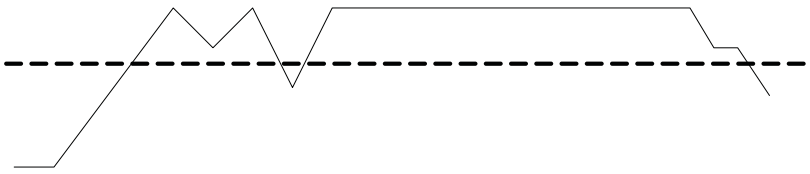


Figure 1. Timing for Overvoltage Sensing

Sense Positive Input for V1

This is an input to sense single battery cell voltage. A series resistor and a capacitor across the cell is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

The gate of an external N-Channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. The out will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

Thermal Pad, PWRPAD

For correct operation, the power pad (PWRPAD) is connected to the V_{SS} terminal on the printed circuit board.

FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V1–VSS	–0.3 to 8 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P_{TOT}		See package dissipation rating.
Functional temperature		–65 to 110°C
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}(1)		3		8	V
Input voltage range	V1–VSS	0		5	V
Operating ambient temperature range, TA		–40		110	°C

(1) See APPLICATION SCHEMATIC.

–8T. 11.3 1.8 T 40

DC CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 4 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 4 V (unless otherwise noted)

58 Tf 100 Tz 0 g f556e

Test	Symbol	Parameter					

to

to

TYPICAL CHARACTERISTICS

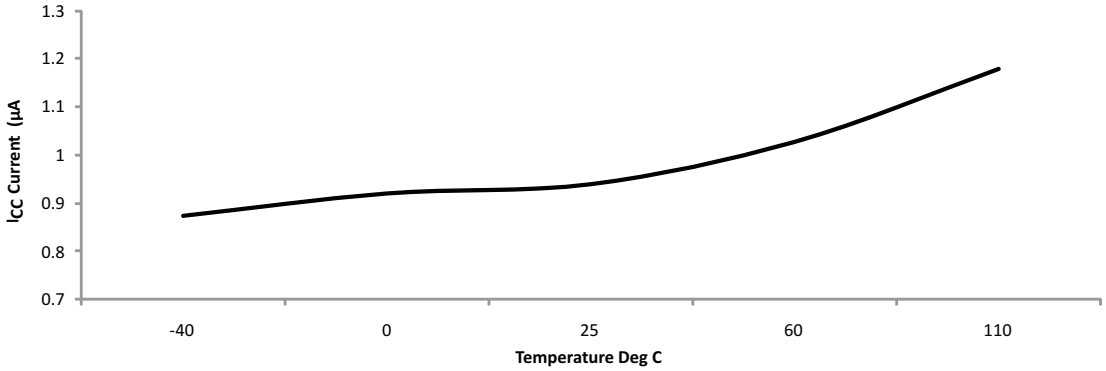


Figure 2. I_{CC} Current Consumption Versus Temperature

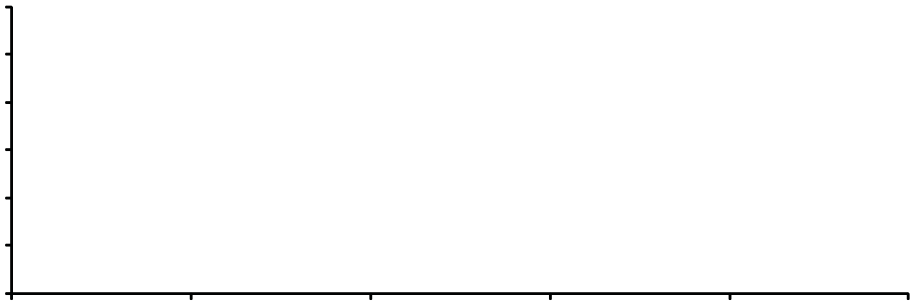


Figure 3. bq294602 Overvoltage Threshold (OVT) vs. Temp

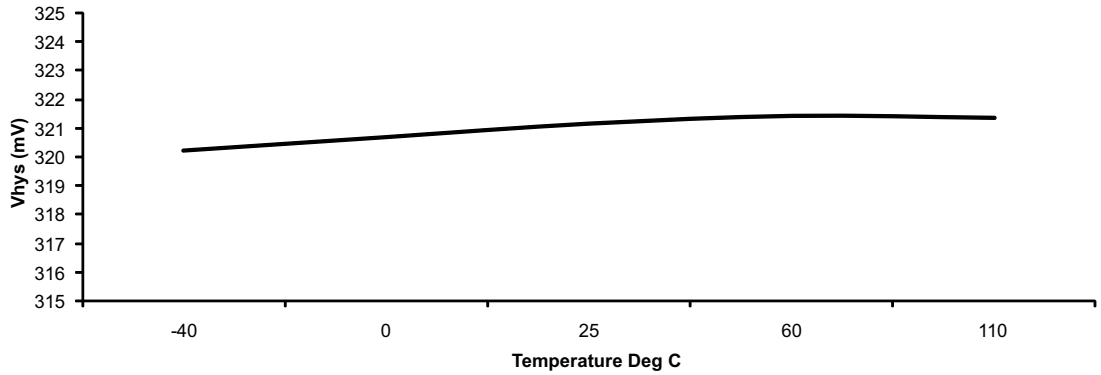


Figure 4. Hysteresis V_{HYS} Versus Temperature

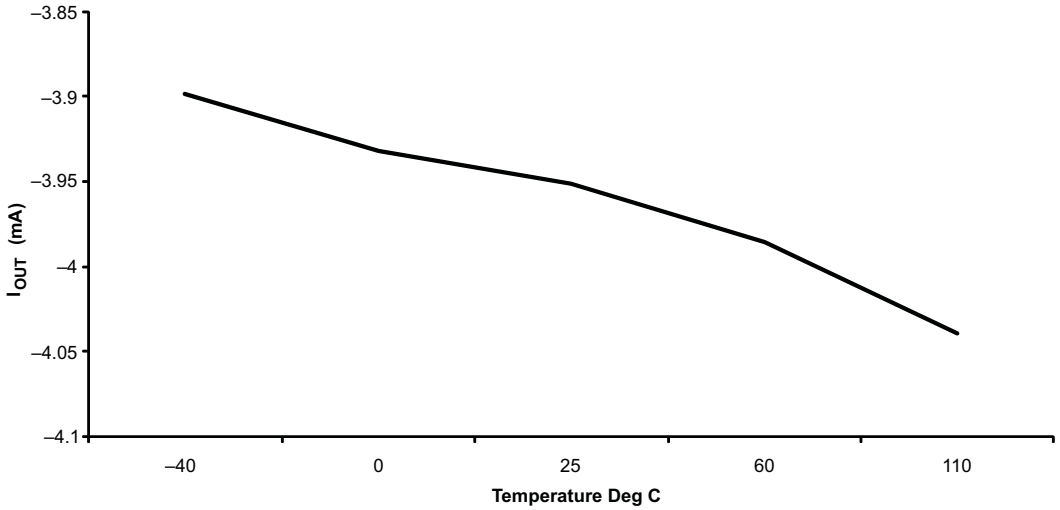


Figure 5. Output Current I_{OUT} Versus Temperature

APPLICATION INFORMATION

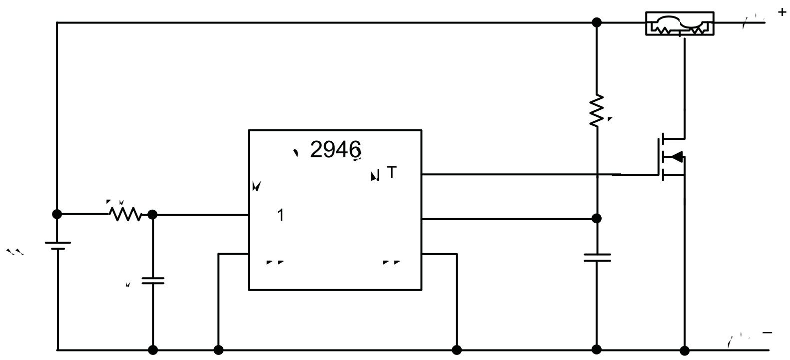


Figure 6. Application Configuration

NOTE

Connect VSS (Pins 3 and 4) externally to the CELL– terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 6 shows each external component.

Table 1. Parameters

PARAMETER	External Component	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01	0.1		µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

APPLICATION SCHEMATIC

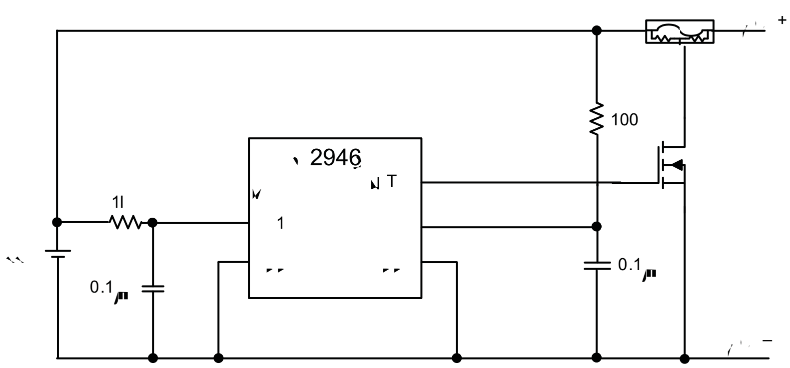


Figure 7. 1-Cell Configuration with Fixed Delay

NOTE

Connect VSS (Pins 3 and 4) externally to the CELL– terminal.

Product EandTSB32 10 Tf 100 Tz 0 0 0 rg 104.4 530 0 0 rrg 77.7 4048oldET BT z 0 77.7 404Link(s):11 Tf

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V1 (see Figure 8). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to V1 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltage for the cell voltage (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 8 shows the timing for the Customer Test Mode.

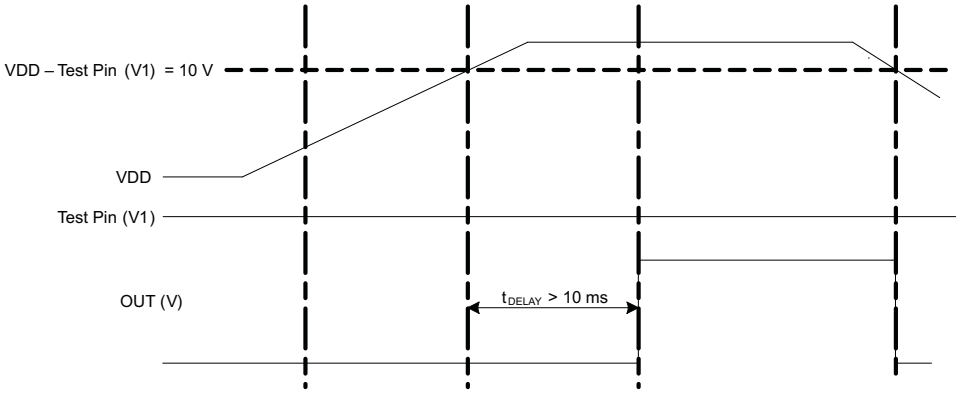


Figure 8. Timing for Customer Test Mode

Figure 9 shows the measurement for current consumption for the product for both VDD and Vx.

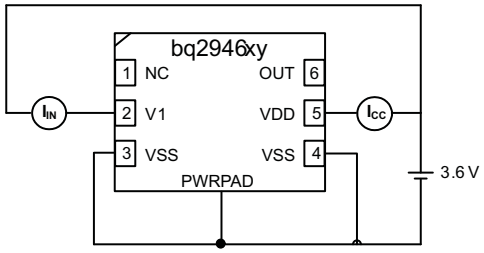


Figure 9. Configuration for IC Current Consumption Test

REVISION HISTORY

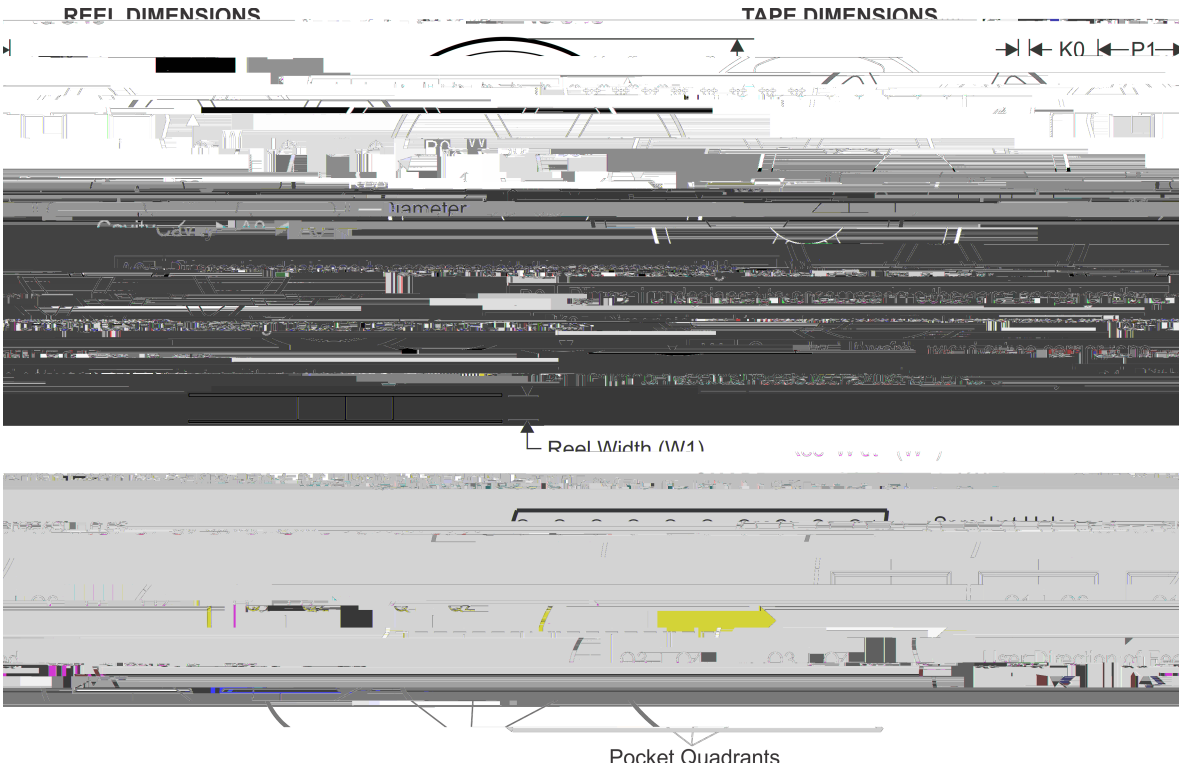
Changes from Original (December 2011) to Revision A	Page
• Added the bq294604 device into production.	2

Changes from Original (February 2012) to Revision B	Page
• Added a second I_{CC} Test Condition	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish

TAPE AND REEL INFORMATION



*All dimensions are nominal

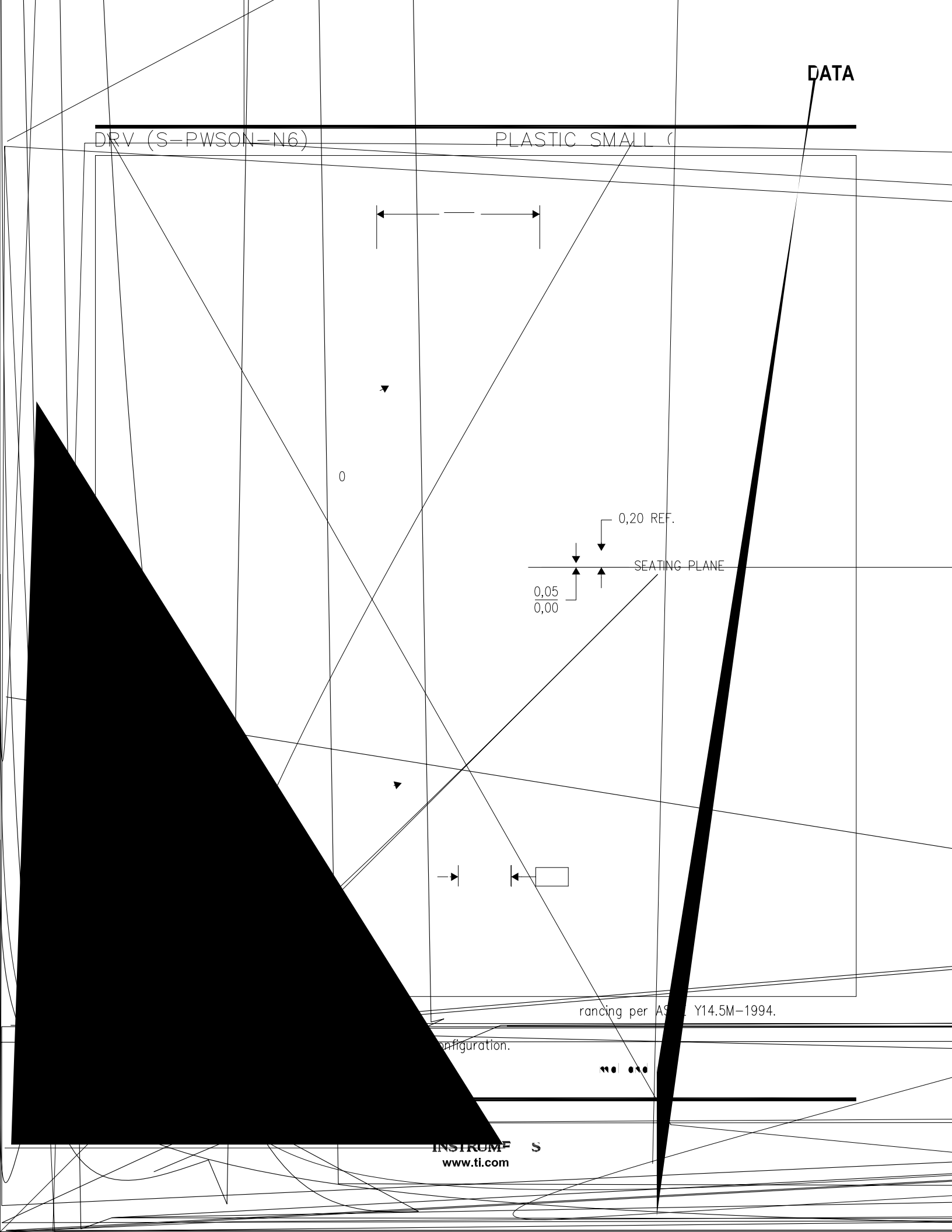
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294602DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294602DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294604DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294604DRVT	SON											

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294602DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294602DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294604DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294604DRVT	SON	DRV	6	250	210.0	185.0	35.0

DRV (S-PWSON-N6) PLASTIC SMALL (



ranging per AS Y14.5M-1994.

onfiguration.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

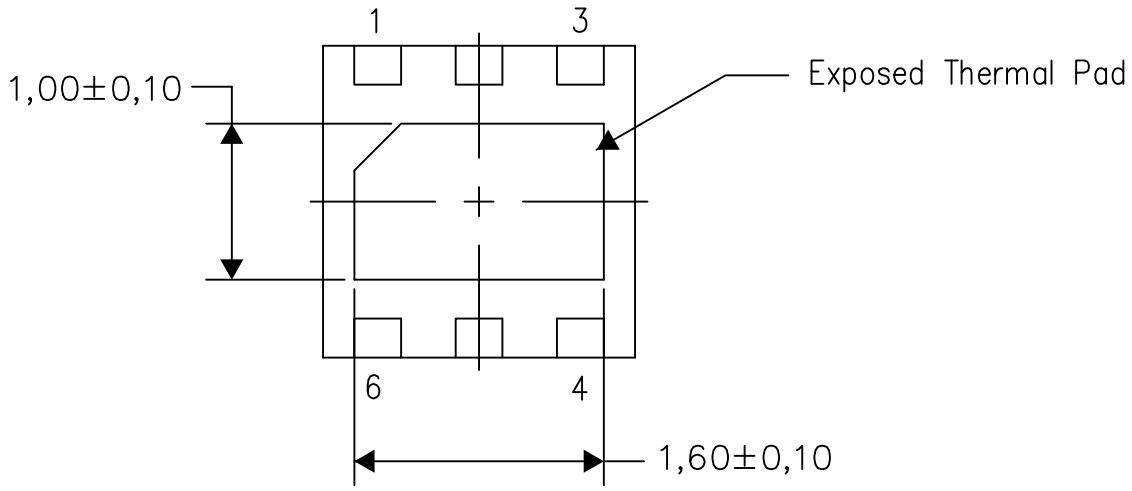
s package incorporates an exposed thermal pad that is designed to be attached directly to an external

must be soldered directly to the printed circuit board (PCB). After soldering, the
directly to the appropriate copper plane shown in c can be attached

integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

C. Publication IPC–7351 is recommended for alternate designs.

for specific thermal information, via requirement

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