2-Series, 3-Series, and 4-Series Li-Ion Battery Pack Manager

Check for Samples: bq3055

FEATURES

- **Fully Integrated 2-Series, 3-Series, and 4-Series Li-Ion or Li-Polymer Cell Battery Pack Manager and Protection**
- **Advanced Compensated End-of-Discharge Voltage (CEDV) Gauging**
- **High Side N-CH Protection FET Drive**
- **Integrated Cell Balancing**
- **Low Power Modes**
  - **Low Power: < 180 μA**
  - **Sleep < 76 μA**
- **Full Array of Programmable Protection Features**
  - **Voltage**
  - **Current**
  - **Temperature**
- **Sophisticated Charge Algorithms**
  - **JEITA**
  - **Enhanced Charging**
  - **Adaptive Charging**
- **Supports Two-Wire SMBus v1.1 Interface**
- **SHA-1 Authentication**
- **Compact Package: 30-Lead TSSOP**

APPLICATIONS

- **Notebook/Netbook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq3055 device is a fully integrated, single-chip, pack-based solution that provides a rich array of features for gas gauging, protection, and authentication for 2-series, 3-series, and 4-series cell Li-Ion and Li-Polymer battery packs.

Using its integrated high-performance analog peripherals, the bq3055 device measures and maintains an accurate record of available capacity, voltage, current, temperature, and other critical parameters in Li-Ion or Li-Polymer batteries, and reports this information to the system host controller over an SMBus v1.1 compatible interface.

The bq3055 provides software-based 1st-level and 2nd-level safety protection for overvoltage, undervoltage, overtemperature, and overcharge conditions, as well as hardware-based protection for overcurrent in discharge and short circuit in charge and discharge conditions.

SHA-1 authentication with secure memory for authentication keys enables identification of genuine battery packs beyond any doubt.

The compact 30-lead TSSOP package minimizes solution cost and size for smart batteries while providing maximum functionality and safety for battery gauging applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING INFORMATION[(1)]	
					TUBE[(2)]	TAPE AND REEL[(3)]
–40°C to 85°C	bq3055	TSSOP-30	DBT	bq3055	bq3055DBT	bq3055DBTR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of the document, or see the TI website at www.ti.com.
(2) A single tube quantity is 50 units.
(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

THERMAL METRIC[(1)]		bq3055	UNITS
		TSSOP	
		30 PINS	
$\theta_{JA, High K}$	Junction-to-ambient thermal resistance[(2)]	73.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance [(3)]	17.5	
θ_{JB}	Junction-to-board thermal resistance [(4)]	34.5	
ψ_{JT}	Junction-to-top characterization parameter [(5)]	0.3	
ψ_{JB}	Junction-to-board characterization parameter [(6)]	30.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance [(7)]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

TYPICAL IMPLEMENTATION

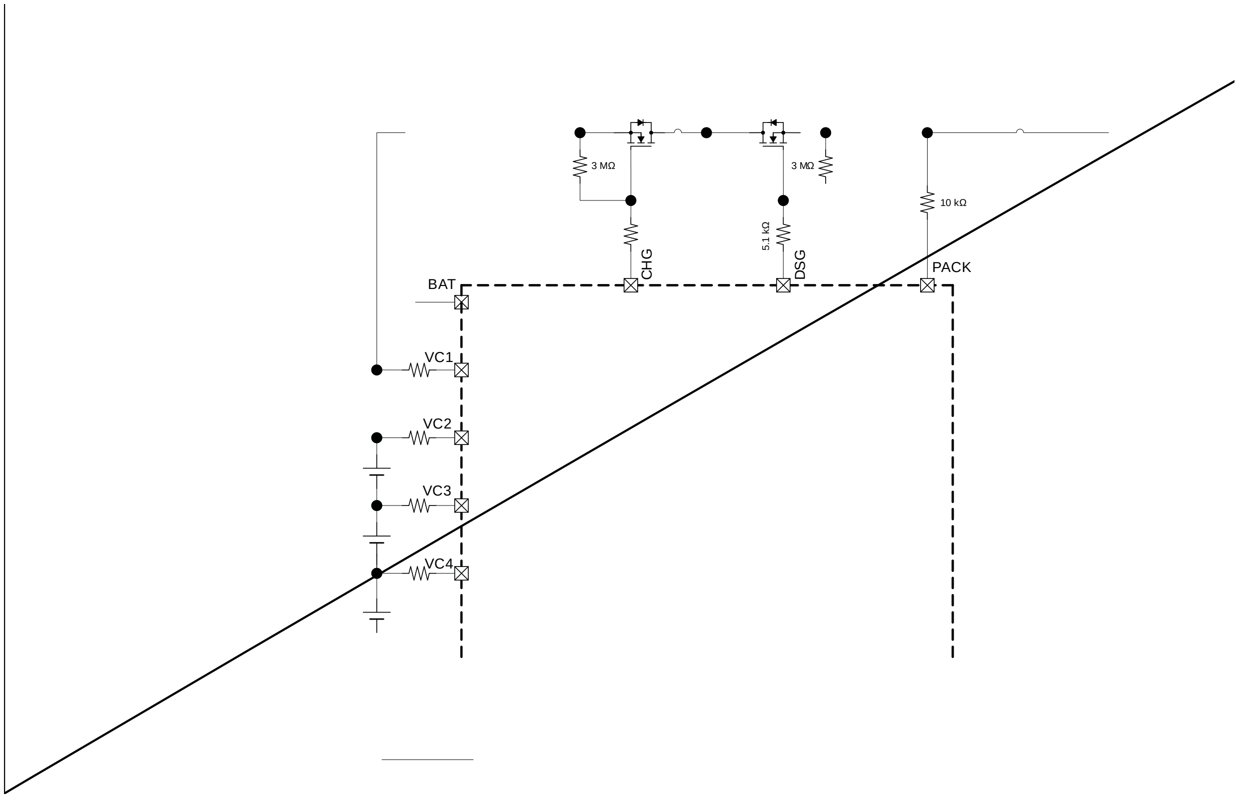
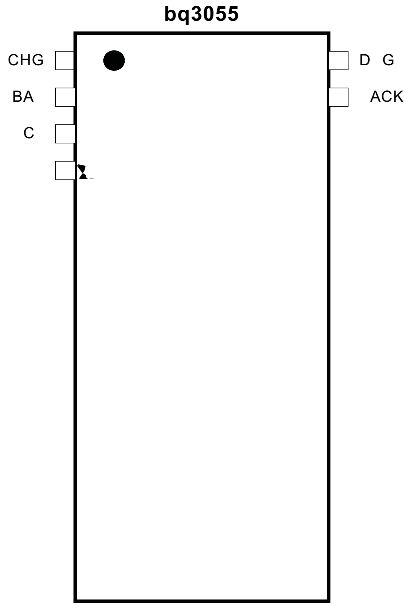


Figure 1. bq3055 Implementation


bq3055
CHG
BA
C
D G
ACK

RECOMMENDED OPERATING CONDITIONS (continued)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	VC1, BAT	V_{VC2}		V_{VC2} + 5.0	V
		VC2	V_{VC3}		V_{VC3} + 5.0	
		VC3	V_{VC4}		V_{VC4} + 5.0	
		VC4	V_{SRP}		V_{SRP} + 5.0	
		VCn – VC(n+1), (n=1, 2, 3, 4)	0		5.0	
		PACK			25	
		SRP to SRN	–0.2		0.2	V
C_{REG33}	External 3.3V REG capacitor		1			µF
C_{REG25}	External 2.5V REG capacitor		1			µF
T_{OPR}	Operating temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS: Supply Current

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Normal	CHG on, DSG on, no Flash write		410		µA
	Sleep	CHG on, DSG on, no SBS communication		160		µA
		CHG off, DSG off, no SBS communication		80		µA
	Shutdown				1	µA

ELECTRICAL CHARACTERISTICS: Power On Reset (POR)

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT–}$	Negative-going voltage input	At REG25	1.9	2.0	2.1	V
V_{HYS}	POR Hysteresis	At REG25	65	125	165	mV

ELECTRICAL CHARACTERISTICS: WAKE FROM SLEEP

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{WAKE}	V_{WAKE} Threshold	V_{WAKE} = 1.2 mV	0.2	1.2	2.0	mV
		V_{WAKE} = 2.4 mV	0.4	2.4	3.6	
		V_{WAKE} = 5 mV	2.0	5.0	6.8	
		V_{WAKE} = 10 mV	5.3	10	13	
V_{WAKE_TCO}	Temperature drift of VWAKE accuracy			0.5		%/°C
t_{WAKE}	Time from application of current and wake of bq3055			0.2	1	ms

ELECTRICAL CHARACTERISTICS: RBI RAM Backup

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RBI)}$	RBI data-retention input current	VRBI > $V_{(RBI)MIN}$, VCC < VIT		20	1100	nA
		VRBI > $V_{(RBI)MIN}$, VCC < VIT, T_A= 0°C to 70°C			500	
$V_{(RBI)}$	RBI data-retention voltage		1			V

ELECTRICAL CHARACTERISTICS: 3.3V Regulator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG33}	Regulator output voltage	3.8 V < VCC or BAT ≤ 5 V, I_{CC} ≤4 mA	2.4		3.5	V
		5V < VCC or BAT ≤ 6.8 V, I_{CC} ≤13 mA	3.1	3.3	3.5	V
		6.8 V < VCC or BAT ≤ 20 V, I_{CC} ≤ 30 mA	3.1	3.3	3.5	V
I_{REG33}	Regulator output current		2			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		0.2		%
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		1	13	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, I_{REG33} = 2 mA		5	18	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, V_{REG33} = 3 V			70	mA
		VCC or BAT = 14.4 V, V_{REG33} = 0 V			33	

ELECTRICAL CHARACTERISTICS: 2.5V Regulator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage	I_{REG25} = 10 mA	2.35	2.5	2.55	V
I_{REG25}	Regulator Output Current		3			mA
$\Delta V_{(VDDTEMP)}$	Regulator output change with temperature	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		0.25		%
$\Delta V_{(VDDLINE)}$	Line regulation	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		1	4	mV
$\Delta V_{(VDDLOAD)}$	Load regulation	VCC or BAT = 14.4 V, I_{REG25} = 2 mA		20	40	mV
$I_{(REG33MAX)}$	Current limit	VCC or BAT = 14.4 V, V_{REG25} = 2.3 V			65	mA
		VCC or BAT = 14.4 V, V_{REG25} = 0 V			23	

ELECTRICAL CHARACTERISTICS: $\overline{PRES}$, SMBD, SMBC

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input	$\overline{PRES}$, SMBD, SMBC	2.0			V
V_{IL}	Low-level input	$\overline{PRES}$, SMBD, SMBC			0.8	V
V_{OL}	Low-level output voltage	SMBD, SMBC			0.4	V
C_{IN}	Input capacitance	$\overline{PRES}$, SMBD, SMBC		5		pF
I_{LKG}	Input leakage current	$\overline{PRES}$, SMBD, SMBC			1	μA
I_{WPU}	Weak Pull Up Current	$\overline{PRES}$, V_{OH} = V_{REG25} – 0.5 V	60		120	μA
$R_{PD(SMBx)}$	SMBC, SMBD Pull-Down	T_A = –40 to 100˚C	550	775	1000	kΩ

[redacted]

,V

PACK

–V

(DSG)

=V

O(FETONDSG)

[redacted]

ELECTRICAL CHARACTERISTICS: CHG, DSG FET Drive ... (unless otherwise noted) PARAMETER T

ELECTRICAL CHARA[redacted] COULOMB COUNTER

Typical values stated where TA = 2[redacted]C and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage ran[redacted]	SRP – SRN	–0.20		0.25	V
	Conversion time	Single conversion		250623ET2028.6Tf1Ô84ve/657Td (±)Tj2 0 Td (and		
	Resolution (no missing codes)	Post	16			Bits
	Effective resolution	Single conversion, signed	15			Bits
10	Offset error	Post calibrated		10		µV
	Offset error conversion,					

VCC error min,

Effective

MIN SRN e/657 Td (±)Ti7.0 rg 435 ƒ74 0 Td (error)Tj 19Tj 24.63 j 11.21 0 Td (Mn,)Tj 43.438.9 604.2 Td (10)Tj ET BT /77Td (misFull-sd (e8 Td (A62 /F2 8 Tf 100 Tz 0 0 0 r

ELECTRICAL CHARACTERISTICS: Internal Thermal Shutdown

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{MAX2}	Maximum REG33 temperature		125		175	
$T_{RECOVER}$	Recovery hysteresis temperature			10		°C
$t_{PROTECT}$	Protection time			5		µs

ELECTRICAL CHARACTERISTICS: High Frequency Oscillator

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency of CPU Clock			4.194		MHz
$f_{(EIO)}$	Frequency error(1)	T_A = –20°C to 70°C	–2%	±0.25%	2%	

ELECTRICAL CHARACTERISTICS: OCD Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OCD detection threshold voltage range, typical	RSNS = 0	50		200	mV
		RSNS = 1	25		100	mV
$\Delta V_{(OCDT)}$	OCD detection threshold voltage program step	RSNS = 0		10		mV
		RSNS = 1		5		mV
$V_{(OFFSET)}$	OCD offset		–10		10	mV
$V_{(Scale\_Err)}$	OCD scale error		–10		10	%
$t_{(OCDD)}$	Over Current in Discharge Delay		1		31	ms
$t_{(OCDD\_STEP)}$	OCDD Step options			2		ms
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD1 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC1)}$	SCD1 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD1T)}$	SCD1 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD1 offset		–10		10	mV
$V_{(Scale\_Err)}$	SCD1 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		915	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		1830	µs
$t_{(SCD1D\_STEP)}$	SCD1D Step options	AFE.STATE_CNTL[SCDDx2] = 0		61		µs
		AFE.STATE_CNTL[SCDDx2] = 1		122		µs
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCD2 Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SDC2)}$	SCD2 detection threshold voltage range, typical	RSNS = 0	100		450	mV
		RSNS = 1	50		225	mV
$\Delta V_{(SCD2T)}$	SCD2 detection threshold voltage program step	RSNS = 0		50		mV
		RSNS = 1		25		mV
$V_{(OFFSET)}$	SCD2 offset		–10		10	mV
$V_{(Scale\_Err)}$	SCD2 scale error		–10		10	%
$t_{(SCD1D)}$	Short Circuit in Discharge Delay	AFE.STATE_CNTL[SCDDx2] = 0	0		458	µs
		AFE.STATE_CNTL[SCDDx2] = 1	0		915	µs
$t_{(SCD2D\_STEP)}$	SCD2D Step options	AFE.STATE_CNTL[SCDDx2] = 0		30.5		µs
		AFE.STATE_CNTL[SCDDx2] = 1		61		µs
$t_{(DETECT)}$	Current fault detect time	VSRP – SRN = VTHRESH + 12.5 mV			160	µs
t_{ACC}	Over Current and Short Circuit delay time accuracy	Accuracy of typical delay time	–20		20	%

ELECTRICAL CHARACTERISTICS: SCC Current Protection

Typical values stated where TA = 25ºC and VCC = 14.4 V, Min/Max values stated where T_A= –40ºC to 85ºC and VCC = 3.8 V to 25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SCCT)}$	SCC detection threshold voltage range, typical	RSNS = 0	–100		–300	mV
		RSNS = 1	–50		–225	mV
$\Delta V_{(SCCDT)}$	SCC detection threshold voltage program step	RSNS = 0		–50		mV
		RSNS = 1		–25		mV
$V_{(OFFSET)}$	SCC offset		–10		10	mV
$V_{(Scale\_Err)}$	SCC scale error		–10		10	%
$t_{(SCCD)}$	Short Circuit in Charge Delay		0		915	ms
$t_{(SCCD\_STEP)}$	SCCD Step options			61Tf 100 Tz1 100 Tz 0 0 0 rg 440.1 564.6 0 0 0 0		

10

Short

V

[illegible]

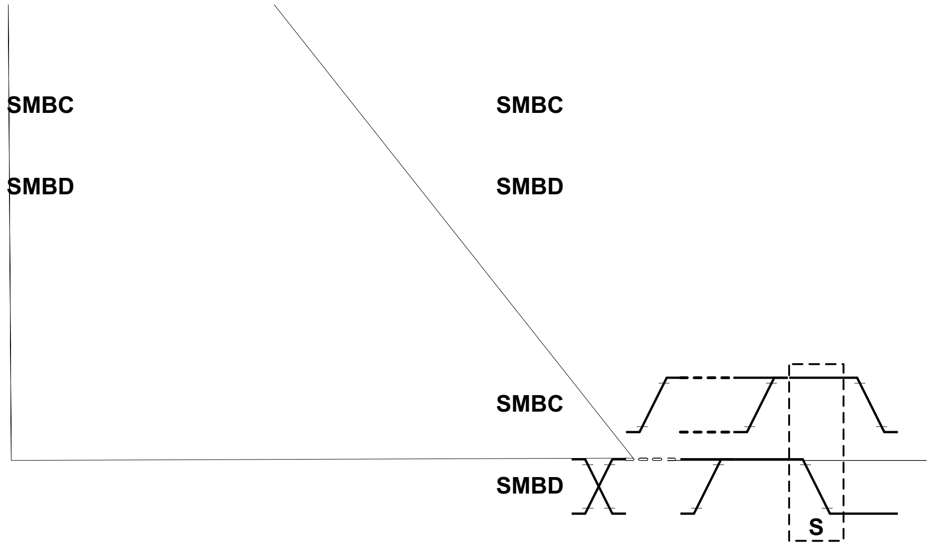


Figure 3. SMBus Timing Diagram

FEATURE SET

Primary (1st Level) Safety Features

The bq3055 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell Overvoltage/Undervoltage Protection
- Charge and Discharge Overcurrent
- Short-Circuit
- Charge and Discharge Over-Temperature
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq3055 can be used to indicate more serious faults via the FUSE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety Overvoltage
- Safety Overcurrent in Charge and Discharge
- Safety Over-Temperature in Charge and Discharge
- Charge FET, Discharge FET, and Pre-Charge FET Faults
- Cell Imbalance Detection
- Fuse Blow by Secondary Voltage Protection IC
- AFE Register Integrity Fault (AFE_P)
- AFE Communication Fault (AFE_C)

Charge Control Features

The bq3055 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Reduce the charge difference of the battery cells in fully charged state of the battery pack gradually using a voltage-based cell balancing algorithm during charging. A voltage threshold can be set up for cell balancing to be active. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms

Gas Gauging

The bq3055 uses the CEDV algorithm to measure and calculate the available capacity in battery cells. The bq3055 accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq3055 estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature. See the *bq3055 Technical Reference Manual* (SLUU440) for further details.

Lifetime Data Logging Features

The bq3055 offers limited lifetime data logging for the following critical battery parameters:

- Lifetime Maximum Temperature
- Lifetime Minimum Temperature

- Lifetime Maximum Battery Cell Voltage
- Lifetime Minimum Battery Cell Voltage

Authentication

- The bq3055 supports authentication by the host using SHA-1.
- SHA-1 authentication by the gas gauge is required for unsealing and full access.

Power Modes

The bq3055 supports three power modes to reduce power consumption:

- In Normal Mode, the bq3055 performs measurements, calculations, protection decisions, and data updates in 0.25-second intervals. Between these intervals, the bq3055 is in a reduced power stage.
- In Sleep Mode, the bq3055 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq3055 is in a reduced power stage. The bq3055 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In Shutdown Mode, the bq3055 is completely disabled.

Configuration

Oscillator Function

The bq3055 fully integrates the system oscillators and does not require any external components to support this feature.

System Present Operation

The bq3055 checks the $\overline{\text{PRES}}$ pin periodically (1s). If $\overline{\text{PRES}}$ input is pulled to ground by the external system, the bq3055 detects this as system present.

2-, 3-, or 4-Cell Configuration

In a 2-cell configuration, VC1 is shorted to VC2 and VC3. In a 3-cell configuration, VC1 is shorted to VC2.

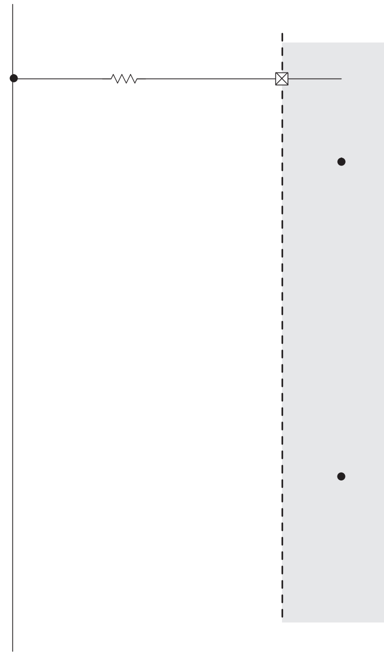
Cell Balancing

The device supports cell balancing by bypassing the current of each cell during charging or at rest. If the device's internal bypass is used, up to 10 mA can be bypassed and multiple cells can be bypassed at the same time. Higher cell balance current can be achieved by using an external cell balancing circuit. In external cell balancing mode, only one cell at a time can be balanced.

The cell balancing algorithm determines the amount of charge needed to be bypassed to balance the capacity of all cells.

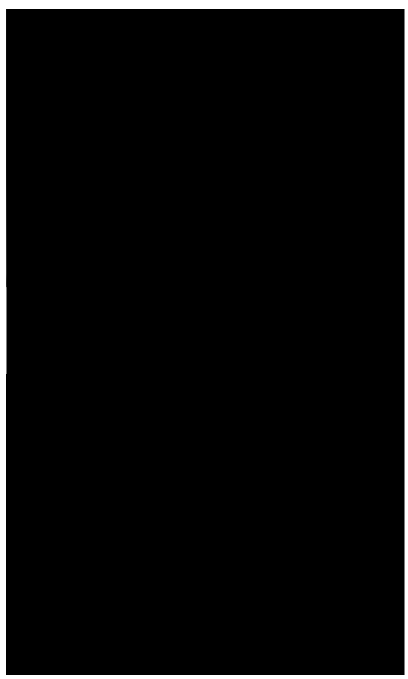
Internal Cell Balancing

When internal cell balancing is configured, the cell balance current is defined by the external resistor R_{VC} at the VCx input.



External Cell Balancing

When external cell balancing is configured, the cell balance current is defined by R_B. Only one cell at a time can be balanced.

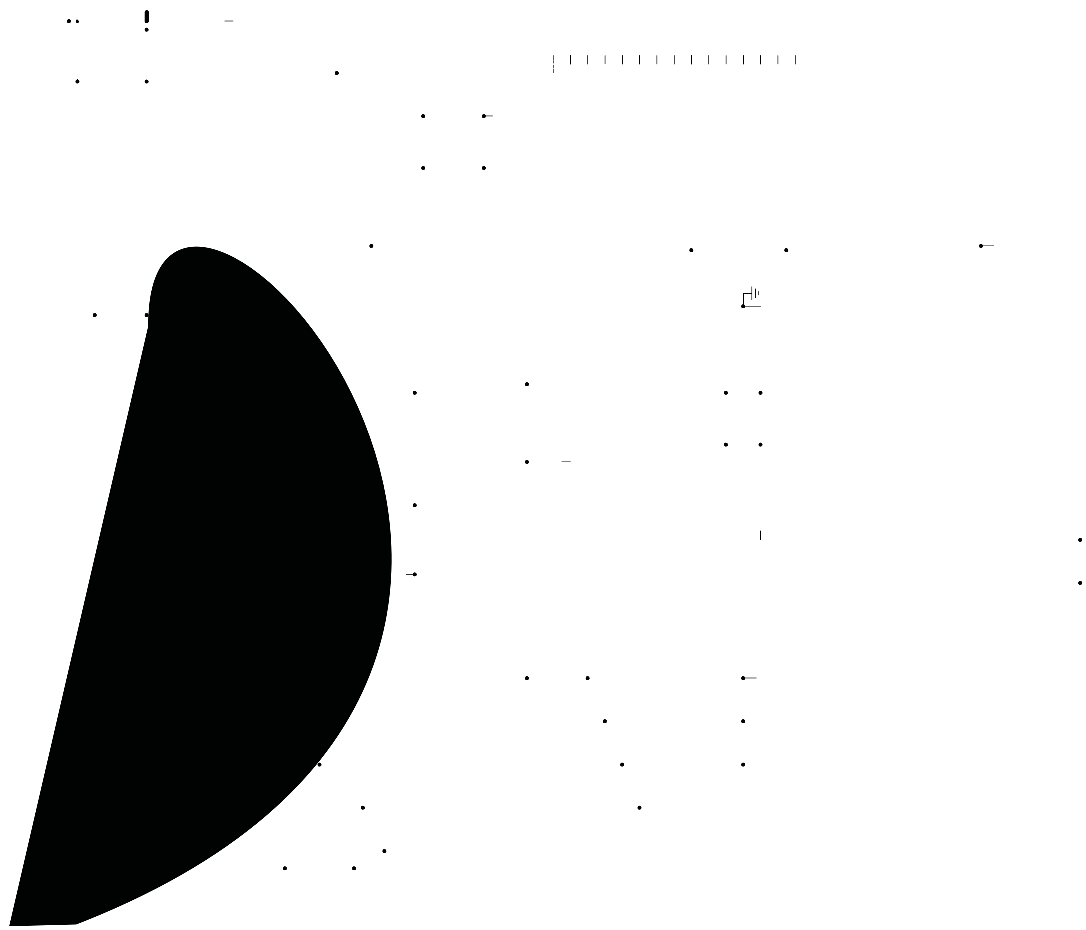


BATTERY PARAMETER MEASUREMENTS

Charge and Discharge Counting

The bq3055 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and

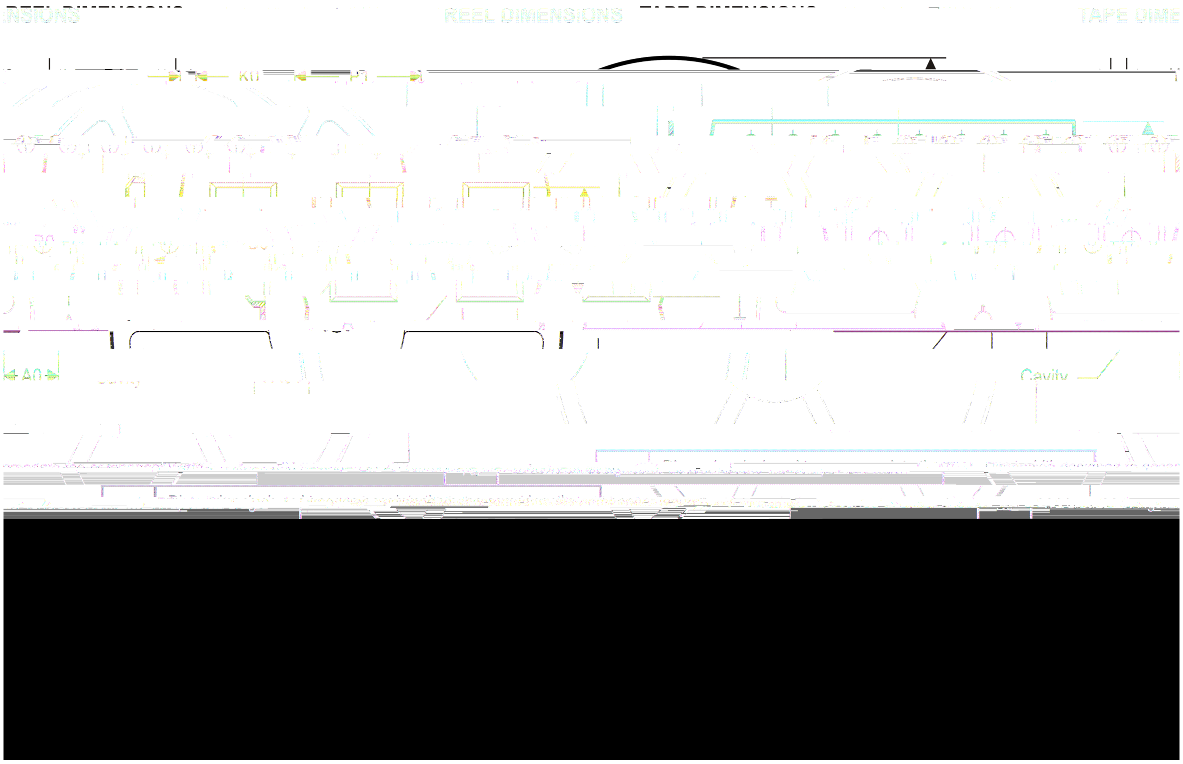
APPLICATE 6 . 8 P8 g8T2.7 6.E‹r rg 7.J4SCHEM g8C2 7 Tf 100 Tz 8 0 0 rg



PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples

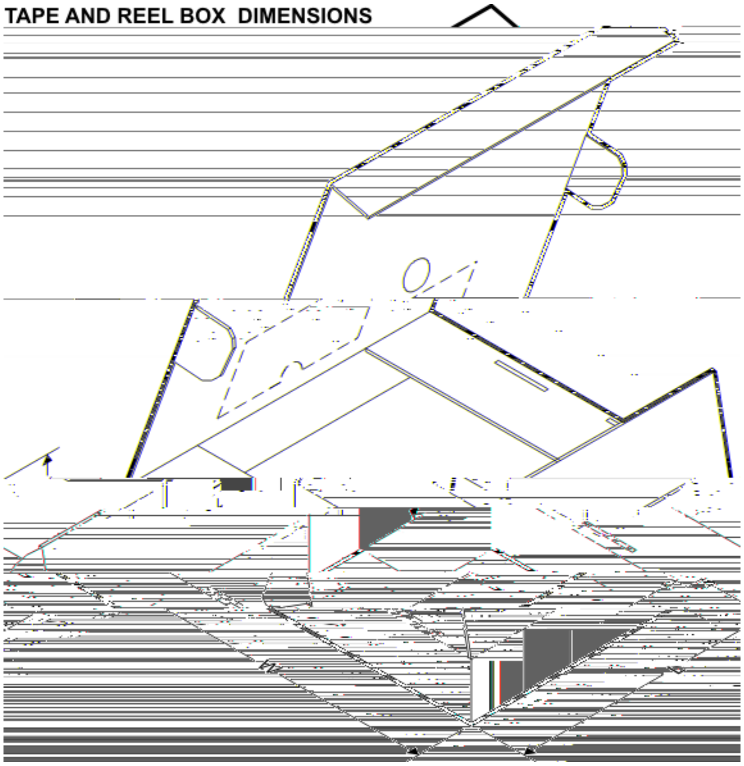
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ3055DBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0

IMPORTANT NOTICE