PowerLAN™ Master Gateway Battery Management Controller With PowerPump™ Cell Balancing Technology

Check for Samples: bq78PL116

FEATURES

- **bq78PL116 Designed for Managing 3- to 16-Series-Cell Battery Systems**
  - **Support for LCD and Electronic Paper Displays or EPDs**
  - **Configurable for 11-A, 26-A, or 110-A Operating Currents**
- **Systems With More Than Four Series Cells Require External bq76PL102 Dual-Cell Monitors**
- **SmartSafety Features:**
  - **Prevention: Optimal Cell Management**
  - **Diagnosis: Improved Sensing of Cell Problems**
  - **Fail Safe: Detection of Event Precursors**
- **Rate-of-Change Detection of All Important Cell Characteristics:**
  - **Impedance**
  - **Cell Temperature**
- **PowerPump Technology Transfers Charge Efficiently From Cell to Cell During All Operating Conditions, Resulting in Longer Run Time and Cell Life**
  - **Includes User-Configurable PowerPump Cell-Balancing Modes**
- **High-Resolution 18-Bit Integrating Delta-Sigma Coulomb Counter for Precise Charge-Flow Measurements and Gas Gauging**
- **Multiple Independent Δ-Σ ADCs: One-per-Cell Voltage, Plus Separate Temperature, Current, and Safety**
- **Simultaneous, Synchronous Measurement of Pack Current and Individual Cell Voltages**
- **Very Low Power Consumption**
  - **< 400 µA Active, < 185 µA Standby, < 85 µA Ship, and < 1 µA Undervoltage Shutdown**
- **Accurate, Advanced Temperature Monitoring of Cells and MOSFETs With up to 4 Sensors**
- **Fail-Safe Operation of Pack Protection Circuits: Up to Three Power MOSFETs and One Secondary Safety Output (Fuse)**
- **Fully Programmable Voltage, Current, Balance, and Temperature-Protection Features**
- **External Inputs for Auxiliary MOSFET Control**
- **Smart Battery System 1.1 Compliant via SMBus**

APPLICATIONS

- **Portable Medical Instruments and Test Equipment**
- **Mobility Devices (E-Bike)**
- **Uninterruptible Power Supplies and Hand-Held Tools**

DESCRIPTION

The bq78PL116 master gateway battery controller is part of a complete Li-Ion control, monitoring, and safety solution designed for large series cell strings.

The bq78PL116 along with bq76PL102 PowerLAN™ dual-cell monitors provide complete battery-system control, communications, and safety functions for a structure of three up to 16 series cells. This PowerLAN system provides simultaneous, synchronized voltage and current measurements using one A/D per-cell technology. This eliminates system-induced noise from measurements and allows the precise, continuous, real-time calculation of cell impedance under all operating conditions, even during widely fluctuating load conditions.

PowerPump technology transfers charge between cells to balance their voltage and capacity. Balancing is possible during all battery modes: charge, discharge, and rest. Highly efficient charge-transfer circuitry nearly eliminates energy loss while providing true real-time balance between cells, resulting in longer run-time and improved cycle life.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Temperature is sensed by up to 4 external sensors and one on-chip sensor. This permits accurate temperature monitoring of each cell individually. Firmware is then able to compensate for the temperature-induced effects on capacity, impedance, and OCV on a cell-by-cell basis, resulting in superior charge/ discharge and balancing control.

External MOSFET control inputs provide user- definable direct hardware control over MOSFET states. Smart control prevents excessive current through MOSFET body diodes. Auxiliary inputs can be used for enhanced safety and control in large multicell arrays.

The bq78PL116 is completely user-configurable, with parametric tables in flash memory to suit a variety of cell chemistries, operating conditions, safety controls, and data reporting needs. It is easily configured using the supplied bqWizard™ graphical user interface (GUI). The device is fully programmed and requires no algorithm or firmware development.

The bq78PL116 pin functions of LED1/SEG1–LED5/SEG5, PSH/BP/TP, and FIELD support LED, LCD, and electronic paper displays (EPDs). The user can configure the bq78PL116 for the desired display type.

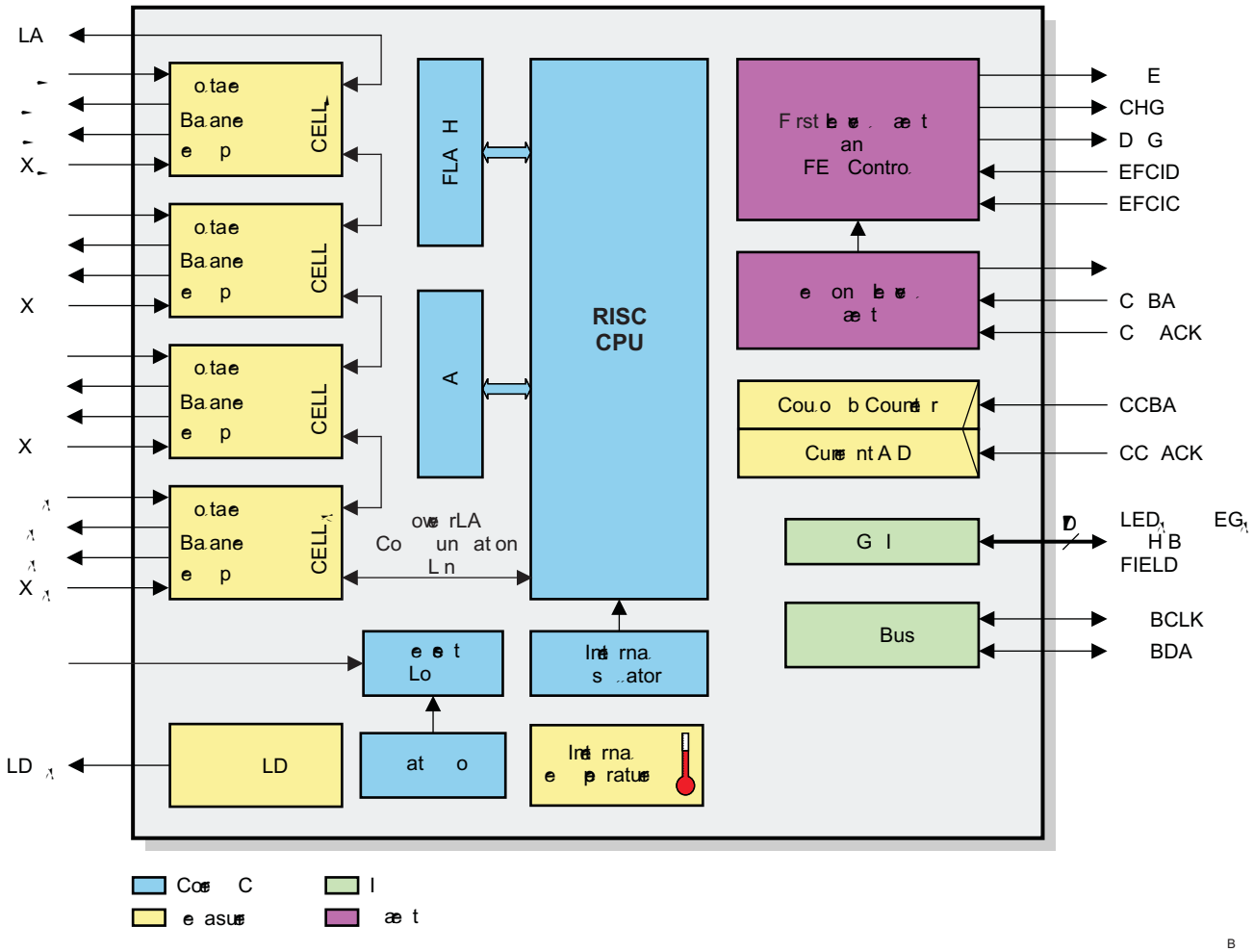


Figure 1. BQ78PL116 Internal Block Diagram

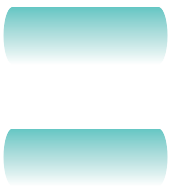
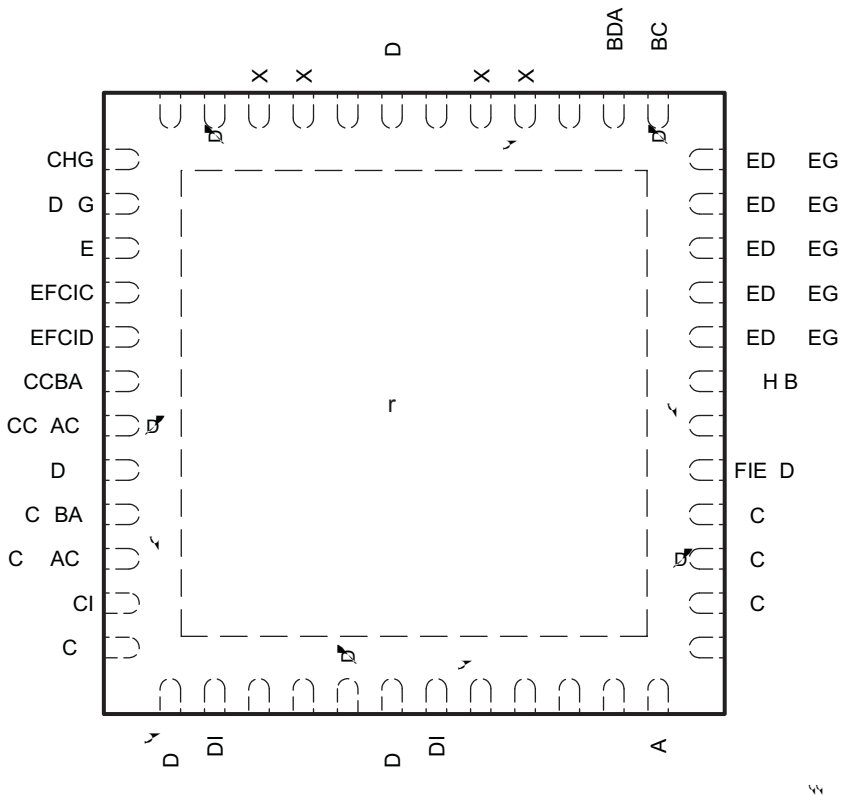


Figure 2. Example bq78PL116 System Implementation (12 Cells)

bq78PL116
RGZ Package
(Top View)



bq78PL116 TERMINAL FUNCTIONS (continued)

NAME	NO.	TYPE(1)	DESCRIPTION
FIELD	29	O	EPD field segment
LED1/SEG1	32	O	LED1 – open-drain, active-low, LCD and EPD segment 1
LED2/SEG2	33	O	LED2 – open-drain, active-low, LCD and EPD segment 2
LED3/SEG3	34	O	LED3 – open-drain, active-low, LCD and EPD segment 3
LED4/SEG4	35	O	LED4 – open-drain, active-low, LCD and EPD segment 4
LED5/SEG5	36	O	LED5 – open-drain, active-low, LCD and EPD segment 5
N/C	26, 27	IO	Connect 1-MΩ resistor to VSS
N/C	28	O	No connect
OSCI	11	I	External oscillator input (no connect, internal oscillator used)
OSCO	12	O	External oscillator output (no connect, internal oscillator used)
P1N	15	O	Charge-balance gate drive, cell 1 north
P2N	17	O	Charge-balance gate drive, cell 2 north
P2S	16	O	Charge-balance gate drive, cell 2 south
P3N	21	O	Charge-balance gate drive, cell 3 north
P3S	20	O	Charge-balance gate drive, cell 3 south
P4N	23	O	Charge-balance gate drive, cell 4 north
P4S	22	O	Charge-balance gate drive, cell 4 south
P-LAN	24	IO	PowerLAN I/O to external bq76PL102 nodes
PRE	3	O	Precharge MOSFET control (active-high)
PSH/BP/TP	31	IO	Pushbutton detect for LED display, LCD backplane, EPD top plane and charge pump
RSTN	25	I	Device reset, active-low
SDI1	14	I	Connect to SDO0 via a capacitor
SDI3	19	I	Internal PowerLAN connection – connect to SDO2 through a 0.01-µF capacitor
SDO0	13	O	Requires 100-kΩ pullup resistor to VLDO1
SDO2	18	O	Internal PowerLAN connection – connect to SDI3 through a 0.01-µF capacitor
SMBCLK	37	IO	SMBus clock signal
SMBDAT	38	IO	SMBus data signal
SPROT	30	O	Secondary protection output, active-high (FUSE)
V1	47	IA	Cell-1 positive input
V2	44	IA	Cell-2 positive input
V3	42	IA	Cell-3 positive input
V4	39	IA	Cell-4 positive input
VLDO1	8	P	Internal LDO-1 output, bypass with 10-µF capacitor to VSS
VLDO2	43	P	Internal LDO-2 output, bypass with 10-µF capacitor to V2
VSS	48	IA	Cell-1 negative input
XT1	rnal	LDO-1	

1

(1)Defaultsetting

Coulomb-Count Characteristics(1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			5		nVh
Intergral nonlinearity			0.008%		
Snap-to-zero (deadband)			±100(3)		µV

(1) Shares common input with current-sense section (CCBAT, CCPACK)
(2) After calibration. Accuracy is dependent on system calibration and temperature.
(3) Corresponds to ±10 mA with 10-mΩ sense resistor

Current-Sense (Safety) Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Measurement range		–0.312		0.312	V
Minimum					

SMBus Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low voltage		0		0.8	V
V_{IH}	Input high voltage		2.1		5.5	V
V_{OL}	Output low voltage	350-µA sink current	0		0.4	V
C_L	Capacitance, each I/O pin				10	pF
f_{SCL}	SCLK nominal clock frequency	T_A = 25°C	10	100	100	kHz
R_{PU}(2)	Pullup resistors for SCLK, SDATA	V_{BUS} 5 V nominal	13.3		45.3	kΩ
		V_{BUS} 3 V nominal	2.4	external	6.8	

(1) SMBus timing and signals meet the SMBus 2.0 specification requirements under normal operating conditions. All signals are measured with respect to PACK-negative.
(2) Pullups are typically implemented external to the battery pack and are selected to meet SMBus requirements.

PowerLAN Characteristics(1)(2)(3)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_L	Load capacitance	SDI1, SDI3, SDO0, SDO2, P-LAN			100	pF
V_{IH}	Input logic high	SDI1	0.8 VLDO1			V
		SDI3	0.8 VLDO2			
V_{OH}	Output logic high	SDO0, SDO2	0.9 VLDO1			V
		P-LAN	0.9 VLDO2			
V_{IL}	Input logic low	SDI1			0.2 VLDO1	V
		SDI3			0.2 VLDO2	
V_{OL}	Output logic low	SDO0, SDO2			0.1 VLDO1	V
		P-LAN			0.1 VLDO2	
$t_{r(I)}$	Input rise time	SDI1, SDI3			500	ns
$t_{f(I)}$	Input fall time	SDI1, SDI3			500	ns
t_C						

PowerPump Characteristics(1)

over free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High drive, P2S	I_{OUT} = –10 µA	0.9 V1			V
V_{OL}	Low drive, P2S	I_{OUT} = 200 µA			0.1 V1	V
V_{OH}	High drive, P1N, P2N	I_{OUT} = –200 µA	0.9 V1			V
V_{OL}	Low drive, P1N, P2N	I_{OUT} = 10 µA			0.1 V1	V
V_{OH}	High drive, P3S, P4S	I_{OUT} = –10 µA	0.9 V1			V
V_{OL}	Low drive, P3S, P4S	I_{OUT} = 200 µA			0.1 V1	V
V_{OH}	High drive, P3N, P4N	I_{OUT} = –200 µA	0.9 V1			V
V_{OL}	Low drive, P1N, P2N	I_{OUT} = 10 µA			0.1 V1	V
I_{OH}	Source current, P2S, P3S, P4S	V_{OH} = V1 – 0.8 V	250			µA
I_{OL}	Sink current, P1N, P2N, P3N, P4N	VOH = V1 + 0.2 V	–250			µA
t_r	Signal rise time	C_{Load} = 300 pF			100	ns
t_f	Signal FET fall time	C_{Load} = 300 pF			100	ns
f_P	Frequency			204.8		kHz
D	PWM duty cycle	P1N, P2N, P3N, P4N		33%		
		P2S, P3S, P4S		67%(2)		

(1) All parameters representative of a typical cell voltage of 3.6 V.
(2) Effective duty cycle is 33%. PxS pins are P-channel drives and MOSFET on-time is (1 – D).

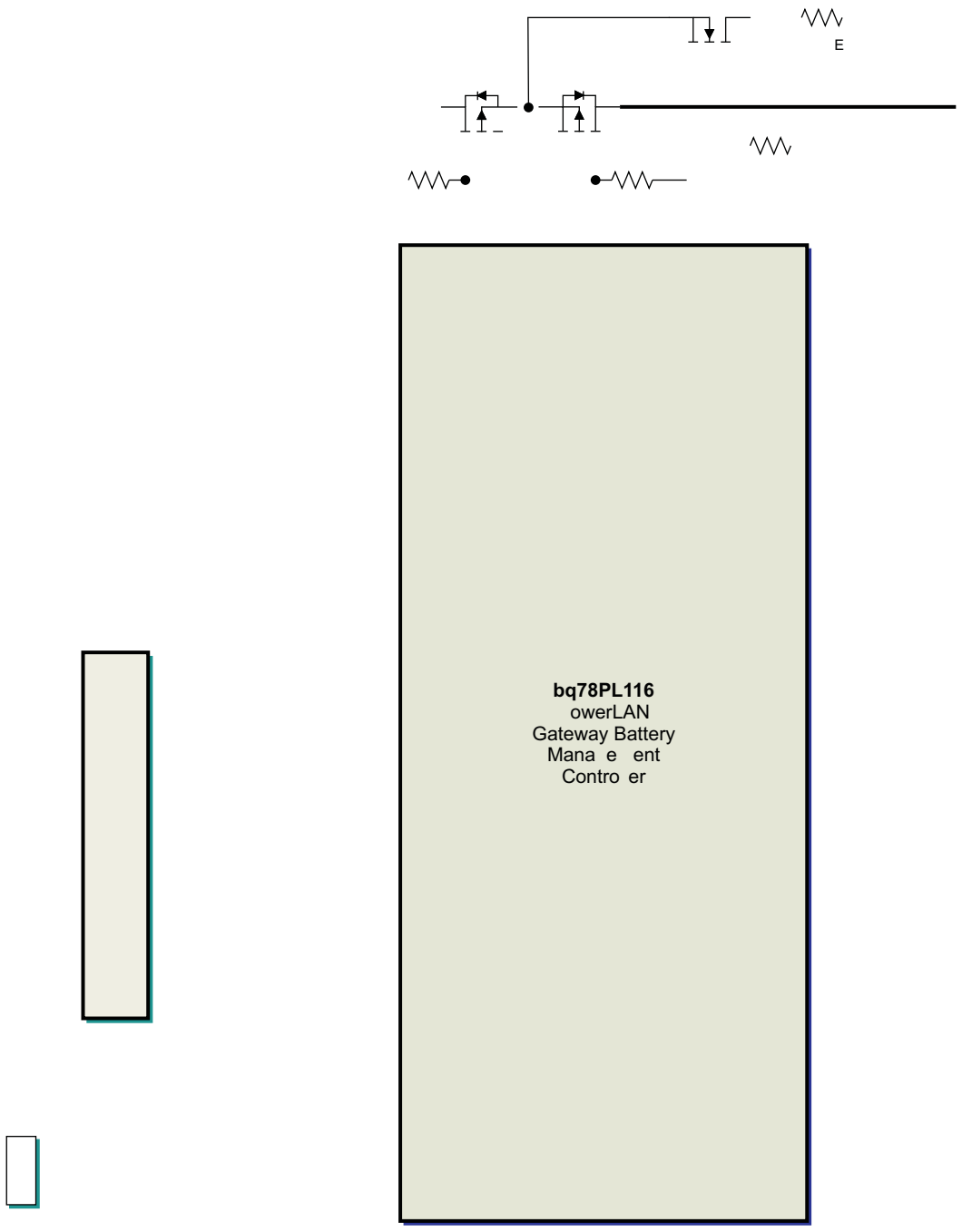


Figure 4. bq78PL116 Simplified Example Circuit Diagram

FEATURE SET

Primary (First-Level) Safety Features

The bq78PL116 implements a breadth of system protection features which are easily configured by the customer. First-level protections work by controlling the MOSFET switches. These include:

- Battery cell over/undervoltage protection
- Pack over/undervoltage protection
- Charge and discharge overcurrent protection
- Short-circuit protection
- External MOSFET control inputs (EFCIx) with programmable polarity
- Up to four external temperature inputs for accurate cell and MOSFET monitoring
- Watchdog timer protection
- Brownout detection and protection against extreme pack undervoltage

Secondary (Second-Level) Safety Features

The bq78PL116 can detect more serious system faults and activate the SPROT pin, which can be used to open an in-line chemical fuse to permanently disable the pack. Secondary optional features include

- Fully independent of first-level protections
- SmartSafety algorithms for early detection of potential faults
  - Temperature abnormalities (extremes, rate of change)
  - Cell imbalance exceeds safety limits
  - Impedance rise due to cell or weld strap fault
- MOSFET failure or loss of MOSFET control
- Safety overvoltage, pack and cell
- Safety overtemperature, limits for both charge and discharge
- Safety overcurrent, charge and discharge
- Failed current measurement, voltage measurement, or temperature measurement

Charge Control Features

- Meets SMBus 1.1 and Smart Battery System (SBS) Specification 1.1 requirements
- Active cell balancing using patented PowerPump technology, which eliminates unrecoverable capacity loss due to normal cell imbalance
- Simultaneous, synchronous measurement of all cell voltages in a pack
- Simultaneous, synchronous measurement of pack current with cell voltages
- Reports target charging current and/or voltage to an SBS Smart Charger
- Reports the chemical state-of-charge for each cell and pack
- Supports precharging and zero-volt charging with separate MOSFET control
- Programmable, Chemistry-specific parameters
- Fault reporting

Gas Gauging

- The bq78PL116 accurately reports battery cell and pack state-of-charge (SOC). No full charge/discharge cycle is required for accurate reporting.
- State-of-charge is reported via SMBus and optional display.
- 18-bit integrating delta-sigma ADC coulomb counter

Display Types

- The bq78PL116 drives a three- to five-segment LED display in response to a pushbutton (LEDEN) input signal. Each LED pin can sink up to 10 mA.
- The bq78PL116 drives a three- to five-segment static liquid-crystal display.
- The bq78PL116 drives a three- to five-segment electronic paper display. An external 15-V voltage source is required. E Ink Corporation supplies this type of display.

The display type is selected via the parameter set.

Lifetime Logging (Readable via SMBus)

- Lifetime delivered ampere-hours
- Last discharge average
- Lifetime maximum power
- Maximum/minimum temperature
- Maximum/minimum pack voltage
- Maximum/minimum cell voltage in a pack
- Maximum charge and discharge currents

Power Modes

- **Normal Mode:** The bq78PL116 performs measurements and calculations, makes decisions, and updates internal data approximately once per second. *All safety circuitry is fully functional in this mode.*
- **Standby Mode:** The bq78PL116 performs as in normal mode, but at a dramatically reduced rate to lower power consumption at times when the host computer is inactive or the battery system is not being used. *All safety circuitry remains fully functional in this mode.*
- **Ship Mode:** The bq78PL116 disables (opens) all the protection MOSFETs, and continues to monitor temperature and voltage, but at a reduced measurement rate to dramatically lower power consumption. Environmental data is saved in flash as a part of the historical record. *Safety circuitry is disabled in this mode*. The device does not enter this power state as a part of normal operation; it is intended for use after factory programming and test. Entry occurs only after a unique SMBus command is issued. Exit occurs when the SMBus lines return to an active state.
- **Extreme Cell Undervoltage (ECUV) Shutdown Mode:** In this mode, the bq78PL116 draws minimal current and the charge and discharge protection MOSFETs are disabled (opened). The precharge MOSFET remains enabled when a charge voltage is present. *Safety circuitry is disabled in this mode*. The device does not enter this mode as a part of normal operation; it enters this state during extreme cell undervoltage conditions (ECUV). The ECUV threshold is programmable between 2.5 V and 2.8 V for even series cell applications and 2.7 V to 2.8 V for odd series cell applications.

STATE	OVERCURRENT PROTECTION	ENTRY CONDITION	EXIT CONDITION
Active	Fully active	Normal operation as determined by firmware	Firmware directed to the following operating modes
Standby	Fully active	No load current flowing for predetermined time	Load activity
Ship	Not active	Protected SMBus command	SMBus becomes active
Extreme cell undervoltage	Not active (precharge enabled)	Enabled when Vcell < ECUV	Vcell charge above ECUV recovery threshold (2.9 V/cell typical)

OPERATION

The bq78PL116 battery-management controller serves as a master controller for a Li-Ion battery system consisting of up to 16 cells in series. Any number of cells may be connected in parallel; other system or safety issues limit the number of parallel cells. The bq78PL116 provides extraordinarily precise state-of-charge gas gauging along with first- and second-level pack safety functions. Voltage and current measurements are performed synchronously and simultaneously for all cells in the system, allowing a level of precision not previously possible in battery management. Temperature is measured by up to four additional external temperature sensors. Coulomb counting is captured continuously by a dedicated 18-bit integrating delta-sigma ADC in the bq78PL116. The CPU in the bq78PL116 is also responsible for system data calculations and communicating parameters via the SMBus interface.

PowerLAN Communication Link

PowerLAN technology is

A variety of techniques, such as simple terminal voltage, terminal voltage corrected for impedance and temperature effects, or state-of-charge balancing, is easily implemented by the bq78PL116. By tracking the balancing required by individual cells, overall

Electronic paper displays require an external power supply, typically 15 V, to power the display. In EPD, mode the bq78PL116 strobes the display outputs for a user- programmable period of milliseconds to drive a,

COMMUNICATIONS

SMBus

The bq78PL116 uses the industry-standard Smart Battery System's two-wire System Management Bus (SMBus) communications protocol for all external communication. SMBus version

Command	Data Type	Description
45	R/W word (unsigned)	Extended Data (Vcell 10)
46	R/W word (unsigned)	Extended Data (Vcell 11)
47	R/W word (unsigned)	Extended Data (Vcell 12)
48	R/W word (unsigned)	Extended Data (Vcell 13)
49	R/W word (unsigned)	Extended Data (Vcell 14)
4A	R/W word (unsigned)	Extended Data (Vcell 15)
4B	R/W word (unsigned)	Extended Data (Vcell 16)
4C	R/W word (unsigned)	Extended Data (Temp 0 – Intenal)
4D	R/W word (unsigned)	Extended Data (Temp 1 – Extenal)
4E	R/W word (unsigned)	Extended Data (Temp 2 – Extenal)
4F	R/W word (unsigned)	Extended Data (Temp 3 – Extenal)
50	R/W word (unsigned)	Extended Data (Temp 4 – Extenal)
51	R/W word (unsigned)	Extended Data (Safety Status)
52	R/W word (unsigned)	Extended Data (Permanent Fail Status)
53	R/W word (unsigned)	Extended Data (Charge Status)
54	R/W word (unsigned)	Extended Data (Lifetime Maximum Pack Voltage)
55	R/W word (unsigned)	Extended Data (Lifetime Maximum Cell Voltage)
56	R/W word (unsigned)	Extended Data (Lifetime Maximum Charge Current)
57	R/W word (unsigned)	Extended Data (Lifetime Maximum Discharge Current)
58	R/W word (unsigned)	Extended Data (Lifetime Maximum Temperature)
80	R/W word (unsigned)	Extended Command (Device Status)
81	R/W word (unsigned)	Extended Command (Device Command)

REFERENCE SCHEMATICS

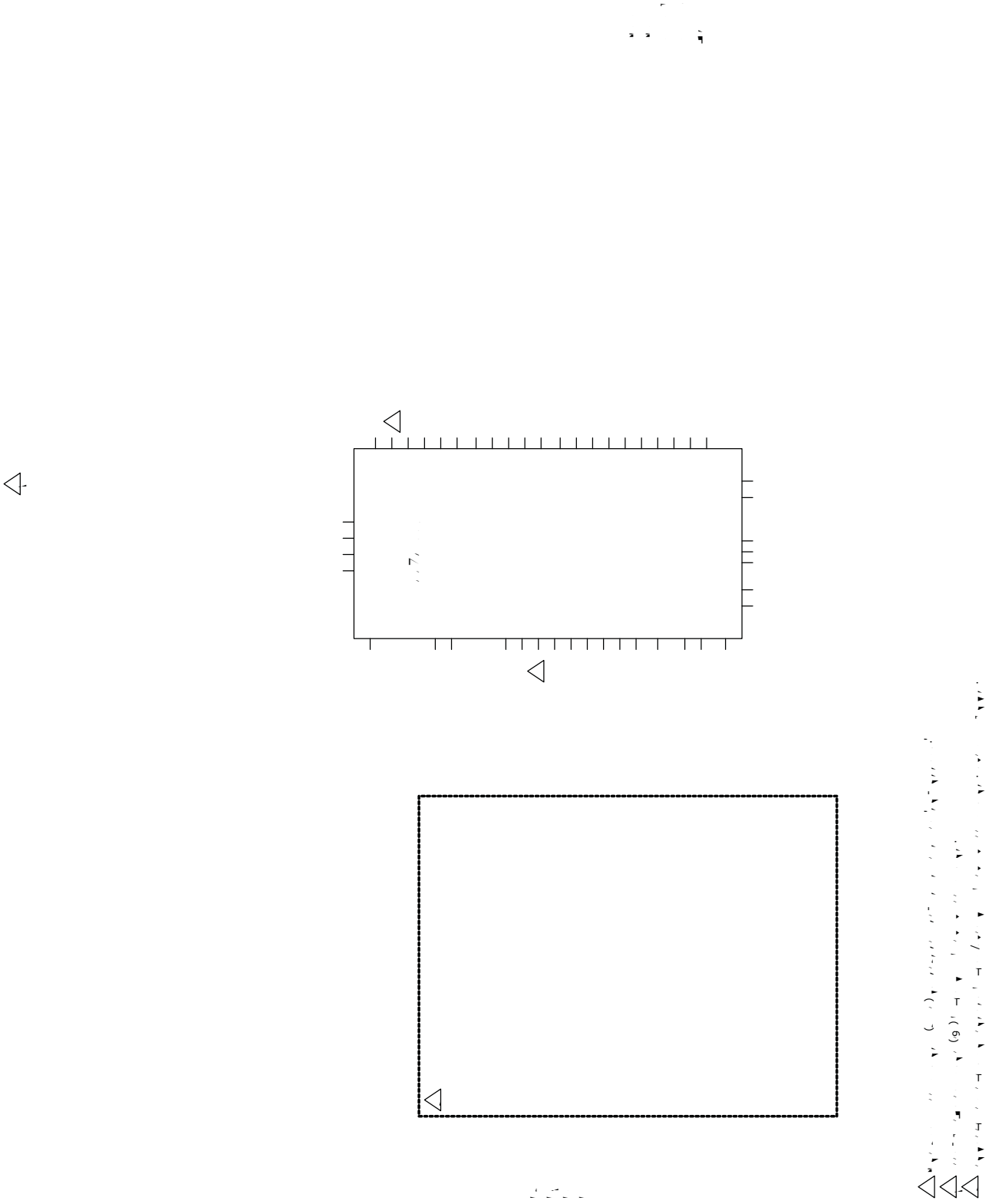


Figure 5. Typical 3S Application Schematic

Table 2. Bill of Materials for 3S Application (continued)

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
2	Q11-12		MOSFET P-Channel SMT -30VDS	SOIC-8	Fairchild	FDS6673
1	U1		PowerLAN Master Gateway Battery Management Controller	QFN48	Texas Instruments	bq78PL116RGZR
3	Z1-2 Z5	5.6V	Common Anode Zener Diode Pair 300mW	SOT-23	Standard	Standard
2	Z3-4	12V	Zener Diode 500mW	SOD-123	Diodes, Inc	BZT52C12-13-F
1	F1	12 Amp	Chemical Fuse For 2-3 Cells In Series		Sony	SFH-1212A
4	BATTERY+ BATTERY- PACK+ PACK-		2 Pin Connector		Standard	Standard
1	CELLS		4 Pin Connector		Standard	Standard
1	HOST		5 Pin Connector		Standard	Standard

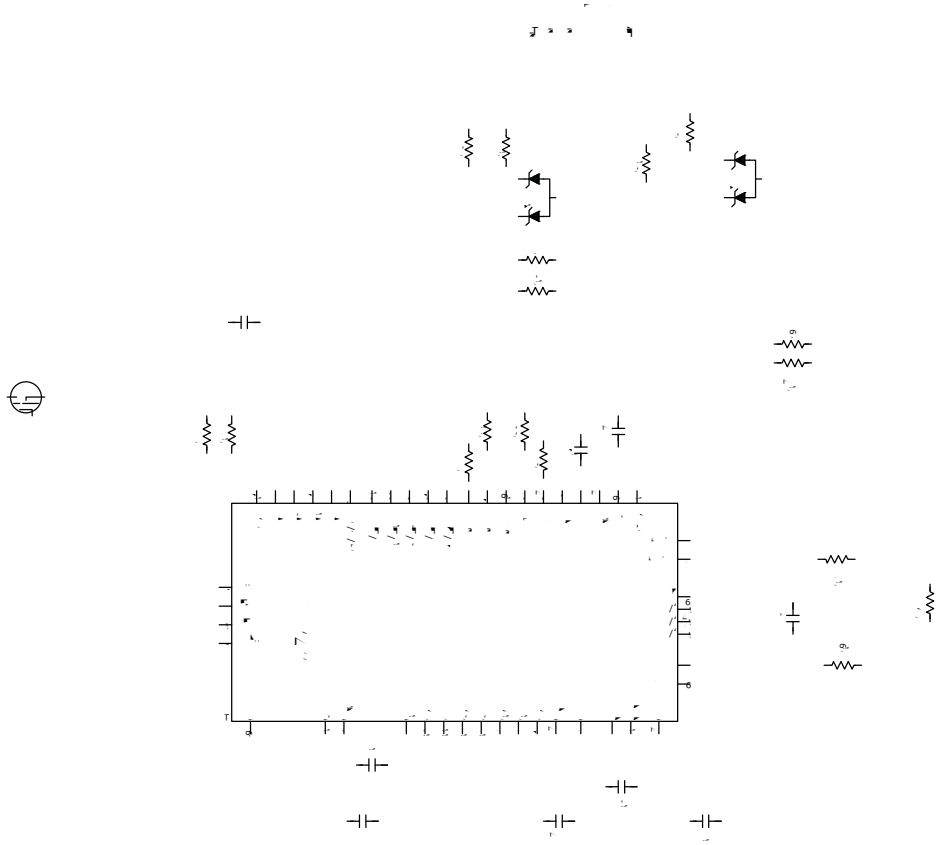


Figure 6. Typical 16S Application Circuit – bq78PL116 and FETs (Sheet 1 of 4)

Cells

Figure 7. Typical 16S Application Circuit – bq76PL102 for Cells 5–8 (Sheet 2 of 4)

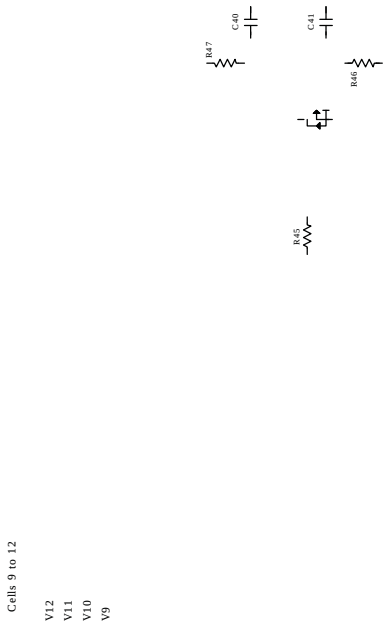


Figure 8. Typical 16S Application Circuit – bq76PL102 for Cells 9–12 (Sheet 3 of 4)

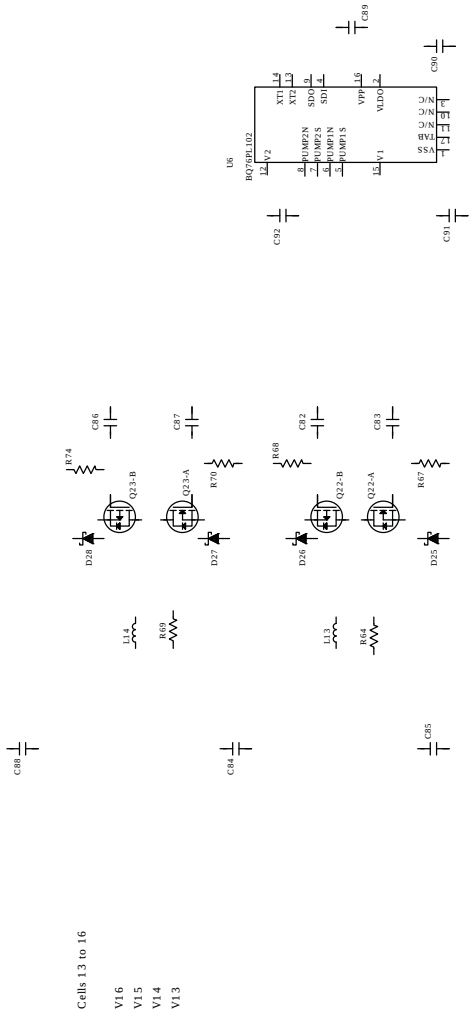


Figure 9. Typical 16S Application Circuit – bq76PL102 for Cells 13–16 (Sheet 4 of 4)

Table 3. Bill of Materials for 16S Application

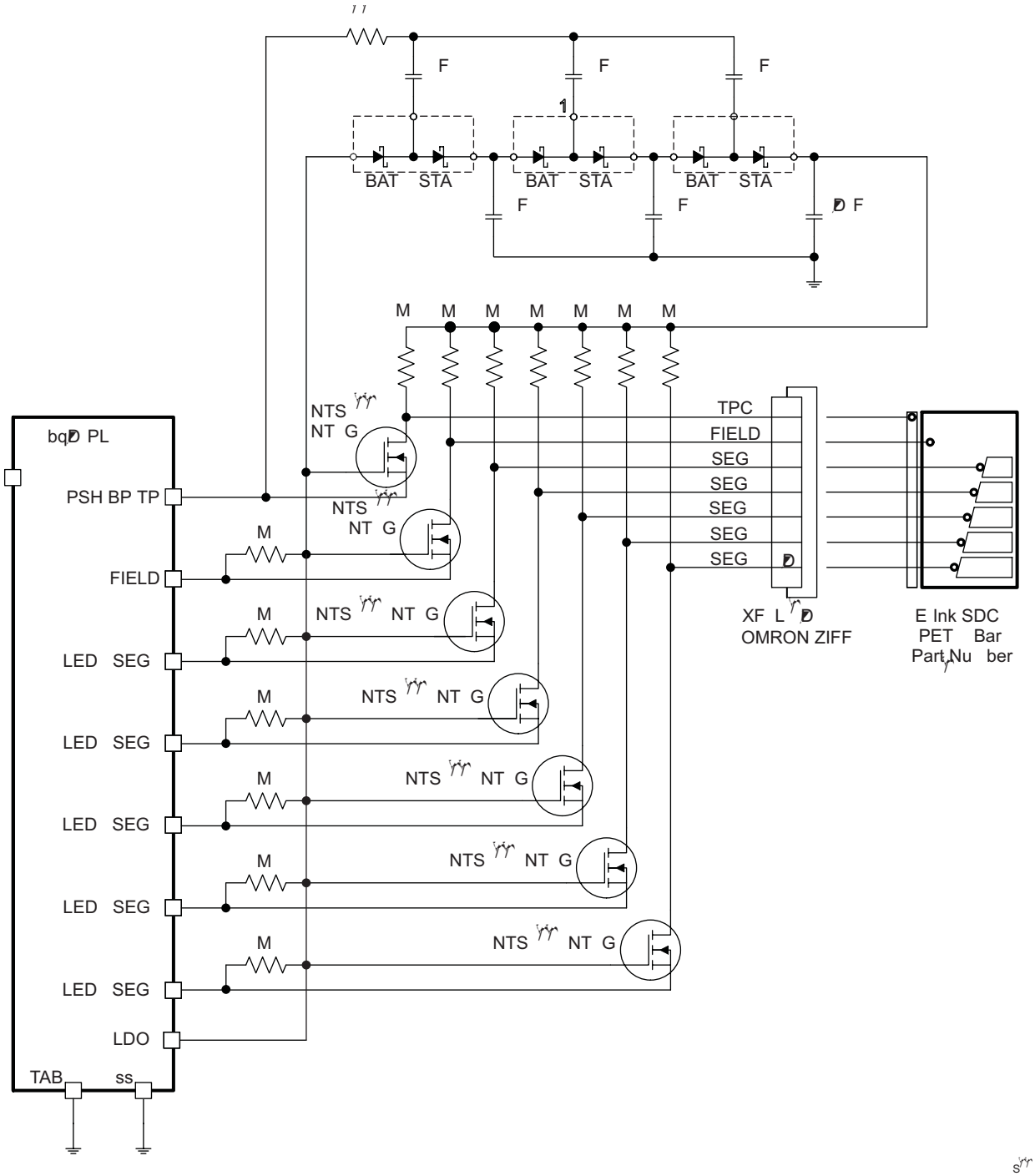
Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
6	U2-7	QFN-16	PowerLAN Dual Cell Monitor	QFN16	Texas Instruments	bq76PL102RGTT
1	U1	QFN-48	PowerLAN Master Gateway Battery Management Controller	QFN48	Texas Instruments	bq78PL116RGZR
24	C11 C18 C20 C23-24 C26 C48-50 C56-58 C69 C72 C74-77 C90-92 C99-101	10uF	Capacitor SMT Ceramic X5R +/-10% 6.3V	603	Standard	Standard
16	C1-3 C30 C32 C35 C39 C63-64 C78-81 C102-104	0.01uF	Capacitor SMT Ceramic X7R +/-10% 25V	603	Standard	Standard
12	C8-9 C14-15 C25 C46 C55 C68 C73 C89 C96 C98	1000pF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
5	C10 C12-13 C16 C22	0.1uF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard

Table 3. Bill of Materials for 16S Application (continued)

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
30	C7 C17 C19 C21 C27-29 C31 C34 C36 C40-41 C43-44 C51-53 C59-60 C62 C65 C67 C70-71 C82-83 C86-87 C93-94	3300pF	Capacitor SMT Ceramic X7R +/-10% 50V	603	Standard	Standard
16	C4-6 C33 C37-38 C42 C45 C47 C54 C61 C66 C84-85 C88 C95	22uF	Capacitor Ceramic SMT Y5V +/-20% 10V	805	Standard	Standard
24	R3 R6 R12-14 R20 R22 R30-33 R39 R42 R45 R48 R51 R53 R58 R61 R64-65 R69 R72 R75	100	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R4 R34	10K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R26 R35	100K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
12	R1 R7-8 R11 R15 R19 R23 R25 R28 R36- 38	1.0M	Resistor SMT 1/10W +/-5%	603	Standard	Standard
30	R5 R10 R21 R24 R40-41 R43-44 R46-47 R49-50 R52 R54-57 R59-60 R62-63 R66- 68 R70-71 R73-74 R76-77	20K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R2 R16	200K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
2	R17-18	30K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
1	R9	3K	Resistor SMT +/-5% 1W	603	Standard	Standard
2	R27 R29	4.7K	Resistor SMT 1/10W +/-5%	603	Standard	Standard
1	RSENSE	0.01	Resistor SMT +/-1% 1W +/-100ppm/°C	2512	Standard	Standard
15	L1-15	4.7uH	Inductor SMD Shielded Isat=2.0A	4.9mm x 4.9mm x 2.0mm	Taiyo Yuden	NRS5020T4R7MMGJ
4	Q1-4	Vds > 80V	N-Channel MOSFET, 2.5Vgs Rated	SOT-23	Standard	Standard
2	Q5-6	Idss=0.2 to 1.0mA	General Purpose N-Channel JFET Amplifier	SOT-23	Fairchild	MMBFJ201
1	Q7	100 Vds	MOSFET N-Channel 20Vgs	D2PAK	Standard	Standard
15	Q8-10 Q13-24	+/-8Vgs	MOSFET N/P Complementary Pair	6-TSOP	Alpha & Omega	AO6604
2	Q11-12	-100 Vds	MOSFET P-Channel 20Vgs	D2PAK	Standard	Standard
30	D1-30	500mA	Schottky Rectifier Diode 20V	SOD-123	Fairchild	MBR0520L
4	T1-4		Dual Diode	SOT-23	Fairchild	MMBD4148SE
5	LED1-5	Green/25 mA	Green Diffused LED 1.6mm x 0.8mm SMT	603	Standard	Standard

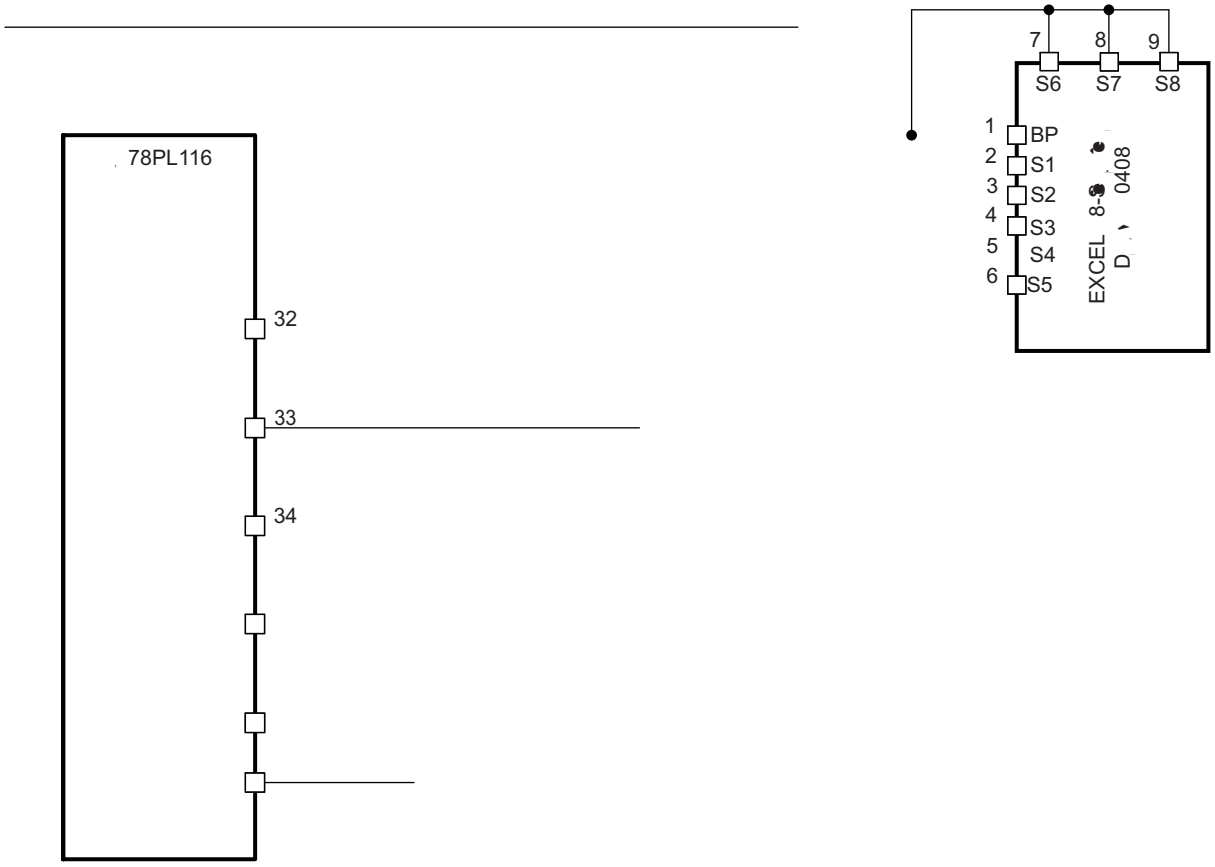
Table 3. Bill of Materials for 16S Application (continued)

Qty	Reference	Value	Description	Size	Manufacturer	Mfg Part No.
2	Z1 Z2	5.6VDC	Common Anode Zener Diode Pair 300mW	SOT-23	Standard	Standard
3	Z3-5	500mW	Zener Diode 500mW 12V	SOD-123	Standard	Standard
1	SOCI	50mA	Tactile Momentary Pushbutton Thru-Hole		Standard	Standard
1	HOST		Header	6 Position	Standard	Standard
1	J1	1.0 Amp	Header	5 Position	Standard	Standard
3	J2-4	3.0A	Header	4 Position	Standard	Standard
4	BATTERY+ BATTERY- PACK+ PACK-	30 Amps	Header	2 Position	Standard	Standard



NOTE: For reference only. Actual display used may require different operating voltage. Consult with display vendor.

Figure 10. Reference Schematic (Electronic-Paper Display Connections)



NOTE: For reference only. Actual display used may require different operating voltage. Consult with display vendor.

Figure 11. Reference Schematic (LCD Connections)

REVISION HISTORY

Changes from Revision A (October 2010) to Revision B **Page**

- Revised PowerLAN Characteristics table 9
- Changed Ah values in Current Measurement paragraph 16

PACKAGING INFORMATION

Orderable Device	Status (1)