Overvoltage Protection for 2-Series and 3-Series Cell Li-Ion Batteries

Check for Samples: bq294502, bq294504, bq294512, bq294515, bq294522, bq294524, bq294532, bq294562, bq294572, bq294582, bq294592

FEATURES

- 2-Series and 3-Series Cell Monitor for Secondary Protection
- Fixed Programmable Delay Timer
- Fixed OVP Threshold:
  - bq294502 = 4.35 V with 4-s Delay Timer
  - bq294504 = 4.35 V with 6.5-s Delay Timer
  - bq294512 = 4.40 V with 4-s Delay Timer
  - bq294515 = 4.425 V with 4-s Delay Timer
  - bq294522 = 4.45 V with 4-s Delay Timer
  - bq294524 = 4.45 V with 6.5-s Delay Timer
  - bq294532 = 4.50 V with 4-s Delay Timer
  - bq294562 = 4.25 V with 4-s Delay Timer
  - bq294572 = 4.00 V with 4-s Delay Timer
  - bq294582 = 4.225 V with 4-s Delay Timer
  - bq294584 = 4.225 V with 6.5-s Delay Timer
  - bq294592 = 4.30 V with 4-s Delay Timer
- High-Accuracy Overvoltage Protection: ± 10 mV
- Low Power Consumption I_{CC} ≈ 1 µA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- Low leakage current per cell input < 100 nA
- Small package footprint
  - 6-pin SON

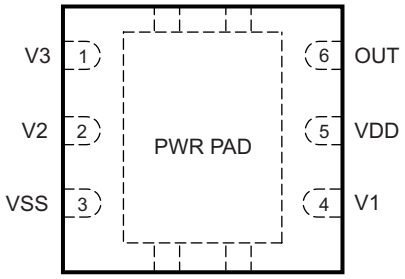
APPLICATIONS

- 2nd-Level Protection in Li-Ion Battery Packs in:
  - Tablets
  - Slates
  - Power Tools
  - Notebook Computers
  - Portable Equipment and Instrumentation

DESCRIPTION

The bq2945xy family of products is a secondary level voltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. Based on the configuration, an output is triggered after a fixed delay if any one of the two or three cells has an overvoltage condition. This output will be triggered into a high state after an overvoltage condition has satisfied the specified delay timer.

DRV Package
(Top View)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	OVP (V)	DELAY TIME (S)	TAPE AND REEL (LARGE)	TAPE AND REEL (SMALL)
–40°C to 110°C	bq294502	SON-6	DRV	4.35	4.0	bq294502DRVR	bq294502DRVT
	bq294504			4.35	6.5	bq294504DRVR	bq294504DRVT
	bq294512			4.40	4.0	bq294512DRVR	bq294512DRVT
	bq294515			4.425	4.0	bq294515DRVR	bq294515DRVT
	bq294522			4.45	4.0	bq294522DRVR	bq294522DRVT
	bq294524			4.45	6.5	bq294524DRVR	bq294524DRVT
	bq294532			4.50	4.0	bq294532DRVR	bq294532DRVT
	bq294562			4.25	4.0	bq294562DRVR	bq294562DRVT
	bq294572			4.00	4.0	bq294572DRVR	bq294572DRVT
	bq294582			4.225	4.0	bq294582DRVR	bq294582DRVT
	bq294584(2)			4.225	6.5	bq294584DRVR	bq294584DRVT
	bq294592			4.30	4.0	bq294592DRVR	bq294592DRVT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com (www.ti.com).
(2) Product Preview only

THERMAL INFORMATION

THERMAL METRIC(1)		bq2945xy SON 6 PINS	UNITS
JA	Junction-to-ambient thermal resistance	186.4	°C/W
JC(top)	Junction-to-case(top) thermal resistance	90.4	
JB	Junction-to-board thermal resistance	110.7	
JT	Junction-to-top characterization parameter	96.7	
JB	Junction-to-board characterization parameter	90	
JC(bottom)	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Submi8ics,

PIN FUNCTIONS

bq2945xy	Pin Name	Type I/O	Description
1	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack
2	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack
3	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
4	V1	IA	Sense input for positive voltage of the lowest cell in the stack
5	VDD	P	Power supply
6	OUT	OA	Output drive for external N-Channel FET
Thermal Pad	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed circuit board for proper operation

PIN DETAILS

Description

The voltage sensing for each cell is done independently using a multiplexer. The method of overvoltage detection is comparing the voltage to an overvoltage protection voltage V_{OV}. Once the voltage exceeds the programmed fixed value, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for either a 4-s or 6.5-s delay. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if *all* of the cell inputs (Vx) are below the OVP threshold minus the Vhys.

Figure 1. Timing for Overvoltage Sensing

Sense Positive Input for Vx

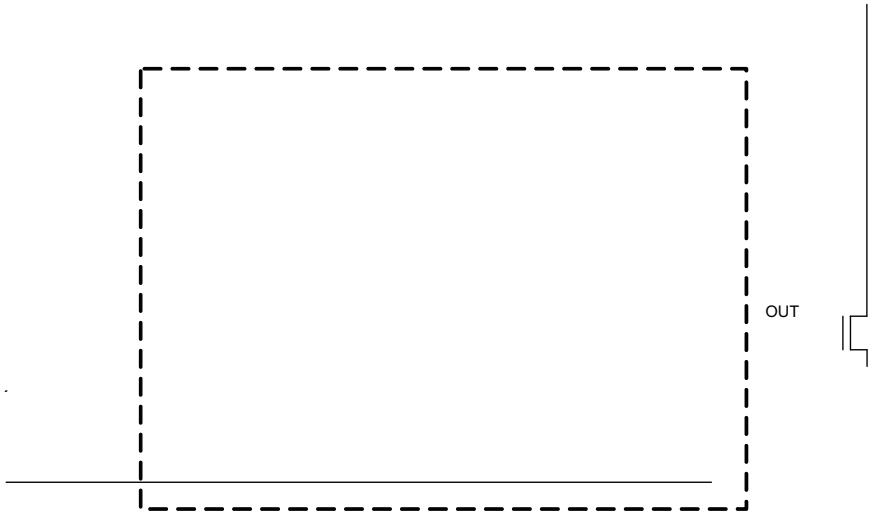
This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

The gate of an external N-Channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. The out will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

Supply Input, VDD

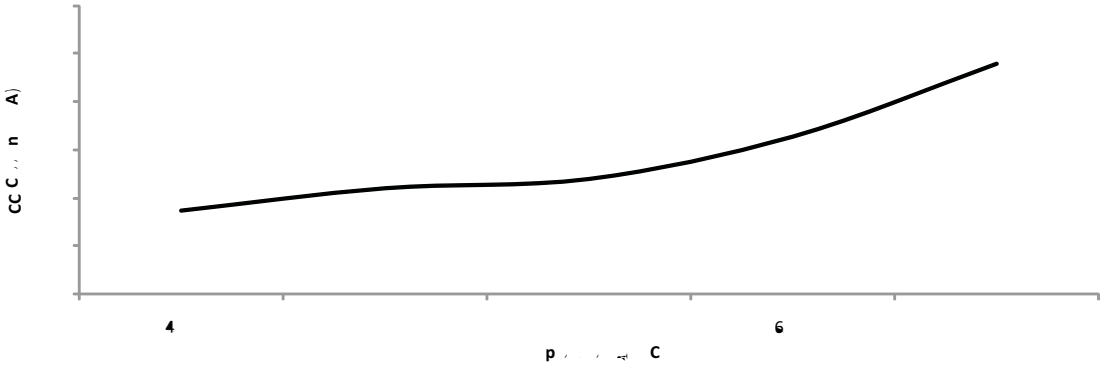
This

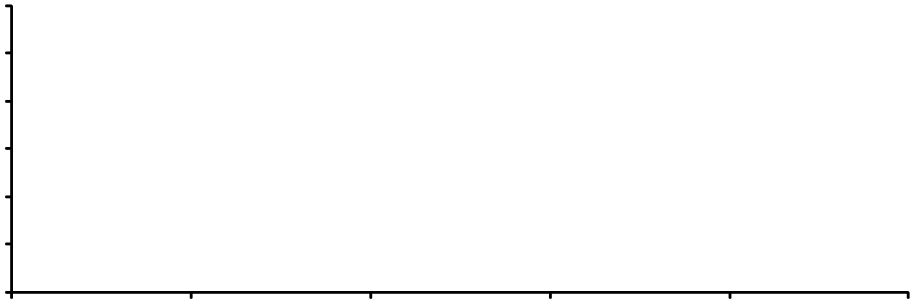

OUT

stated where T_A = 25

DC CHARACTERISTICS (continued)

Typical values stated where T_A = 25°C and VDD





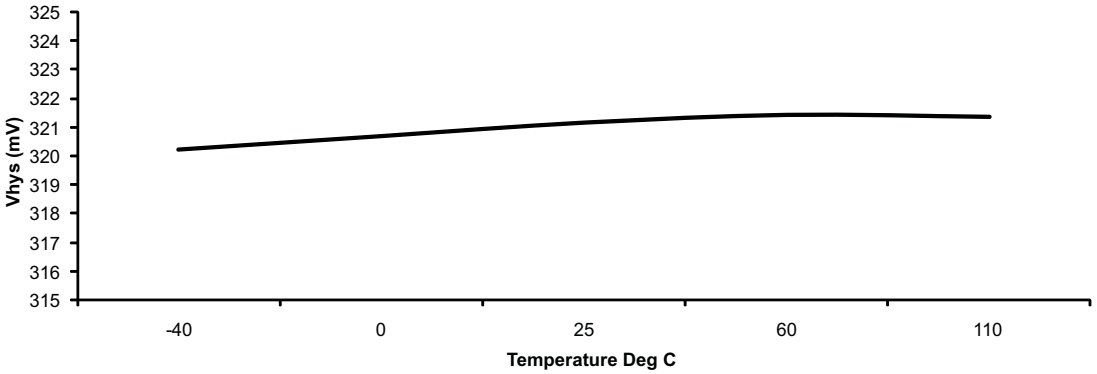


Figure 4. Hysteresis V_{HYS} Versus Temperature

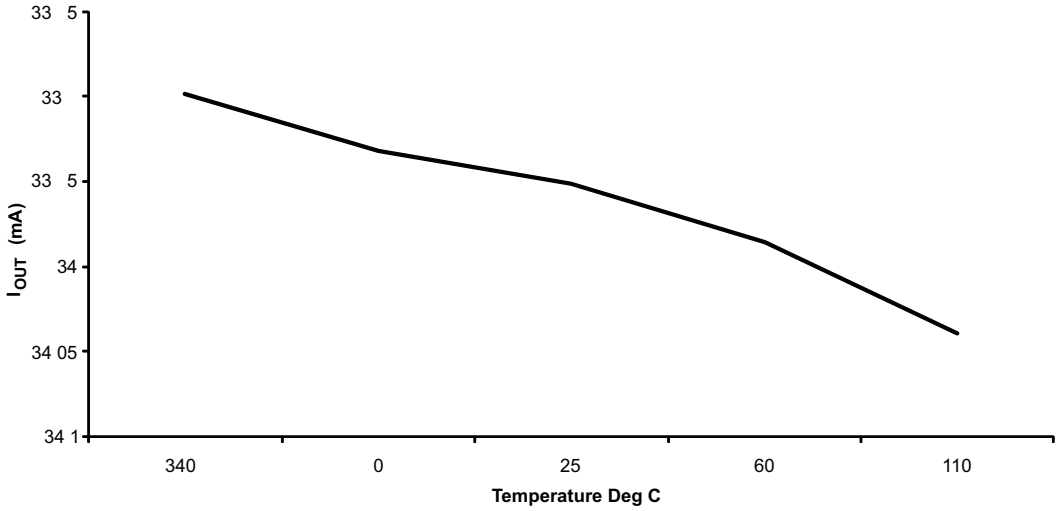


Figure 5. Output Current I_{OUT} Versus Temperature

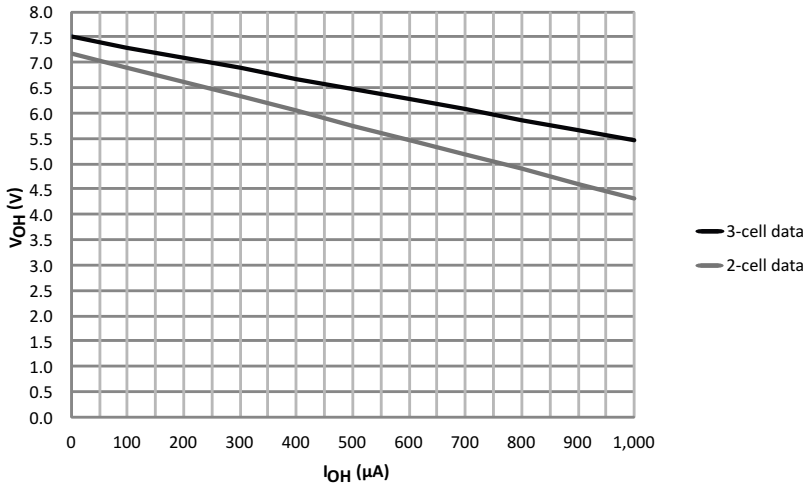


Figure 6. Output Voltage Versus Output Current

APPLICATION INFORMATION

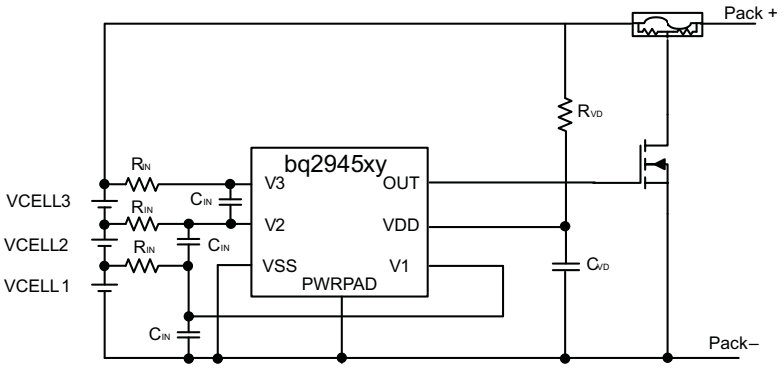


Figure 7. Application Configuration

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 7 shows each external component.

Table 1. Parameters

PARAMETER	External Component	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	
Voltage monitor filter capacitance	CIN	0.01		0.1	µF
Supply voltage filter resistance	RVD	100		1K	
Supply voltage filter capacitance	CVD		0.1		µF

APPLICATION SCHEMATIC

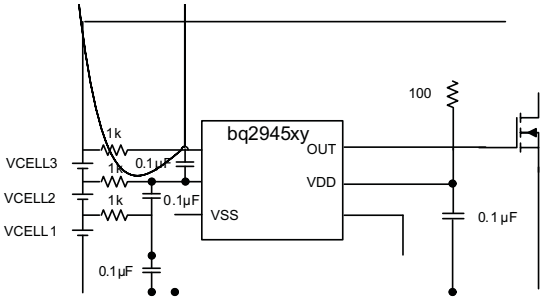


Figure 8. 3-Series Cell Configuration with Fixed Delay

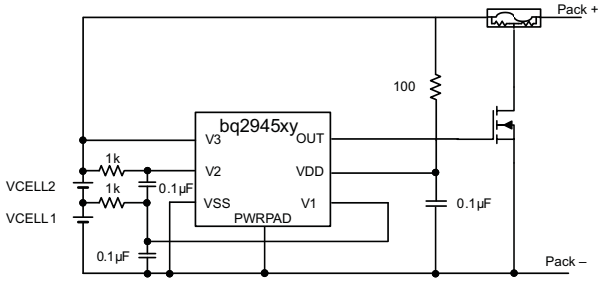


Figure 9. 2-Series Cell Configuration with Internal Fixed Delay

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V3 (see Figure 10). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to VC3 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 10 shows the timing for the Customer Test Mode.

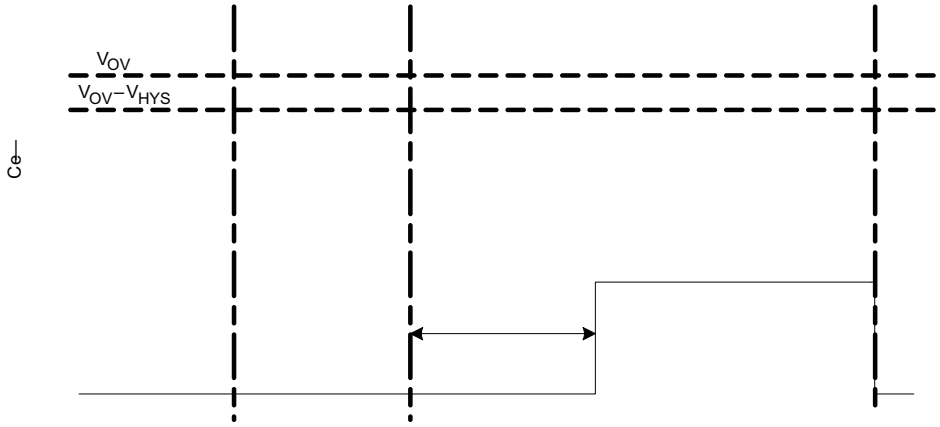


Figure 10. Timing for Customer Test Mode

Figure 11 shows the measurement for current consumption for the product for both VDD and Vx.

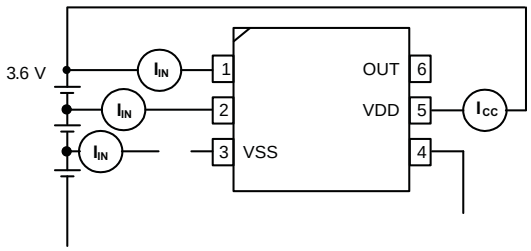


Figure 11. Configuration for IC Current Consumption Test

REVISION HISTORY

Changes from Original (September 2011) to Revision A **Page**

- Added the bq294582 Device to Production Data 2

Changes from Revision A (November 2011) to Revision B **Page**

- Changed the bq294504 Device to Production Data 1
- Added the bq294512 Device 1
- Added the bq294592 Device 1
- Added a second I_{CC} Test Condition 5
- Changed Fault Detection Delay Time in bq2945x4 Test Mode Specifications 5

Changes from Revision B (February 2012) to Revision C **Page**

- Added the bq294515 Device to Production Data 2
- Added the bq294524 Device to Production Data 2
- Added the bq294532 Device to Production Data 2
- Added the bq294572 Device to Production Data 2
- Changed Overvoltage Detection Hysteresis 5
- Added Output Voltage Versus Output Current graphic 7
- Changed Timing for Customer Test Mode figure 9

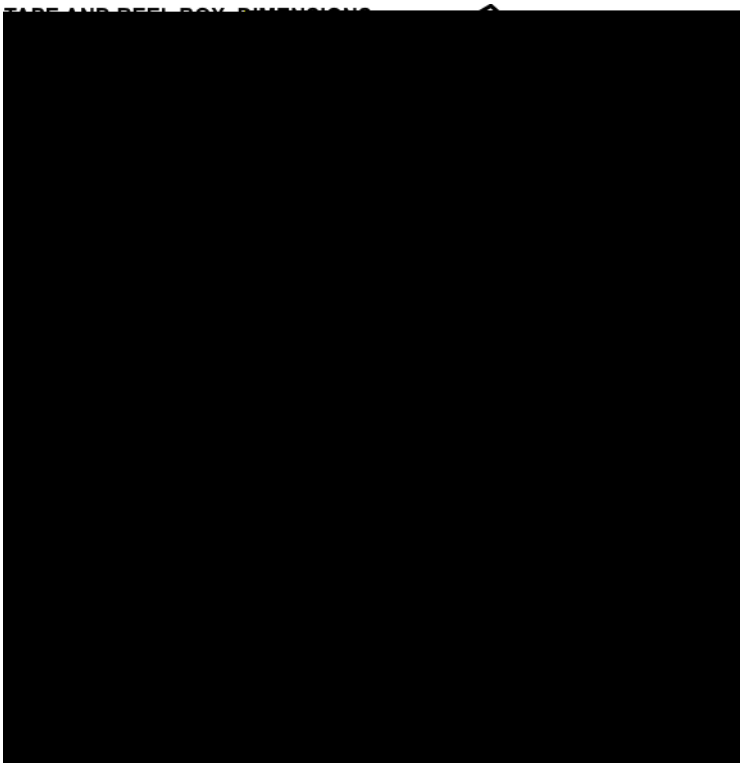
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ294502DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294502DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294504DRVR	PREVIEW	SON	DRV	6		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	
BQ294504DRVT	PREVIEW	SON	DRV	6		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	
BQ294512DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294512DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294515DRVR	PREVIEW	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4515	
BQ294515DRVT	PREVIEW	SON	DRV	6		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4515	
BQ294522DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294522DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU				

TAPE AND REEL INFORMATION

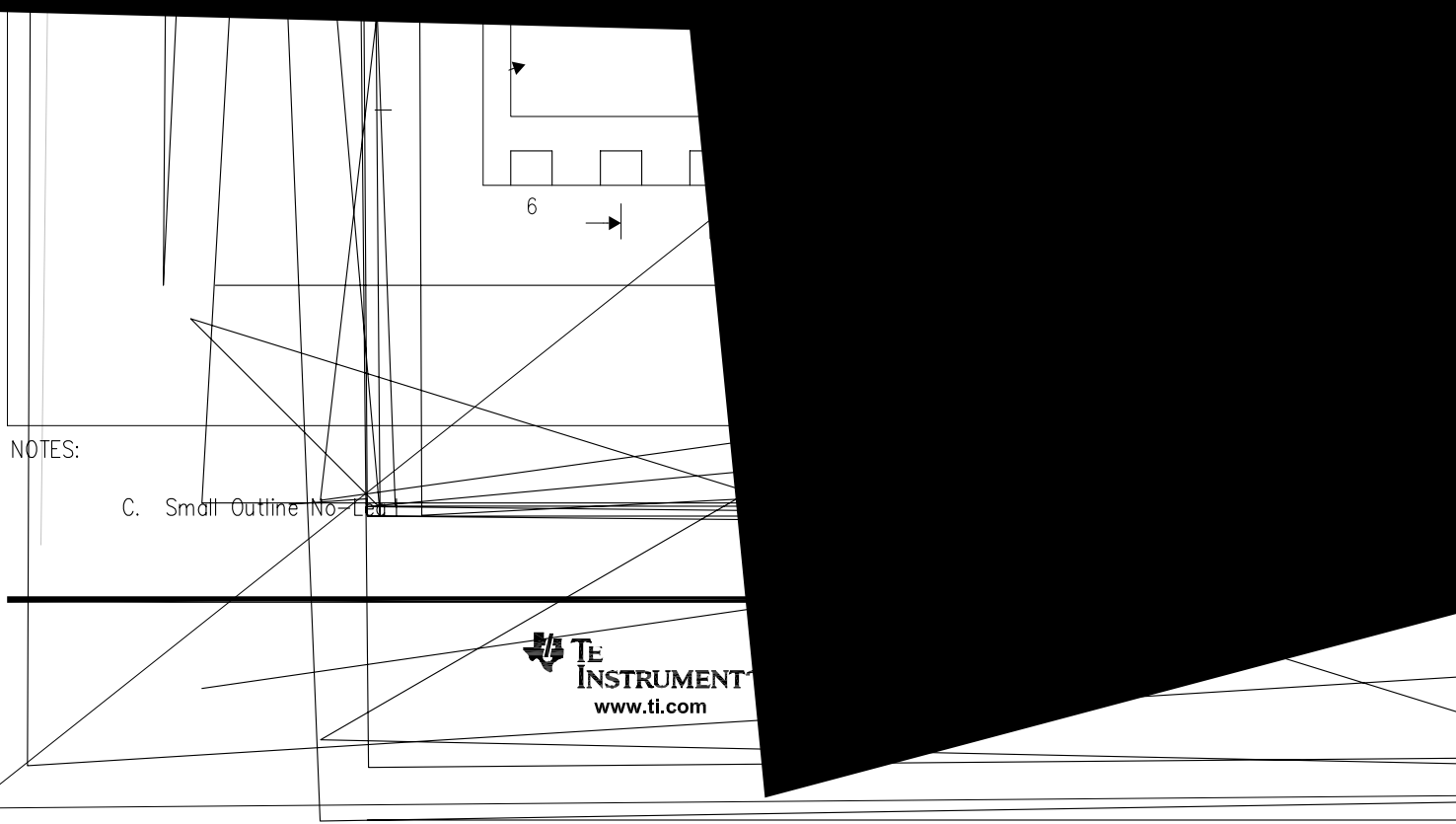
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294502DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294502DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294504DRVR	SON	DRV	6	0	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294504DRVT	SON	DRV	6	0	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294512DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294512DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294522DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294522DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294524DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294524DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294532DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294532DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294582DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294582DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294592DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294592DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294502DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294502DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVR	SON	DRV	6	0	367.0	367.0	35.0
BQ294504DRVT	SON	DRV	6	0	210.0	185.0	35.0
BQ294512DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294512DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294522DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294522DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294524DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294532DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294582DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294592DRVT	SON	DRV	6	250	210.0	185.0	35.0



NOTES:

C. Small Outline No-Lead

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

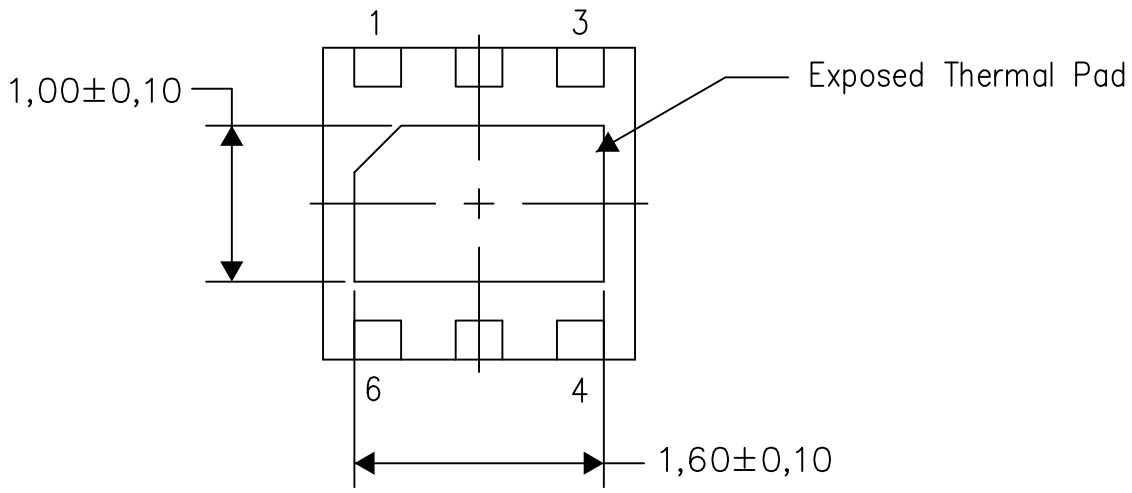
s package incorporates an exposed thermal pad that is designed to be attached directly to an external

thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the
directly to the appropriate copper plane shown in the electrica can be attached

integrated circuit (IC).

For in kage and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

Refer to IPC 7525 for stencil design considerations.
board fabrication site for solder mask tolerances.

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