THREE- AND FOUR-CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION IC

FEATURES

- **3- or 4-Cell Series Protection Control**
- **Autonomous Overcurrent and Short Circuit Protection**
- **Provides Individual Cell Voltages to Battery Management Host**
- **Integrated Cell Balancing Control**
- **I²C Compatible User Interface Allows Access to Battery Information**
- **User Control to Initiate Protection**
- **Integrated 3.3-V 25-mA LDO**
- **Programmable Shutdown and Brownout Control**
- **Provides Drive for Three External FETs**
- **Low Supply Current of 140 μA Typical**
- **Programmable Threshold and Delay for Short-Circuit Current Protection**
- **Provides Drive for Three External FETs**
- **Can Directly Interface With bq2083/5 for Complete Battery Management Solution**

APPLICATIONS

- **Notebook Computer Battery Packs**
- **Test Equipment**

PIN ASSIGNMENTS

DESCRIPTION

The bq29311 is a three- or four-cell lithium-ion battery pack protection analog front end (AFE) IC that incorporates a 3.3-V 25-mA low-dropout regulator (LDO) and an I²C compatible interface to extract battery parameters such as cell voltages and control output status. Other parameters, such as overcurrent protection threshold and delay,

T_A	PACKAGED TSSOP (PW)
−25°C to 85°C	bq29311PW
	bq29311PWR(1)

(1) R suffix indicates tape and reel.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PW	874 mW	6.99 W/°C	559 mW	454 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		bq29311
Supply voltage range(2)	V_{CC}, VPACK	−0.3 V to 34 V
Input voltage range	VC1, VC2, VC3, VC4, VBAT	−0.3 V to 34 V
	VC5, SR1, SR2	−1 V to 1 V
	VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to VC5	−0.3 V to 8.5 V
	CLK-IN, SCLK, SDATA	−0.3 V to 7 V
	CNTL	−0.3 V to 34 V
Output voltage range	DSG, CHG, PCHG	−0.3 V to V_{CC}
	LEDOUT, TOUT, SCLK, SDATA, VCELL, XALERT	−0.3 V to 7 V
Current for cell balancing		10 mA
Continuous total power dissipation		See Dissipation Rating Table
ESD rating(3)	HBM	1.5 kV
	CDM	250 V
	MM	50 V
Operating free-air temperature range, T_A		−25°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature (soldering, 10 s)		260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground of this device except VCn-VC(n+1), where n = 1, 2, 3, 4 cell voltage.
(3) Design considerations should be made with respect to excessive ESD.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
Supply voltage (V_{CC} or VPACK)					25	V
Input voltage range, V_I		VBAT	0		V_{CC}	V
		VC1, VC2, VC3, VC4	0		V_{CC}	
		SR1, SR2, VC5	−0.5		0.5	
		VCn−VC(n+1), (n = 1, 2, 3, 4)	0		5	
		CNTL			VREG	
Logic level input voltage	V_{IH}	SCLK, SDATA, CLK−IN	0.8×VREG		VREG	V
	V_{IL}		0		0.2×VREG	

F,

b3 in the SVOLTAGE UNIT

ELECTRICAL CHARACTERISTICS CONTINUED

T_A = 25°C, C_{REG} = 1 µF, V_{CC} = 14 V (unless otherwise noted)

OVERCURRENT (OC) AND SHORT CIRCUIT (SC) DETECTION							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(OCD)}$	OC detection threshold range, typical(1)	Charge (overcurrent)		50		205	mV
		Discharge (overload)		−50		−205	
$\Delta V_{(OCD)}$	OC detection threshold program step	Charge (overcurrent)			5		mV
		Discharge (overload)			−5		
$V_{hys(OCD)}$	OC detection threshold hysteresis	Charge and discharge (overcurrent and overload)		7	10	13	mV
$V_{(SC)}$	SC detection threshold range, typical(2)	Charge		100		475	mV
		Discharge		−100		−475	
$\Delta V_{(SC)}$	SC detection threshold program step	Charge			25		mV
		Discharge			−25		
$V_{hys(SC)}$	SC detection threshold hysteresis	Charge and discharge		40	50	60	mV
$V_{(OCD\_acr)}$	OC detection threshold accuracy(1)	Charge and discharge	$V_{(OCD)}$ = 50 mV (min)	37.5	50	62.5	mV
			$V_{(OCD)}$ = 100 mV	85	100	115	
			$V_{(OCD)}$ = 205 mV (max)	174	205	236	
$V_{(SC\_acr)}$	SC detection threshold accuracy(2)	Charge and discharge	$V_{(SC)}$ = 100 mV (min)	75	100	125	mV
			$V_{(SC)}$ = 200 mV	170	200	230	
			$V_{(SC)}$ = 475 mV (max)	403	475	547	

(1) See OCVD and OCVC registers for setting detection threshold.
(2) See SCV register for setting detection threshold.

FET DRIVE CIRCUIT							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(FETOL)}$	Output voltage	VBAT = 16 V	DSG	1	5	7	V
		VPACK = 16 V	CHG	1	5	7	
		VPACK = 16 V	PCHG	8.5	10.5	11.5	
$V_{(FETCLAMP)}$	Output clamp voltage	VPACK = 4.5 V	PCHG	3.3	3.5	3.7	V
t_r	Rise time	C_L = 4700 pF, 10% to 90%	DSG		10	100	µs
			CHG		10	100	

ELECTRICAL CHARACTERISTICS CONTINUED

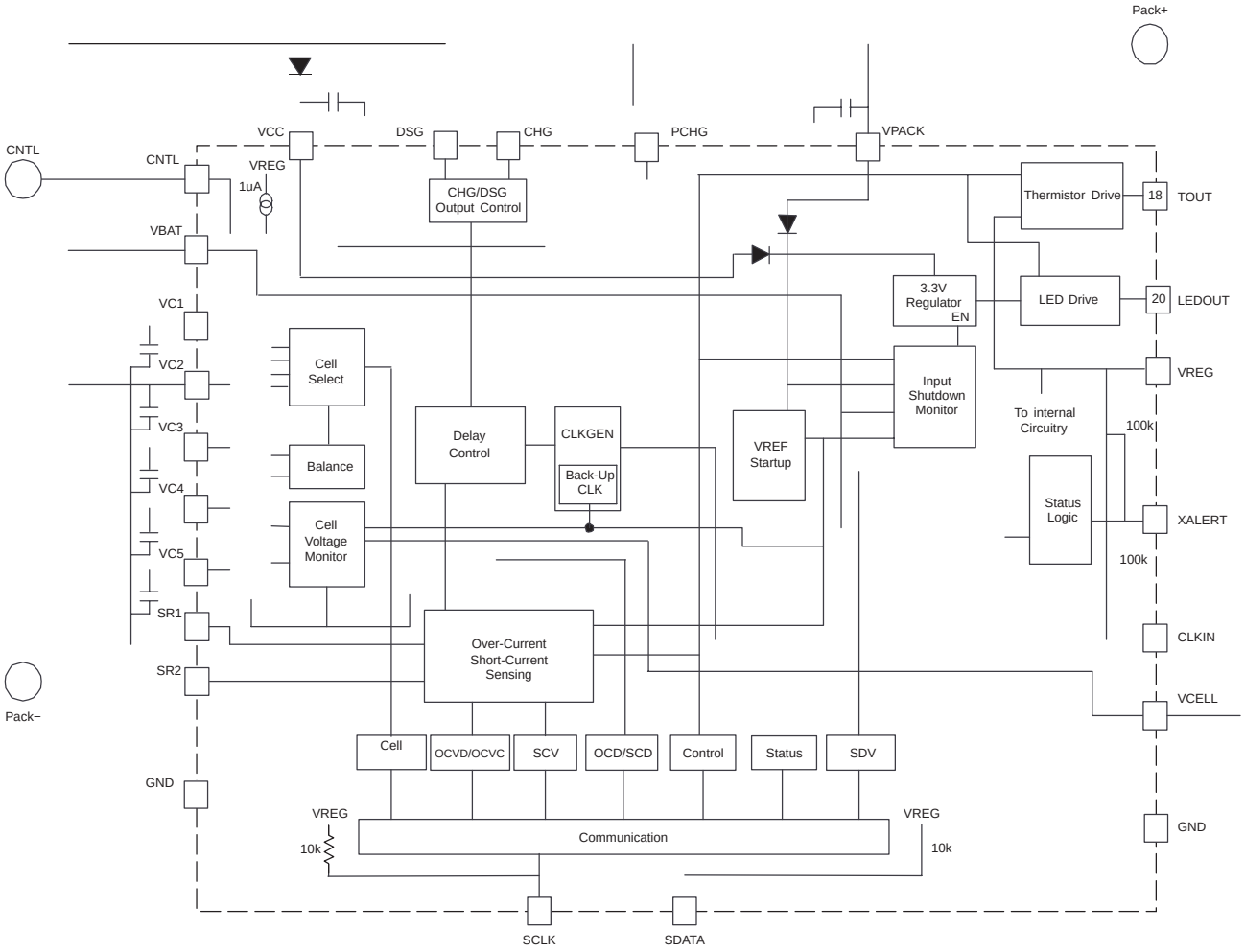
T_A = 25°C, C_{REG} = 1 µF, V_{CC} = 14 V (unless otherwise noted)

AC						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
$f_{(CLKIN)}$	CLKIN input frequency	External clock	32.100	32.768	33.420	kHz
$t_{(CLKIN\_HI)}$	CLKIN high time	External clock	2		28	µs
$f_{(INTERNAL)}$	Internal clock frequency	T_A = −25°C to 85°C	26.2	32.768	39.4	kHz
$t_{(SCDDELAY)}$	SC delay time	$t_{d(SC)}$ = 0 ms for charge and discharge $V_{(OCD)}$ = 100 mV, SR(50%) to DSG/CHG(50%) delay. No load.		1	10	µs

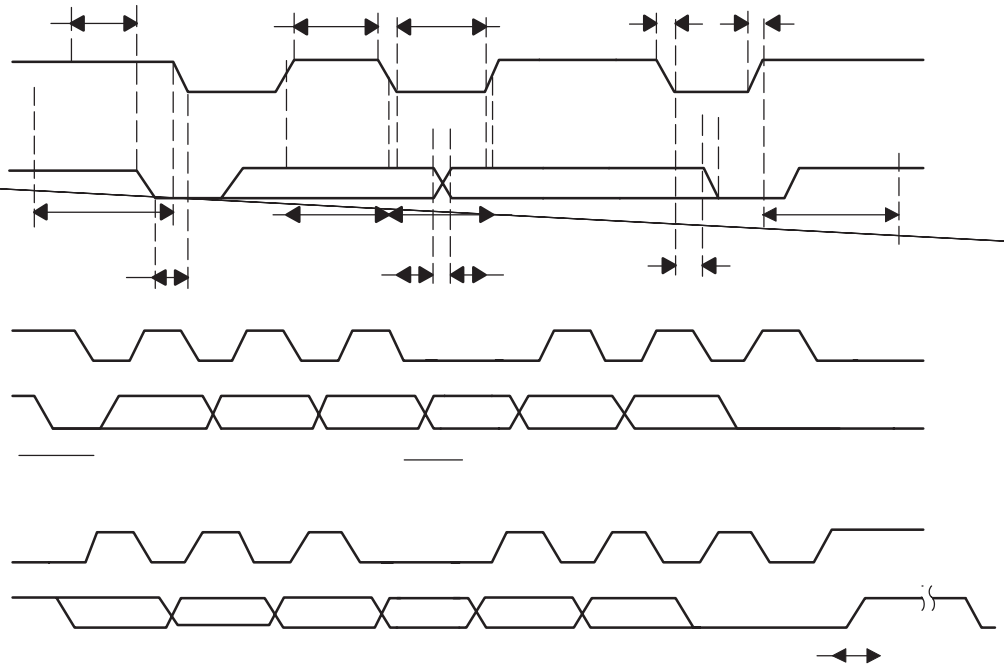
Terminal Functions

TERMINAL		DESCRIPTION
NAME	**NO.**	
CHG	21	Push-pull output charge FET gate voltage supply
CLKIN	16	Digital input that provides an alternate clock with internal 100-kΩ pullup to VREG
CNTL	10	Active low input enables CHG, DSG and PCHG. Internal pullup
DSG	23	Push-pull output discharge FET gate voltage supply
GND	11, 13	Analog ground pin and negative pack terminal
LEDOUT	20	Provides current to drive LED capacity display
PCHG	22	Push-pull output precharge FET gate voltage supply
SCLK	14	Open-drain bidirectional serial interface clock with internal 10-kΩ pullup to VREG
SDATA	15	Open-drain bidirectional serial interface data with internal 10-kΩ pullup to VREG
SR1	8	Current sense positive terminal when charging relative to SR2
SR2	9	Current sense positive terminal when discharging relative to SR1
TOUT	18	Provides thermistor bias current
VBAT	2	Battery positive terminal sense input for regulator shutdown
VC1	3	Sense voltage input terminal for most positive cell and balance current input for most positive cell. Connected to VC2 in 3-cell applications
VC2	4	Sense voltage input terminal for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell
VC3	5	Sense

FUNCTIONAL BLOCK DIAGRAM



AC TIMING SPECIFICATIONS (I^2C COMPATIBLE SERIAL INTERFACE)



APPLICATION INFORMATION

PRECHARGE MODE CURRENT LIMITING RESISTOR SELECTION

The selection of this resistor value should take into account the maximum potential charge voltage, which should include the voltage of a failed charger to ensure that 0-V and pre-charge mode current levels are within desirable limits under all conditions.

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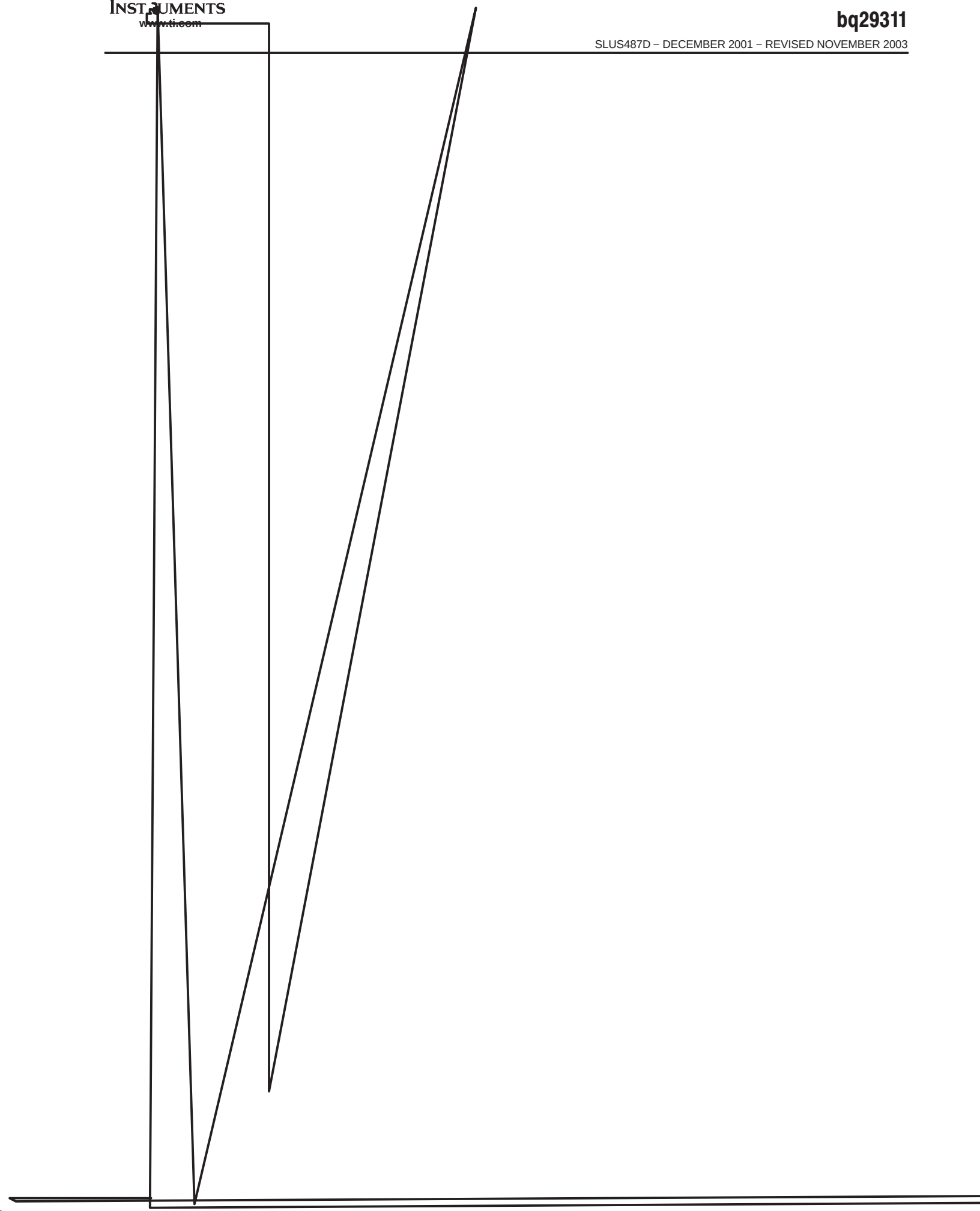


OVERCURRENT, OVERLOAD AND SHORT-CIRCUIT DELAY

The overcurrent and overload delays allow the system to momentarily accept a high current condition. The default overcurrent delay is 1 ms. The delay time can be increased via the OCD register, where the overcurrent and overload delays can be independently defined. The OCD register can be programmed for a range of 1 ms to 31 ms with steps of 2 ms.

The short-circuit delay has a default value of 0 ms and is also programmable in the SCD register. This register can be programmed from 0 to 915 µs with steps of 61 µs.

OVERCURRENT, OVERLOAD AND SHORT-CIRCUIT RESPONSE

When an overcurrent, overload, or short-circuit condition is detected, the CHG and DSG FETs are turned off and the PCHG FET turned on, limiting the charge current to the pre-charge rate. The STA

V. The translation output is inversely proportional to the input.

AGE T CELL VOL

The cell voltage is translated to allow a system host to measure individual series elements of the battery.

T h e series element voltage is translated to a GND-based voltage equal to 0.15 of the series element voltage. This provides a

CALIBRATION OF CELL VOLTAGE MONITOR AMPLIFIER GAIN

The cell voltage monitor amplifier has an offset, which can be calibrated to increase accuracy.

The following procedure shows how to measure and calculate the offset:

1. Set CAL2=0, CAL1=1, VM1=0, VM0=0
   The output voltage includes the offset and is represented by
   $V_{OUT1} = 0.975 + (1 + K) \times V_{OS}$ (V)
   where K = VCELL scaling factor
   V_{OS} = offset voltage at input of the internal op-amp
2. Set CAL2=1, CAL1=0, VM1=0, VM0=0
   The output voltage includes the scale factor error and offset and is represented by
   $V_{OUT2} = 0.975 + (1 + K) \times V_{OS} – K \times 0.975$ (V)
3. Calculate $(V_{OUT1} – V_{OUT2})/0.975$
   The result is the actual scaling factor, K_{ACT} and is represented by
   $K_{ACT} = (V_{OUT1}–V_{OUT2})/0.975 = (0.975 + (1 + K) \times V_{OS}) − (0.975 + (1 + K) \times V_{OS} – K \times 0.975)/0.975$
   $= K \times 0.975/0.975 = K$
4. Calculate the actual offset value where
   $V_{OS(ACT)} = (V_{OUT1} – 0.975)/(1 + K_{ACT})$
5. Calibrated cell voltage is calculated by
   $VCn − VC(n+1) = [0.975 + (1 + K_{ACT}) \times V_{OS(ACT)} − V_{CELLOUT}]/K_{ACT}$

CELL BALANCE CONTROL

The cell balance control allows a small discharge to be controlled for any one series element. The purpose of this discharge is to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the discharge current value.

Individual series element selection is made using CELL_SEL (b4...b7). Cell balance discharge is also disabled if bits CELL_SEL (b4...b7) are zero. When all CELL_SEL (b4 μ− − μ μμ Δ− − Δ

THERMISTOR DRIVE CIRCUIT

The TOUT pin can be enabled to drive a thermistor from VREG. The typical thermistor resistance is 10 kΩ at 25°C. The default-state for this is OFF to conserve power. The maximum output impedance is 100 Ω. TOUT (b6 of the control register) enables or disables this function. TOUT (b6 of CONTROL register) enables or disables this feature.

LED DRIVE CIRCUIT

The LED drive provides a current source from VREG. LEDEN (b5 of the control register) enables or disables this function.

CONTROL INPUT (CNTL)

1 thes O9. /F5 1s are 16.n thes O9TD 0by11 45.12 59c7 Tc ((safety)18F211 45FF 13esistance is 527.and.6079 -1. thes O9.logic. A

SDV: SHUTDOWN VOLTAGE

SDV REGISTER (0X02)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BOV3	BOV2	BOV1	BOV0	SDV3	SDV2	SVD1	SDV0

The SDV register is used to configure the regulator shutdown and brownout thresholds. 00000000 is the default.

SDV b3...b0 With Corresponding Threshold

0000	6.475 V	0100	7.675 V	1000	8.875 V	1100	10.075 V
0001	6.775 V	0101	7.975 V	1001	9.175 V	1101	10.375 V
0010	7.075 V	0110	8.275 V	1010	9.475 V	1110	10.675 V
0011	7.375 V	0111	8.575 V	1011	9.775 V	1111	10.975 V

SDV b7...b4 With Corresponding Threshold

0000	7.975 V	0100	9.175 V	1000	10.375 V	1100	11.575 V
0001	8.275 V	0101	9.475 V	1001	10.675 V	1101	11.875 V
0010	8.575 V	0110	9.775 V	1010	10.975 V	1110	12.175 V
0011	8.875 V	0111	10.075 V	1011	11.275 V	1111	12.475 V

OCVD: OVERCURRENT (OVERLOAD) VOLTAGE THRESHOLD IN DISCHARGE

OCVD REGISTER (0X03)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
–	–	–	OCVD4	OCVD3	OCVD2	OCVD1	OCVD0

OCVD b0−b4 (OCVD0−OCVD4): These five bits select the value of the overcurrent threshold in the discharge direction. 00000 is the default.

OCVD b4...b0 With Corresponding Threshold

00000	0.050 V	01000	0.090 V	10000	0.130 V	11000	0.170 V
00001	0.055 V	01001	0.095 V	10001	0.135 V	11001	0.175 V
00010	0.060 V	01010	0.100 V	100100			

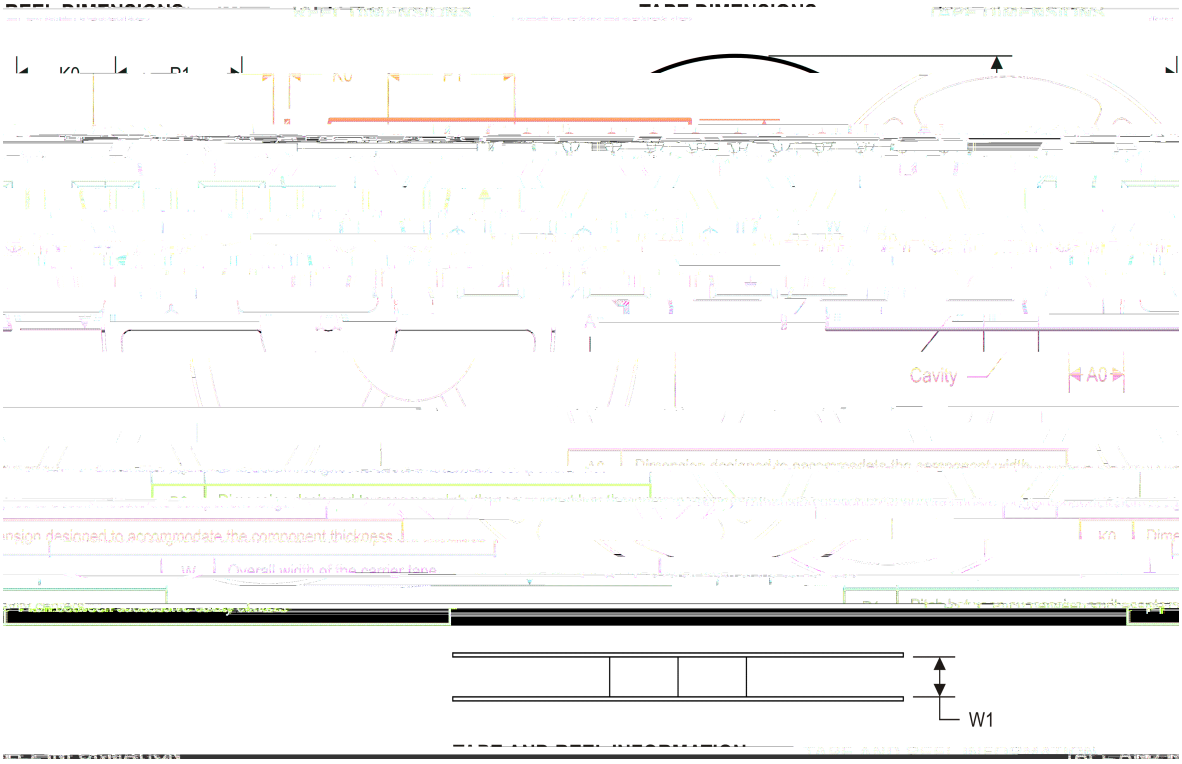
SCD b7...b4 With Corresponding Delay Time

0000	0 µs	0100	244 µs	1000	488 µs	1100	732 µs
0001	61 µs	0101	305 µs	1001	549 µs	1101	793 µs
0010	122 µs	0110	366 µs	1010	610 µs	1110	854 µs
0011	183 µs	0111	427 µs	1011	671 µs	1111	915 µs

PACKAGING INFORMATION

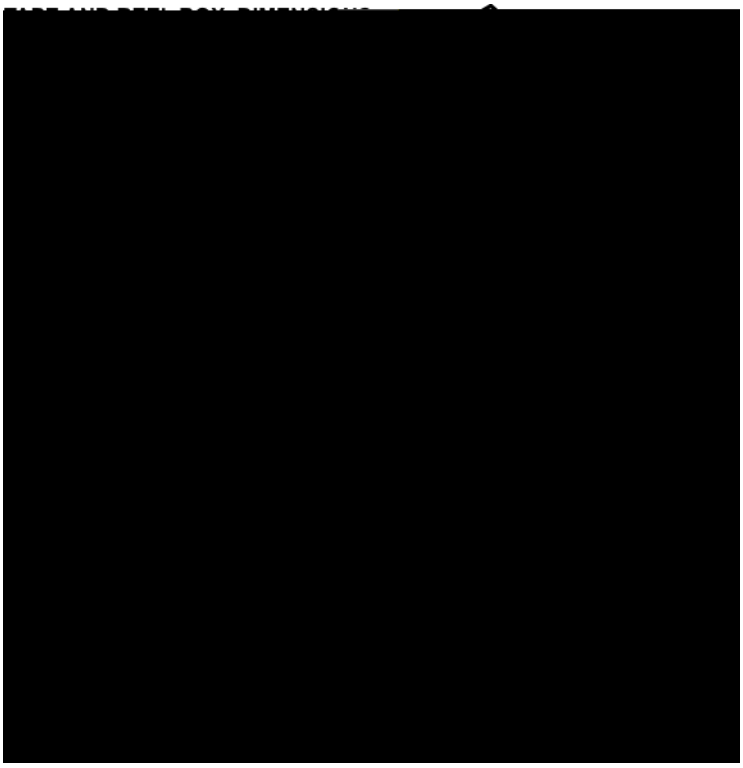
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ29311PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ29311PWG4	ACTIVE	TSSOP	PW	24				

TAPE AND REEL INFORMATION



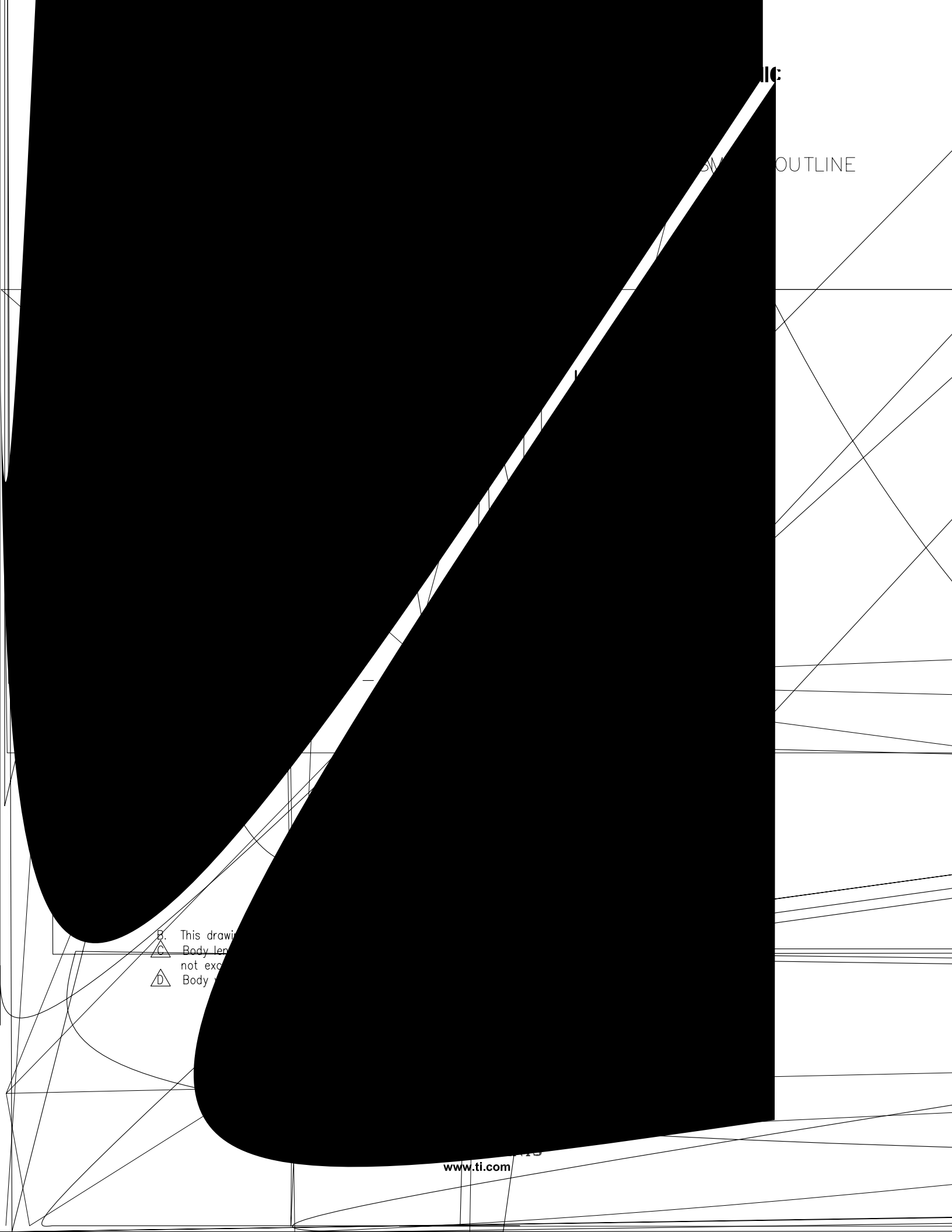
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29311PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29311PWR	TSSOP	PW	24	2000	367.0	367.0	38.0


OUTLINE
B. This drawi
C Body len
not exc
D Body