

Tablet PC and Netbook 2-Series Cell Li-Ion Battery Gas Gauge and Protection

 Check for Samples: [bq28400](#)

FEATURES

- Fully Integrated Gas Gauge and Analog Monitoring with Protection in a Single Package
- 2-Series Cell Li-Ion or Li-Polymer Battery Packs
- Flexible Memory Architecture with Integrated Flash Memory
- Zero-Volt and Pre-Charge Mode
- Full Array of Programmable Protection:
 - OV (Overvoltage)
 - UV (Undervoltage)
 - SC (Short Circuit)
 - OT (Overtemperature)
 - CIM (Cell Imbalance)
- Accurate CEDV Gauging Algorithm with Self Discharge Compensation
- High Accuracy Analog Interface with Two Independent ADCs:
 - High Resolution 16-Bit Integrator for Coulomb Counting
 - 16-Bit Delta-Sigma ADC with a 16-Channel Multiplexer for Voltage, Current, and Temperature
- High Side Protection FET Drive
- Fully Integrated Internal Clock Synthesizer with No External Components Required
- Two-Wire SMBus v1.1 Compliant Communications

- Reduced Power Modes (Typical Battery Pack Operating Range Conditions)
 - Low Power
 - Shutdown
- 20-Pin TSSOP Package (RoHS-Compliant)
- JEITA/Enhanced Charging
- Supports SHA-1 Authentication Responder

APPLICATIONS

- Tablet PCs
- Slate PCs
- Netbooks/Notebooks
- Smartbooks

DESCRIPTION

The bq28400 device is a fully integrated gas gauge and analog monitoring management solution that provides protection and control for 2-series cell Li-Ion battery packs in a single TSSOP package.

Implementing the optimum balance of quick response analog hardware-based monitoring and control along with an integrated fast CPU provides the ideal pack-based or in-system Li-Ion battery solution. The bq28400 also provides flexible user programmable settings stored in flash memory for control of critical system parameters such as overcurrent, short circuit, under/overvoltage, and over/undertemperature conditions.

The bq28400 communicates with the system host via a two-wire SMBus 1.1 compatible interface, providing high-accuracy reporting and control of battery pack operation. The FET drive and TSSOP package enable a lower cost and small footprint solution along with a simple layout and routing on narrow pack PCBs.

AVAILABLE OPTIONS

T _A	PACKAGE ⁽¹⁾	
	20-PIN TSSOP (PW) Tube	20-PIN TSSOP (PW) Tape and Reel
–40°C to 85°C	bq28400PW ⁽²⁾	bq28400PWR ⁽³⁾

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) A single tube quantity is 50 units.

(3) A single reel quantity is 2000 units.

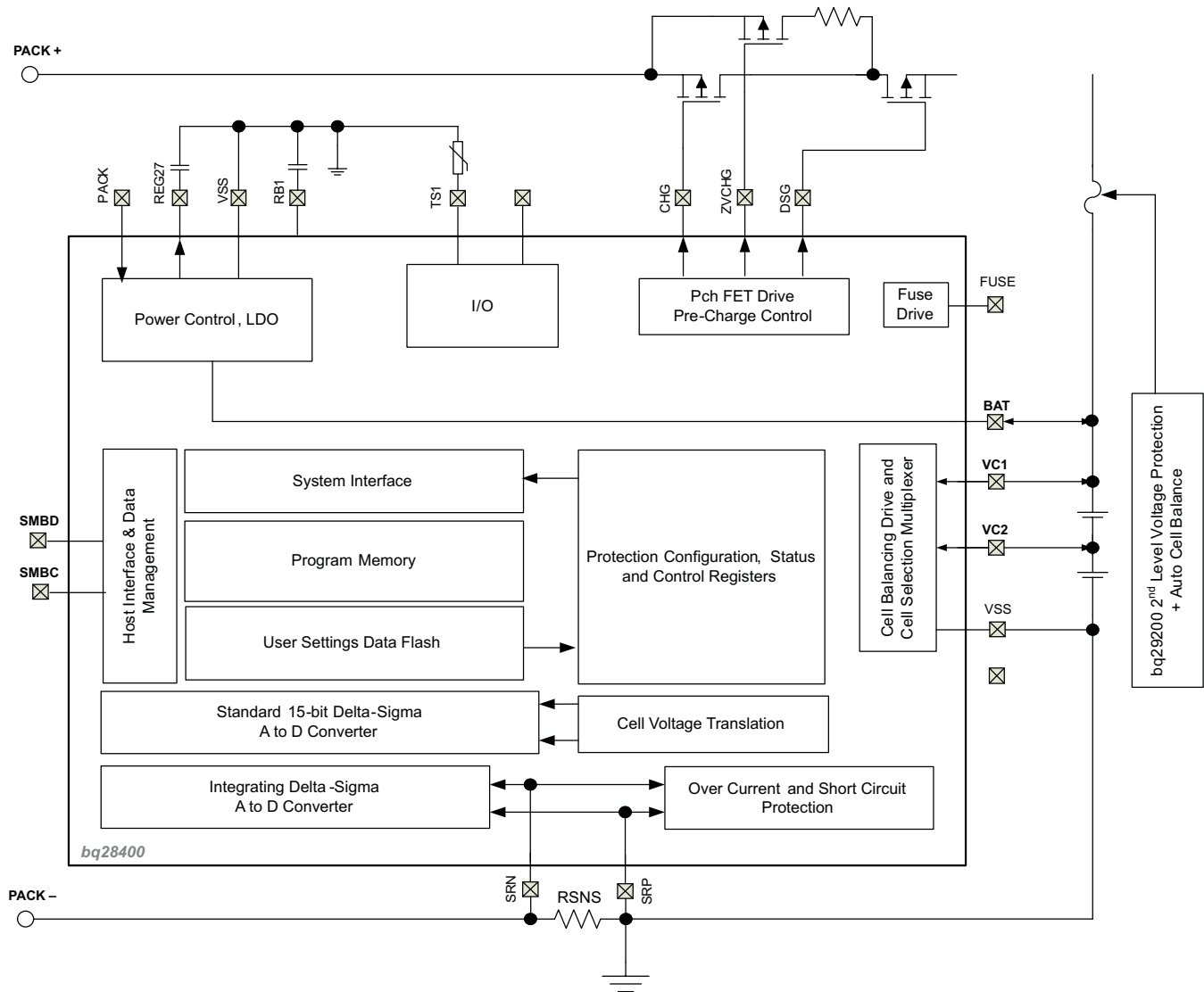


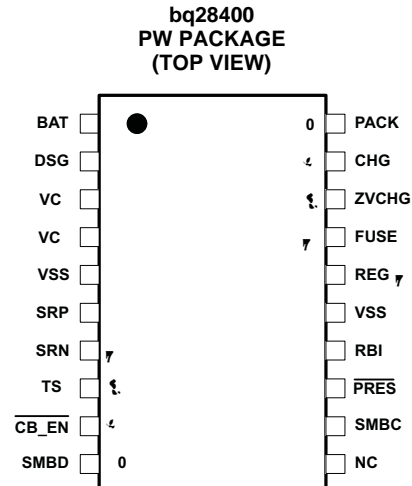
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM and TYPICAL IMPLEMENTATION





PIN FUNCTIONS

PIN NAME	PIN NUMBER	TYPE ⁽¹⁾	DESCRIPTION
BAT	1	P	Alternate supply input
DSG	2	O	P-channel discharge FET gate drive
VC1	3	AI	Sense input for the most positive cell. Also external cell balancing drive output for the most positive cell
VC2	4	AI	Sense input for the lowest cell. Also external cell balancing drive output for the lowest cell
VSS	5	P	Device ground
SRP	6	AI	Differential Coulomb Counter input or SRP oversampled ADC input
SRN	7	AI	Differential Coulomb Counter input or SRN oversampled ADC input
TS1	8	I	Thermistor 1 input. Connect NTC from this pin to VSS pin
$\overline{\text{CB_EN}}$	9	O	Output signal to control cell balancing
SMBD	10	I/OD	SBS data
NC	11	—	No connection, leave floating
SMBC	12	I/OD	SBS clock
$\overline{\text{PRES}}$	13	I	System present
RBI	14	P	RAM backup pin to provide backup potential to the internal DATA RAM if power is momentarily lost, by using a capacitor attached between RBI and VSS
VSS	15	P	Device ground
REG27	16	P	2.7-V regulator. Connect a capacitor between REG27 and VSS
FUSE	17	O	Push-pull fuse circuit drive
ZVCHG	18	O	P-channel precharge FET gate drive
CHG	19	O	P-channel charge FET gate drive
PACK	20	P	Alternate supply input

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		bq28400	UNITS
		PW	
		20 PINS	
q_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	91.7	°C/W
$q_{JC(top)}$	Junction-to-case(top) thermal resistance ⁽³⁾	20.4	
q_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	45.6	
y_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.5	
y_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	43.3	
$q_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance ⁽⁷⁾	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, y_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining q_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, y_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining q_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)⁽¹⁾

		Value/Unit
Supply voltage range, V_{MAX}	PACK w.r.t. V_{SS}	-0.3 to 34 V
Input voltage range, V_{IN}	VC1, BAT	$V_{VC2} - 0.3$ to $V_{VC2} + 8.5$ or 34 V, whichever is lower
	VC2	$V_{VSRP} - 0.3$ to $V_{VSRP} + 8.5$ V
	SRP, SRN	-0.3 to V_{REG27}
	General Purpose open-drain I/O pins: SMBD, SMBC	$V_{SS} - 0.3$ V to 6 V
	General Purpose push-pull I/O pins: TS1, \overline{PRES} , $\overline{CB_EN}$	-0.3 V to $V_{REG27} + 0.3$ V
	Input voltage range to all other pins, V_{IN} relative to V_{SS}	-0.3 V to $V_{REG27} + 0.3$ V
	DSG, CHG, ZVCHG	-0.3 to BAT
	FUSE	-0.3 to [BAT or PACK] (whichever is lower)
	RBI, REG27	-0.3 to 2.75 V
Maximum Operational VSS current, I_{SS}		50 mA
Ambient Temperature, T_A		-20 to 110°C
Storage temperature range, T_{STG}		-65 to 150°C
ESD Human Body Model ⁽²⁾	All pins except VC1 and VC2	2 kV
	VC1 and VC2	1 kV
ESD Machine Model	All pins	200 V

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The human body model is a 100-pF capacitor discharged through a 1.5-k Ω resistor into each pin.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	PIN	MIN	NOM	MAX	UNIT
Supply voltage	PACK			$V_{BAT} + 5$	V
	BAT	3.8		$V_{VC2} + 5$	
$V_{(STARTUP)}$					

ELECTRICAL CHARACTERISTICS (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{BAT} = V_{PACK} = 7.2\text{ V}$, Min/Max values stated where $T_A = -20^\circ\text{C}$ to 85°C and $V_{BAT} = V_{PACK} = 3.8\text{ V}$ to 18.75 V over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITION ⁽¹⁾	MIN	TYP	MAX	UNIT
SRx Wake from					

ELECTRICAL CHARACTERISTICS (continued)

Typical values stated where T_A = 25°C and V_BAT = V_PACK = 7.2 V, Min/Max values stated where T_A = -20°C to 85°C and V_BAT = V_PACK = 3.8 V to 18.75 V over operating free-air temperature range (unless otherwise noted)

Table with columns: PARAMETER, TEST CONDITION(1), MIN, TYP, MAX, UNIT. Rows include Internal Temperature Sensor, Thermistor Measurement Support, Internal Thermal Shutdown, Current Protection Thresholds, and Current Protection Timing.

M... (DETECT) ... (DETECT)

ELECTRICAL CHARACTERISTICS (continued)

Typical values stated where $T_A = 25^\circ\text{C}$ and $V_{\text{BAT}} = V_{\text{PACK}} = 7.2\text{ V}$, Min/Max values stated where $T_A = -20^\circ\text{C}$ to 85°C and $V_{\text{BAT}} = V_{\text{PACK}} = 3.8\text{ V}$ to 18.75 V over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION ⁽¹⁾	MIN	TYP	MAX	UNIT
Pre-Charge/ZVCHG FET Drive						
$V_{(\text{PreCHGON})}$	$V_{\text{O}(\text{PreCHGON})} = V_{(\text{PACK})}$ $-V_{(\text{ZVCHG})}$, pre-charge FET on ⁽⁸⁾	$R_{\text{GS}} = 1\text{ M}\Omega$, $V_{\text{PACK}} = 10\text{ V}$	9	9.5	10	V
$V_{(\text{PreCHGOFF})}$	Output voltage, pre-charge FET off ⁽⁸⁾	$R_{\text{GS}} = 1\text{ M}\Omega$, $T_A = -20^\circ\text{C}$ to 110°C			$V_{\text{BAT}} - 0.5$	V
t_r	Rise time	$C_L = 4700\text{ pF}$, $R_G = 5.1\text{ k}\Omega$		80	200	μs
t_f	Fall time	$C_L = 4700\text{ pF}$, $R_G = 5.1\text{ k}\Omega$		1.7		ms
SMBus						
f_{SMB}	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	Master mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			μs
$t_{\text{HD:STA}}$	Hold time after (repeated) start		4			μs
$t_{\text{SU:STA}}$	Repeated start setup time		4.7			μs
$t_{\text{SU:STO}}$	Stop setup time		4			μs
$t_{\text{HD:DAT}}$	Data hold time	Receive mode	0			ns
		Transmit mode	300			
$t_{\text{SU:DAT}}$	Data setup time		250			ns
t_{TIMEOUT}	Error signal/detect		See ⁽⁹⁾		35	ms
t_{LOW}	Clock low period		4.7			μs
t_{HIGH}	Clock high period		See ⁽¹⁰⁾		50	μs
$t_{\text{LOW:SEXT}}$	Cumulative clock low slave extend time		See ⁽¹¹⁾		25	ms
$t_{\text{LOW:MEXT}}$	Cumulative clock low master extend time		See ⁽¹²⁾		10	ms
t_f	Clock/data fall time		See ⁽¹³⁾		300	ns
t_r	Clock/data rise time		See ⁽¹⁴⁾		1000	ns

(8) For a V_{BAT} or V_{PACK} input range of 3.8 V to 18.75 V, MIN $V_{\text{O}(\text{FETON})}$ voltage is 9 V or $V_{(\text{BAT})} - 1\text{ V}$, whichever is less.

(9) The bq28400 times out when any clock low exceeds t_{TIMEOUT} .

(10) $t_{\text{HIGH:MAX}}$ is the minimum bus idle time. SMBC = SMBD = 1 for $t > 50\text{ }\mu\text{s}$ causes reset of any transaction involving bq28400 that is in progress.

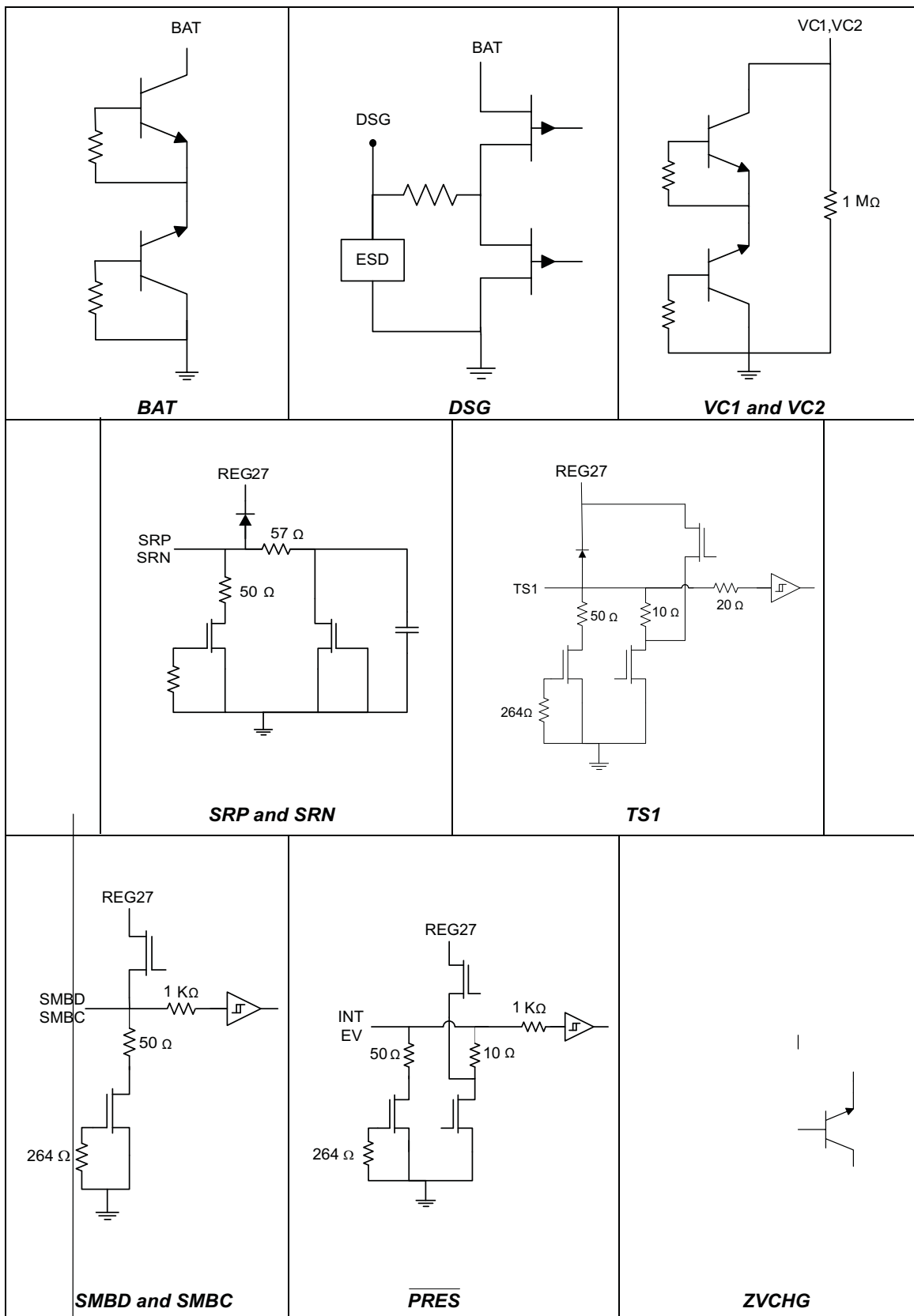
(11) $t_{\text{LOW:SEXT}}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.

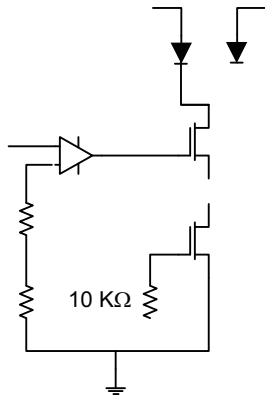
(12) $t_{\text{LOW:MEXT}}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

(13) Rise time $t_r = V_{\text{ILMAX}} - 0.15$ to $(V_{\text{IHMIN}} + 0.15)$.

(14) Fall time $t_f = 0.9V_{\text{DD}}$ to $(V_{\text{ILMAX}} - 0.15)$.

PIN EQUIVALENT CIRCUITS





TIMING CIRCUITS



Figure 1. Timing Conditions

GENERAL OVERVIEW

The bq28400 has a flexible architecture that enables development of numerous battery-management solutions. The device is a fully integrated battery manager, as shown in the functional block diagram, and performs necessary calculations and control for a fully functional 2-series cell battery management system. The device provides flexible user settings that are stored in flash memory.

The bq28400 determines battery capacity by monitoring the amount of charge input or removal from 2-series cell Li-Ion rechargeable batteries via a small value series sense resistor. The device then controls and reports the battery status using corrections for environmental and operating conditions. Additional control and monitoring is implemented for individual cell voltages, temperature, and current.

FEATURE SET

Safety Features

The bq28400 supports a wide range of battery and system protection features that can be configured. The primary safety features include:

- Cell over/undervoltage protection
- Overcurrent during charge and discharge
- Short circuit
- Overtemperature during charge and discharge
- Device watchdog timer

The secondary safety features used to indicate more serious faults which can be used to control FET state or blow an in-line fuse to permanently disable the battery pack include:

- Safety overvoltage
- Safety undervoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge
- Charge, pre-charge, and discharge FET fault
- Cell imbalance detection

Charge Control

The bq28400 charge control features include:

- Reporting charging current needed for constant current charging and charging voltage needed for constant voltage charging to a smart charger using SMBus communications
- Supports pre-charging/zero-volt charging
- Supports fast charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms

Gas Gauging

The device uses advanced Compensated End-of-Discharge Voltage (CEDV) technology to measure and calculate the available charge capacity in battery cells under system use and environmental conditions. The device accumulates a measure of charge and discharge currents, then compensates the charge current measurement for temperature and the state-of-charge of the battery. The bq28400 further estimates battery self-discharge, adjusts the self-discharge estimation for temperature, and then updates internal status registers. These internal registers are made available to the system host via the two-wire SMBus.

The internal general-purpose SRAM can be powered by the RBI pin of the bq28400 if power is lost. Typically, a 0.1- μ F capacitor provides the necessary voltage to the SRAM array during inadvertent momentary power loss.

See the bq28400 technical reference guide for further details.

Lifetime Data Logging

The bq28400 maintains the highest temperature value from the last device reset.

Power Modes

The bq28400 supports three power modes to reduce power consumption:

- In Normal Mode, the device performs measurements, calculations, protection decisions, and data updates in 1-second intervals. Between these intervals, the device is in a reduced power stage.
- In Sleep Mode, the bq28400 performs measurements, calculations, protection decisions and data updates in longer intervals. Between these intervals, the device is in a reduced power stage.
 - A wake function operates so that an exit from Sleep mode occurs when current flow, detection of failure,

or SMBus activity detected.

- In Shutdown Mode, the bq28400 is completely disabled by turning off all FETs and powering down the bq28400. Charge 292. (C3606 Td (onTj) 360 Td (charge)

CONFIGURATION

Oscillator Function

The bq28400 fully integrates the system oscillator; therefore, no external components are required for this feature.

System Present Operation

The device checks the $\overline{\text{PRES}}$ pin periodically. If the $\overline{\text{PRES}}$ pin input is pulled to ground by the external system, the bq28400 detects this event as the presence of the system.

2-Series Cell Configuration

The bq28400 supports 2-series cell battery pack configurations.

Cell Balancing Configuration

If cell balancing is required, the bq28400 cell balance control enables a weak, internal pull-down for each VCx pin. The purpose of this weak pull-down is to enable an external FET for current bypass. Series resistors placed between the input VCx pins and the positive battery cell terminals control the VGS of the external FET. Alternatively, CB_EN output can be used with the bq29200 device to control the auto cell-balancing feature for the system (see [Figure 5](#)). Further details are provided in the [APPLICATION INFORMATION](#) section of this document.

BATTERY PARAMETER MEASUREMENTS

The bq28400 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell voltage, battery voltage, and temperature measurements. The individual cell voltages, *Voltage*, *Current*, *AverageCurrent*, and *Temperature* are updated in 1-second intervals during normal operation. discharge 360 Td (onTj) 360 Td (charge)

Charge and Discharge Counting

The integrating ADC measures the charge and discharge flow of the battery. 5000 Td (featuoni /Fd (measures 0 0 0 rg 54 9T)

Current

The bq28400 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-m Ω to 20-m Ω typical sense resistor.

Temperature

The bq28400 has an internal temperature sensor and input pin for an external temperature sensor. The bq28400 can be configured to use either the internal or external temperature sensor. The default setting for the bq28400 is for a Semitec 103AT thermistor as input to the TS1 pin. Reporting of measured temperature is available by way of the SBS Temperature command.

COMMUNICATIONS

The bq28400 uses SMBus v1.1 in Slave Mode per the SBS specification.

SBS Commands

Table 1. SBS COMMANDS

SBS Command	Mode	Name	Format	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	H2	0x0000	0xffff	—	
0x03	R/W	BatteryMode	H2	0x0000	0xe383	—	
0x08	R	Temperature	U2	0	65535	—	0.1°K
0x09	R	Voltage	U2	0	65535	—	mV
0x0a	R	Current	I2	–32768	32767	—	mA
0x0b	R	AverageCurrent	I2	–32768	32767	—	mA
0x0c	R	MaxError	U1	0	100	—	%
0x0d	R	RelativeStateOfCharge	U1	0	100	—	%
0x0f	R/W	RemainingCapacity	U2	0	65535	—	mAh or 10 mWh
0x10	R	FullChargeCapacity	U2	0	65535	7200	mAh
0x14	R	ChargingCurrent	U2	0	65534	2500	mA
0x15	R	ChargingVoltage	U2	0	65534	12600	mV
0x16	R	BatteryStatus	U2	0x0000	0xdbff	—	
0x17	R/W	CycleCount	U2	0	65535	0	
0x18	R/W	DesignCapacity	U2	0	65535	7200	mAh
0x19	R/W	DesignVoltage	U2	0	65535	10800	mV
0x1a	R/W	SpecificationInfo	H2	0x0000	0xffff	0x0031	
0x1b	R/W	ManufactureDate	U2	—	—	0	ASCII
0x1c	R/W	SerialNumber	H2	0x0000	0xffff	0x0001	
0x20	R/W	ManufacturerName	S12	—	—	Texas Inst.	ASCII
0x21	R/W	DeviceName	S8	—	—	bq28400	ASCII
0x22	R/W	DeviceChemistry	S5	—	—	LION	ASCII
0x23	R/W	ManufacturerData	S9	—	—	—	ASCII
0x2f	R/W	Authenticate	S21	—	—	—	ASCII
0x3e	R	CellVoltage2	U2	0	65535	—	mV
0x3f	R	CellVoltage1	U2	0	65535	—	mV

Extended SBS Commands

Table 2 shows the extended SBS commands for the device.

Table 2. Extended SBS Commands

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x61	R/W	FullAccessKey	hex	4	0x00000000	0xffffffff	—	
0x63	R/W	AuthenKey3	hex	4	0x00000000	0xffffffff	—	
0x64	R/W	AuthenKey2	hex	4	0x00000000	0xffffffff	—	
0x65	R/W	AuthenKey1	hex	4	0x00000000	0xffffffff	—	
0x66	R/W	AuthenKey0	hex	4	0x00000000	0xffffffff	—	

APPLICATION INFORMATION

Run Time to Empty

To predict how much run time the battery pack can supply to the host system, a “Run Time To Empty” value can be calculated.

The SBS host system needs to read, store, and update the following values during a discharging period and average them over a user-determined period of time:

- DSG bit of the BatteryStatus register (ensure that it is in discharge mode)
- AverageCurrent (mA)
 - Positive value = charge current
 - Negative value = discharge current
 - One minute rolling average of current (the user can accumulate this time for improved granularity)
- RemainingCapacity (mAh)

Then calculating:

$\text{RunTimeToEmpty} = \text{RemainingCapacity}(\text{avg mAh}) \div \text{AverageCurrent}(\text{avg mA})$ (The result will be in hours.
For minutes, the user can take the above results and divide by 60.)

Charging Time to Full

To predict how much charging time before the battery pack is full

Cell Balancing

Cell balancing increases the useful life of battery packs. Cell-to-cell differences in self-discharge, capacity, and impedance can lead to different charge states among the cells; however, the charger terminates the charge based on the summed voltage only, which may leave some cells undercharged and others overcharged. To remedy this imbalance and to achieve the goal of having all cells reach 100% state-of-charge at charge termination, it is

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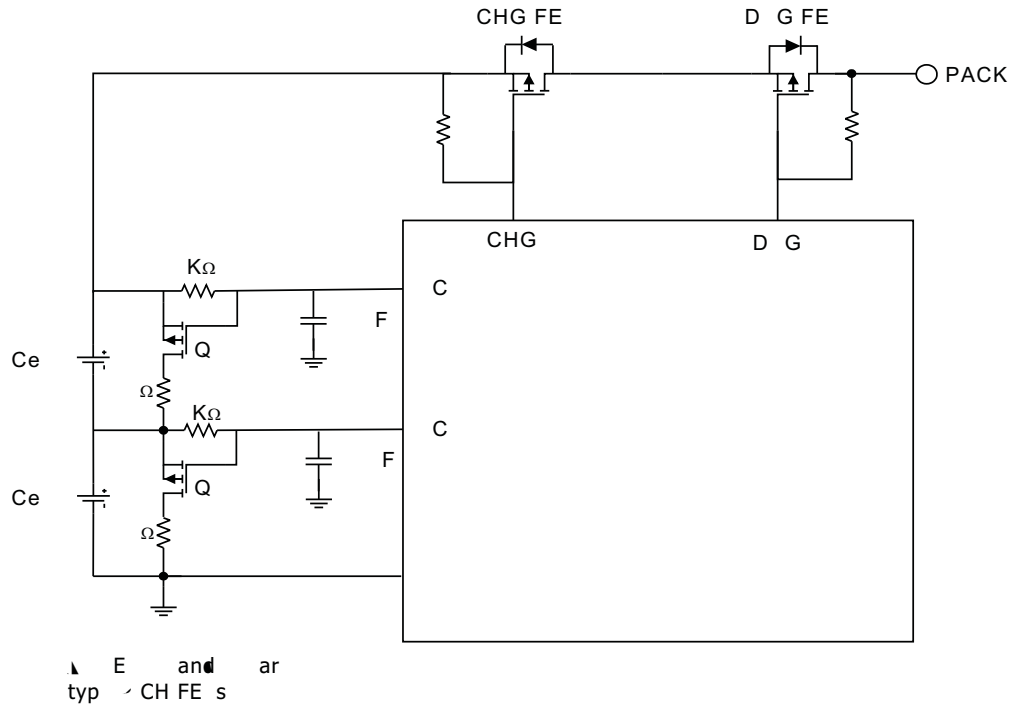


Figure 3. Internal Cell

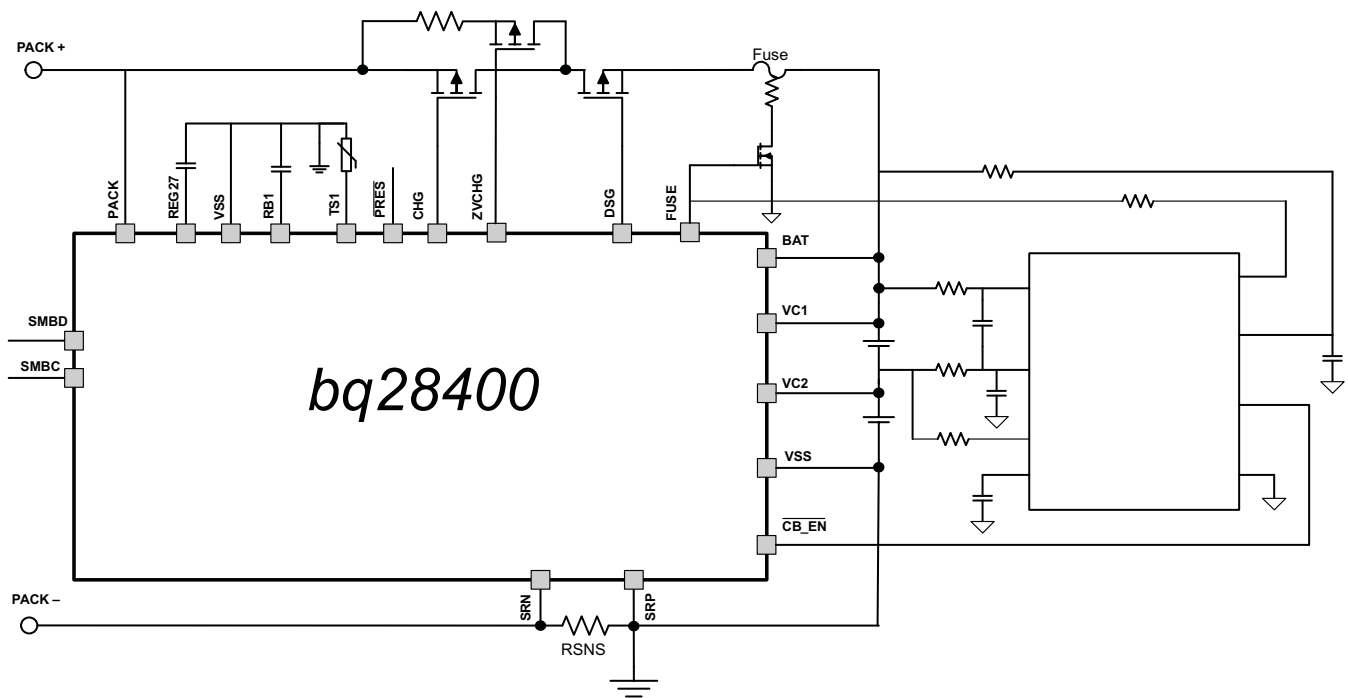




Figure 5. Application Schematic

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ28400PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ28400	Samples
BQ28400PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ28400	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information such as informati and Tlaccuracy c.9.625 9i7re0 -1] TJ ET q 1 0 0 1 0 332.908 cm BT /F381.574prov0 -1

MECHANICAL DATA

PLASTIC

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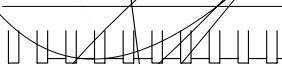
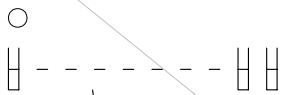
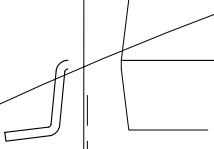
⊕ 0,10 (M)



0,15 NOM



0,25



0,15
0,05

⊕ 0,10

c in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

clude mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall



E. Falls within JEDEC MO-153



S
R

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IMPORTANT NOTICE

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