Voltage Protection for 2-Series, 3-Series, or 4-Series Cell Li-Ion Batteries (Second-Level Protection)

Check for Samples: bq29440, bq2944L0, bq29441, bq29442, bq29443, bq29449, bq2944L9

FEATURES

- **2-Series, 3-Series, or 4-Series Cell Secondary Protection**
- **External Capacitor-Controlled Delay Timer**
- **Low Power Consumption I_{CC} < 2 µA Typical [V_{CELL}(ALL) < $V_{PROTECT}$]**
- **High-Accuracy Overvoltage Protection: ±25 mV with T_A = 0°C to 60°C**
- **Fixed Overvoltage Protection Thresholds: 4.30 V, 4.35 V, 4.40 V, 4.45 V, 4.50 V**
- **Small 8L QFN Package**

APPLICATIONS

- **Second-Level Protection in Li-Ion Battery Packs**
  - **Notebook Computers**
  - **Power Tools**
  - **Portable Equipment and Instrumentation**

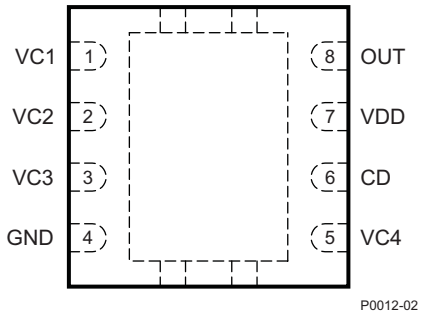
DESCRIPTION

The bq2944x is a secondary overvoltage protection IC for 2-series, 3-series, or 4-series cell Li-Ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit.

FUNCTION

The voltage of each cell in a battery pack is compared to an internal reference voltage. If any cells reach an overvoltage condition, the bq2944x device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low state to a high state. An optional latch configuration is available that holds the OUT pin in a high state indefinitely after an overvoltage condition has satisfied the specified delay timer period. The latch is released when the CD pin is shorted to GND.

DRB Package
(Top View)



P0012-02

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. ORDERING INFORMATION(1)

T_A	PART NUMBER	OUT PIN LATCH OPTION	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	OVP	ORDERING INFORMATION(2)	
							TAPE AND REEL (LARGE)(3)	TAPE AND REEL (SMALL)(4)
–40°C to +110°C	BQ29440	No	QFN-8	DRB	440	4.35 V	BQ29440DRBR	BQ29440DRBT
	BQ2944L0	Yes			44L0	4.35 V	BQ2944L0DRBR	BQ2944L0DRBT
	BQ29441	No			441	4.40 V	BQ29441DRBR	BQ29441DRBT
	BQ29442	No			442	4.45 V	BQ29442DRBR	BQ29442DRBT
	BQ29443	No			443	4.50 V	BQ29443DRBR	BQ29443DRBT
	BQ29449	No			449	4.30 V	BQ29449DRBR	BQ29449DRBT
	BQ2944L9	Yes			44L9	4.30 V	BQ2944L9DRBR	BQ2944L9DRBT

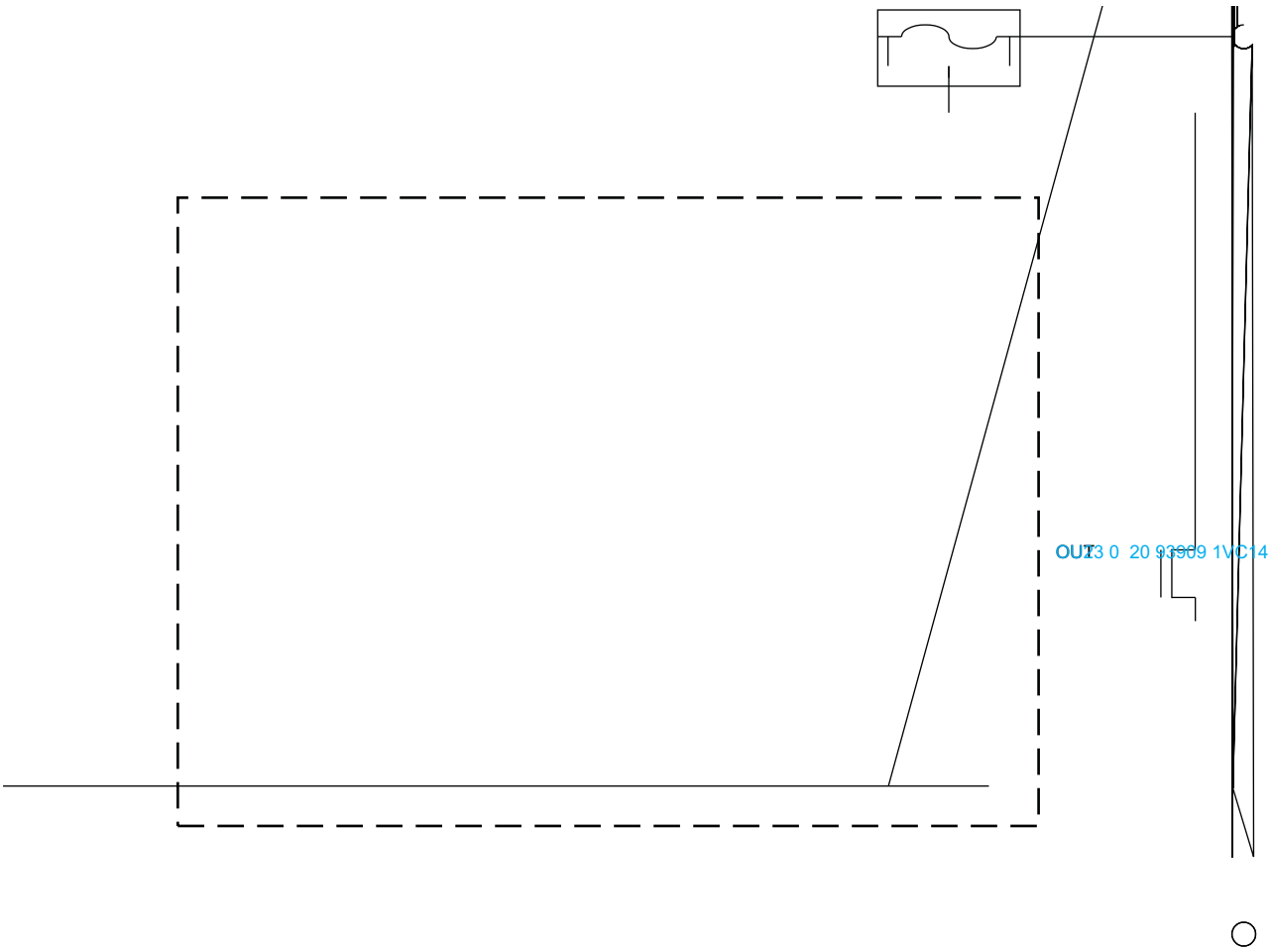
(1) Example: bq2944L0DRBR is a device with the OUT latch option with a V_{OV} threshold of 4.35 V. Contact Texas Instruments for other V_{OV} threshold options.
(2) For the most current package and ordering information, see the Package Addendum at the end of this document, or the TI website at www.ti.com.
(3) Large tape and reel quantity is 3,000 units.
(4) Small tape and reel quantity is 250 units.

THERMAL INFORMATION

THERMAL METRIC(1)		bq2944x DRB 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance(3)	25.1	
θ_{JB}	Junction-to-board thermal resistance(4)	19.3	
ψ_{JT}	Junction-to-top characterization		

Thermal-to-top (4)

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE/UNIT
Supply voltage range, V_{MAX}	VDD–GND	–0.3 to 28 V
Input voltage range, V_{IN}	VC1–GND, VC2–GND, VC3–GND	–0.3 to 28 V
	VC1–VC2, VC2–VC3, VC3–VC4, VC4–GND	–0.3 to 8 V
	CD–GND	–0.3 to 8 V
Output voltage range, V_{OUT}	OUT–GND	–0.3 to 28 V
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4		25	V
Input voltage range	VC1–VC2, VC2–VC3, VC3–VC4, VC4–GND	0		5	V
$t_{d(CD)}$ delay-time capacitance	C_{CD} (See Figure 7.)		0.1		µF
Voltage monitor filter resistance	R_{IN} (See Figure 7.)	0.1	1		k

RECOMMENDED OPERATING CONDITIONS (continued)

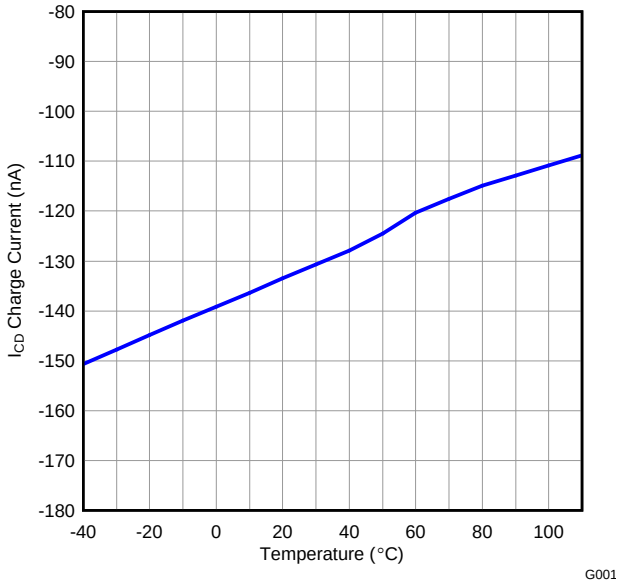
		MIN	NOM	MAX	UNIT
Voltage monitor filter capacitance	C_{IN} (See Figure 7.)	0.01	0.1		µF
Supply voltage filter resistance	R_{VD} (See Figure 7.)	0.1		1	k
Supply voltage filter capacitance	C_{VD} (See Figure 7.)		0.1		µF
Operating ambient temperature range, T_A		–40		110	°C

ELECTRICAL CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 17 V, MIN/MAX values stated where T_A = –40°C to 110°C and VDD = 4 V to 25 V (unless otherwise noted).

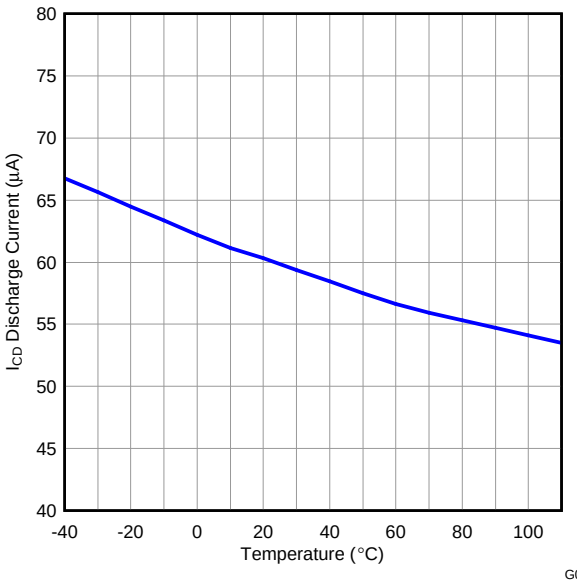
PARAMETER			TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{PROTECT}$	Overvoltage detection voltage	bq29440			4.35		V
		bq29441			4.40		
		bq29442			4.45		
		bq29443			4.50		
		bq29449			4.30		
V_{HYS}	Overvoltage detection	bq29449	For non-latch devices only				

I_{CD} CHARGE CURRENT vs TEMPERATURE



G001

I_{CD} DISCHARGE CURRENT vs TEMPERATURE



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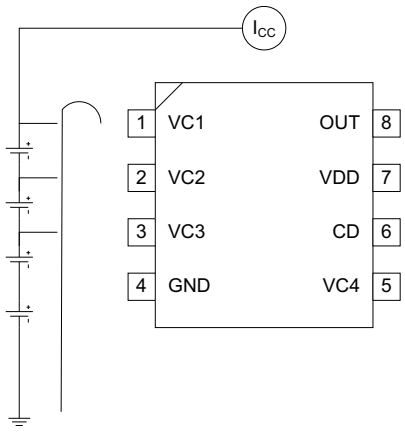


APPLICATIONS INFORMATION

PROTECTION (OUT) TIMING AND DELAY TIME CAPACITOR SIZING

The bq2944x uses an external capacitor to set delay timing during an overvoltage condition. When any of the cells exceed the overvoltage threshold, the bq2944x activates an internal current source of nominally 140 nA, which charges the external capacitor. When the external capacitor charges up to a voltage of nominally 1.2 V, the OUT pin transitions from a low state to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when I_{OH} = 0 mA.

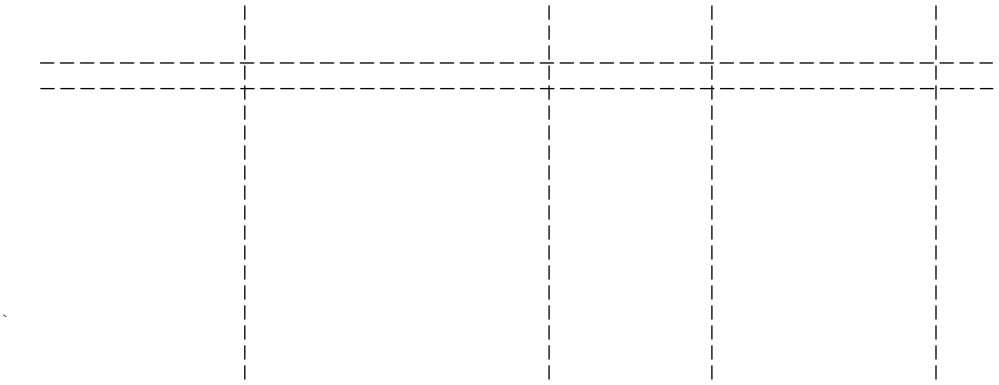


Figure 4. Timing for Overvoltage Sensing

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where t_d is the desired delay time and x_{DELAY} is the overvoltage delay time scale factor, expressed in seconds per microFarad. x_{DELAY} is nominally 9.0 s/µF. For example, if a nominal delay of 3 seconds is desired, the customer should use a C_{CD} capacitor that is 3 s/9.0 s/µF = 0.33 µF.

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

If the cell overvoltage condition is removed before the external capacitor reaches the reference voltage, the internal current source is disabled and an internal discharge block is employed to discharge the external capacitor down to 0 V. In this instance, the OUT pin remains in a low state.

For latched versions of the bq2944x, if an overvoltage condition has caused the OUT pin to transition to a high state, the external capacitor remains charged even after the overvoltage condition has been removed. In this instance, the OUT pin remains in a high state.

For non-latched versions, the OUT pin is allowed to transition back from a high to low state when the overvoltage condition is no longer present, and the external capacitor is discharged down to 0 V.

BATTERY CONNECTION FOR 2-SERIES, 3-SERIES, AND 4-SERIES CELL CONFIGURATIONS

Figure 5, Figure 6, and Figure 7 show the 2-series, 3-series, and 4-series cell configurations.

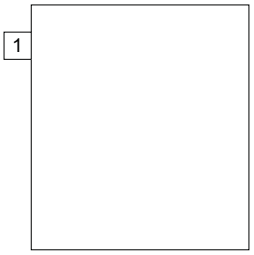


Figure 5. 2-Series Cell Configuration

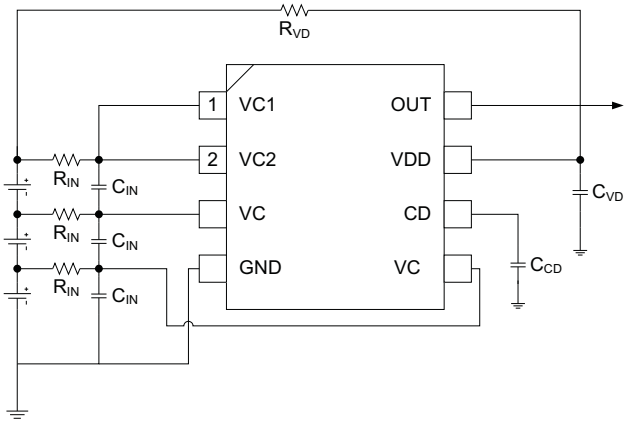


Figure 6. 3-Series Cell Configuration

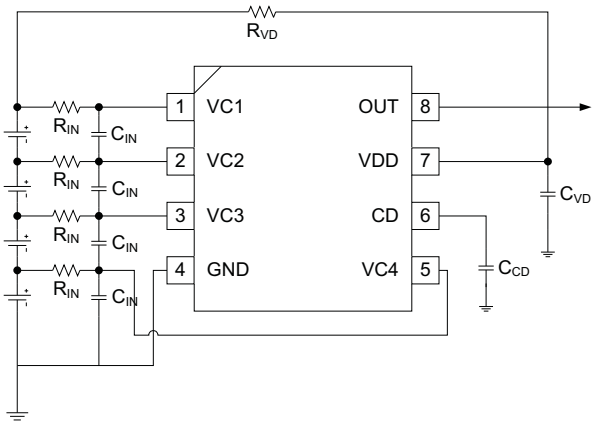


Figure 7. 4-Series Cell Configuration

CELL CONNECTION SEQUENCE

NOTE

Before

$$t_{d\_CTM} = C_{CD} \times X_{DELAY\_CTM}$$

REVISION HISTORY

Changes from Revision B (June 2010) to Revision C **Page**

- Added new protection thresholds 1
- Changed occurrences of V_{DD} to VDD throughout document 1
- Added part numbers 2
- Changed the Functional Block Diagram 3
- Changed the Electrical Characteristics 4
- Deleted 3.5 from one of the maximum values from the V_{OUT} specification 4
- Changed nominal delay time 6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ29440DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	440	
BQ29440DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	440	
BQ29441DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	441	
BQ29441DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	441	
BQ29442DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	442	
BQ29442DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	442	
BQ29443DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	443	
BQ29443DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	443	
BQ29449DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	449	
BQ29449DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	449	

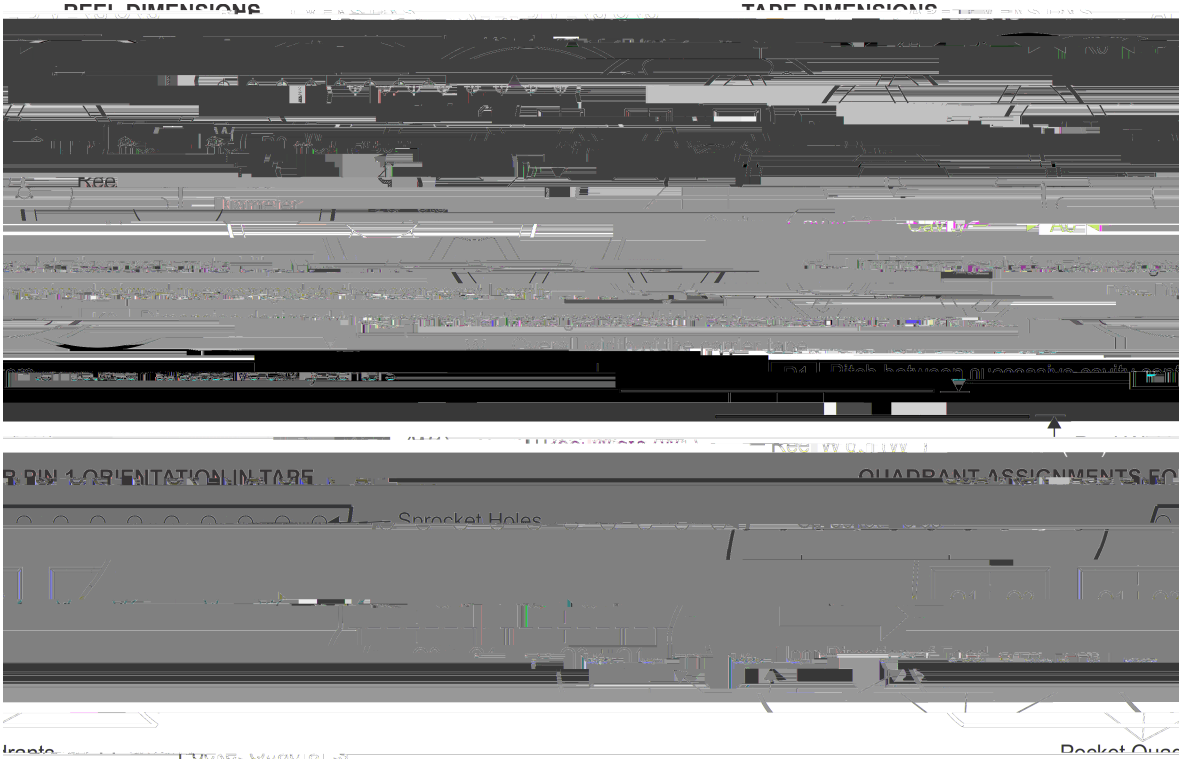
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

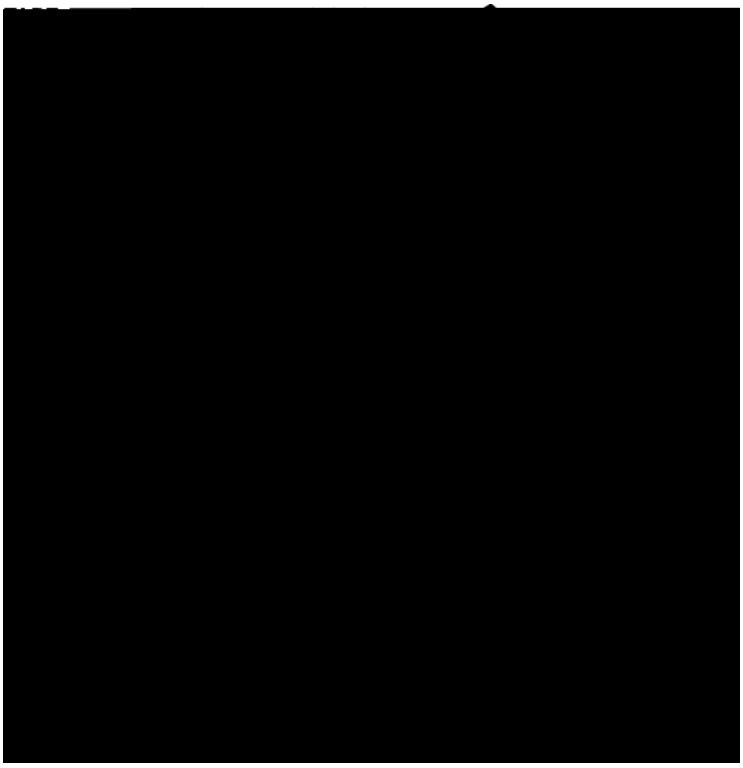
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION



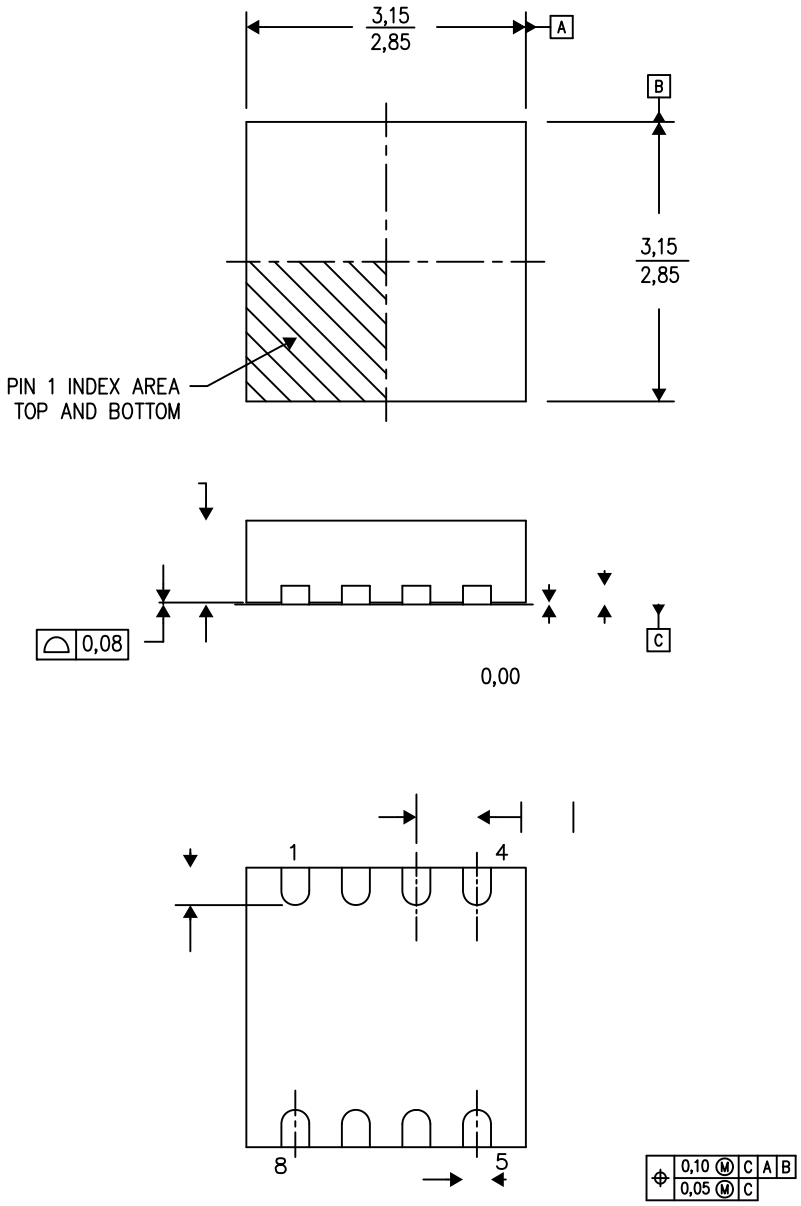
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29440DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29440DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29441DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29441DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29442DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29442DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29443DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29443DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29449DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29449DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29440DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29440DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29441DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29441DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29442DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29442DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29443DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29443DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29449DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29449DRBT	SON	DRB	8	250	210.0	185.0	35.0

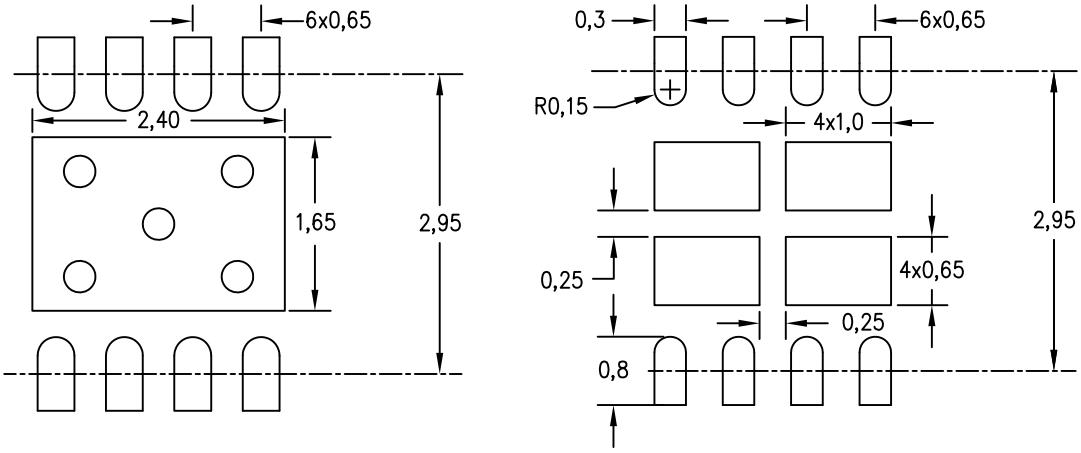


Bottom View

C1 VSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

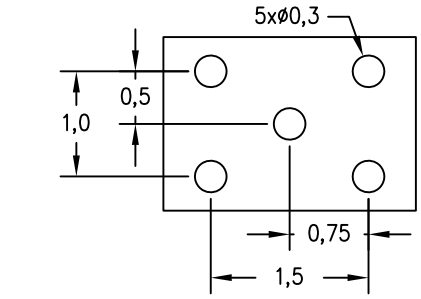
THERMAL PAD MECHANI



66% Printed Solder Coverage by Area

Center Pad Lav
(Note D)

Note D



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D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN o the Product Data Sheets

Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Γ

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