System-Side Impedance Track™ Fuel Gauge With Integrated LDO

Check for Samples: bq27520-G4

FEATURES

- **Single series cell Li-Ion battery fuel gauge resides on system board**
  - **Integrated 2.5 VDC LDO**
  - **External low-value 10 m sense resistor**
- **Patented Impedance Track™ technology**
  - **Adjusts for battery aging, self-discharge, temperature, and rate changes**
  - **Reports Remaining Capacity, State of Charge (SOC), and Time-to-Empty**
    - **Optional Smoothing Filter**
  - **Battery State of Health (aging) estimation**
  - **Supports embedded or removable packs with up to 32Ahr capacity**
    - **Accomodates pack swapping with 2 separate battery profiles**
- **Microcontroller peripheral supports:**
  - **400-kHz I²C ™ serial interface**
  - **32 Bytes of Scratch-Pad FLASH NVM**
  - **Battery Low digital ouptut warning**
  - **Configurable SOC Interrupts**
  - **External thermistor, internal sensor, or host reported temperature options**
- **Tiny 15-pin 2610 × 1956 µm, 0.5 mm pitch NanoFree™ (CSP) package**

APPLICATIONS

- **Smartphones, Feature phones and Tablets**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

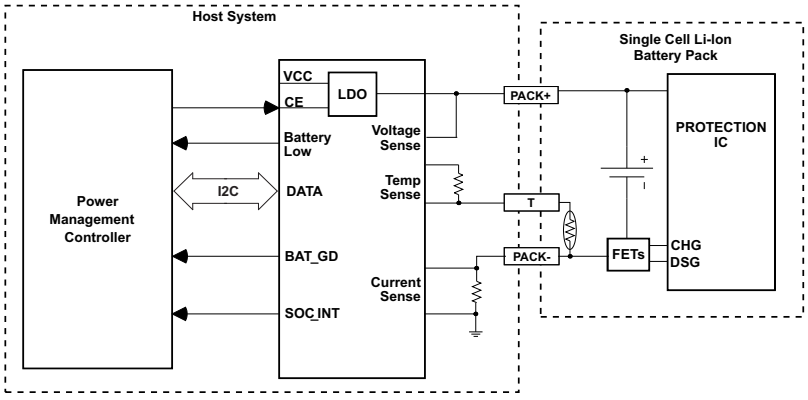
DESCRIPTION

The Texas Instruments bq27520-G4 system-side Li-Ion battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell Li-Ion battery packs. The device requires little system microcontroller firmware development. The bq27520-G4 resides on the system's main board and manages an embedded battery (non-removable) or a removable battery pack.

The bq27520-G4 uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), run-time to empty (min), battery voltage (mV), temperature (°C) and state of health (%).

Battery fuel gauging with the bq27520-G4 requires only PACK+ (P+), PACK– (P–), and optional Thermistor (T) connections to a removable battery pack or embedded battery circuit. The device uses a 15-ball NanoFree™ (CSP) package in the nominal dimensions of 2610 × 1956 µm with 0,5 mm lead pitch. It is ideal for space constrained applications.

TYPICAL APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PIN ASSIGNMENT AND PACKAGE DIMENSIONS

(TOP VIEW)

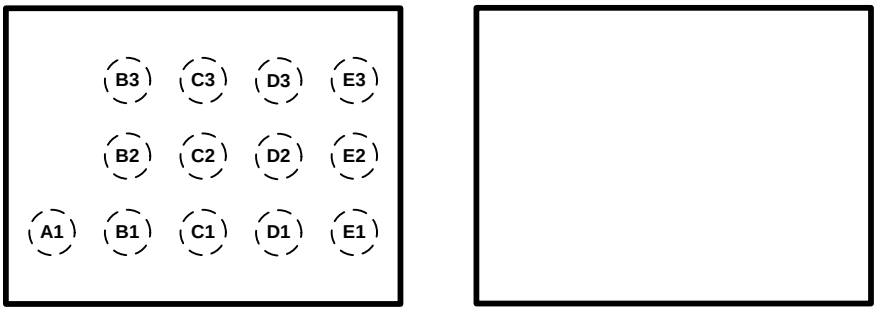


Table 1. PIN FUNCTIONS

PIN			

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		VALUE	UNIT
V_{REGIN}	Regulator input range	–0.3 to 5.5	V
		–0.3 to 6.0 (2)	V
V_{CE}	CE input pin	–0.3 to V_{REGIN} + 0.3	V
V_{CC}	Supply voltage range	–0.3 to 2.75	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, SOC_INT)	–0.3 to 5.5	V
V_{BAT}	BAT input pin	–0.3 to 5.5	V
		–0.3 to 6.0 (2)	V
V_I	Input voltage range to all other pins (BI/TOUT , TS , SRP, SRN, BAT_GD)	–0.3 to V_{CC} + 0.3	V
ESD	Human-body model (HBM), BAT pin	1.5	kV
	Human-body model (HBM), all other pins	2	
T_A	Operating free-air temperature range	–40 to 85	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Condition not to exceed 100 hours at 25 °C lifetime.

RECOMMENDED OPERATING CONDITIONS

T_A = -40°C to 85°C, V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REGIN}	Supply voltage	No operating restrictions	2.8		4.5	V
		No FLASH writes	2.45		2.8	
C_{REGIN}	External input capacitor for internal LDO between REGIN and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO25}	External output capacitor for internal LDO between V_{CC} and V_{SS}		0.47	1		µF
t_{PUCD}	Power-up communication delay			250		ms

SUPPLY CURRENT

T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} (1)	Normal operating-mode current	Fuel gauge in NORMAL mode. I_{LOAD} > ***Sleep Current***		118		µA
I_{SLP+} (1)	Sleep+ operating mode current	Fuel gauge in SLEEP+ mode. I_{LOAD} < ***Sleep Current***		62		µA
I_{SLP} (1)	Low-power storage-mode current	Fuel gauge in SLEEP mode. I_{LOAD} < ***Sleep Current***		23		µA
I_{HIB} (1)	Hibernate operating-mode current	Fuel gauge in HIBERNATE mode. I_{LOAD} < ***Hibernate Current***		8		µA

(1) Specified by design. Not production tested.

ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{A1}	Input voltage range (TS)		V_{SS} – 0.125		2	V
V_{A2}	Input voltage range (BAT)		V_{SS} – 0.125		5	V
$V_{IN(ADC)}$	Input voltage range		0.05		1	V
G_{TEMP}	Internal temperature sensor voltage gain			–2		mV/°C
t_{ADC_CONV}	Conversion time				125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
Z_{ADC1} (1)	Effective input resistance (TS)		8			MΩ
Z_{ADC2} (1)	Effective input resistance (BAT)	bq27520-G4 not measuring cell voltage	8			MΩ
		bq27520-G4 measuring cell voltage		100		kΩ
$I_{lkg(ADC)}$ (1)	Input leakage current				0.3	µA

(1) Specified by design. Not tested in production.

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR}	Input voltage range, $V_{(SRN)}$ and $V_{(SRP)}$	V_{SR} = $V_{(SRN)}$ – $V_{(SRP)}$	–0.125		0.125	V
t_{SR_CONV}	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV
INL	Integral nonlinearity error			±0.007	±0.034	% FSR
$Z_{IN(SR)}$ (1)	Effective input resistance		2.5			MΩ
$I_{lkg(SR)}$ (1)	Input leakage current				0.3	µA

(1) Specified by design. Not tested in production.

DATA FLASH MEMORY CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR} (1)	Data retention		10			Years
	Flash-programming write cycles (1)		20,000			Cycles
$t_{WORDPROG}$ (1)	Word programming time				2	ms
I_{CCPROG} (1)	Flash-write supply current			5	10	mA
$t_{DFERASE}$ (1)	Data flash master erase time		200			ms
$t_{IFERASE}$ (1)	Instruction flash master erase time		200			ms
$t_{PGERASE}$ (1)	Flash page erase time		20			ms

(1) Specified by design. Not production tested

I²C-COMPATIBLE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse duration (high)		600			ns
$t_{w(L)}$	SCL pulse duration (low)		1.3			µs
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{su(DAT)}$	Data setup time		100			ns
$t_{h(DAT)}$	Data hold time		0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
$t_{(BUF)}$	Bus free time between stop and start		66			µs
f_{SCL}	Clock frequency (1)				400	kHz

(1) If the clock frequency (f_{SCL}) is > 100 kHz, use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to I²C INTERFACE and I²C Command Waiting Time)

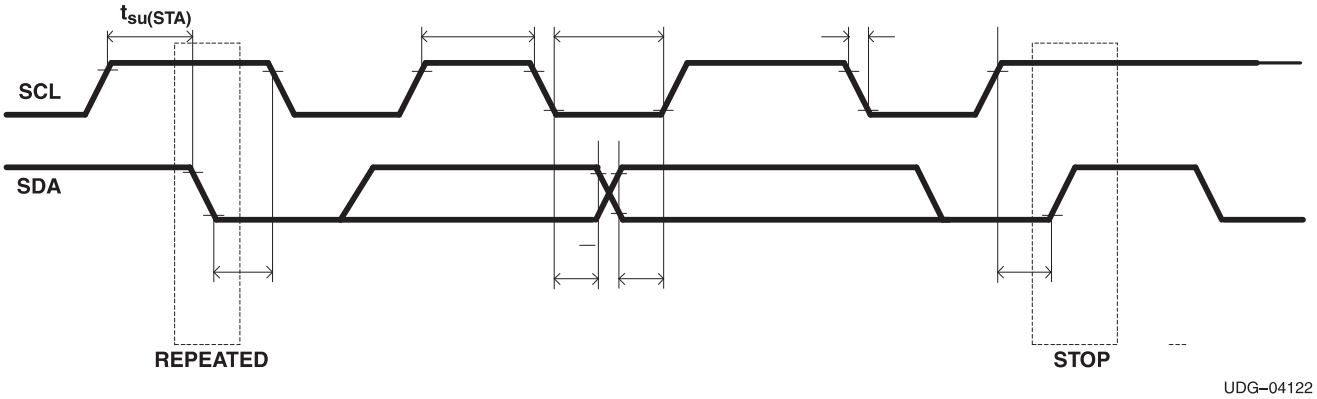


Figure 1. I²C-Compatible Interface Timing Diagrams

Control( ): 0x00/0x01

Issuing a *Control( )* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control( )* command allows the system to control specific features of the bq27520-G4 during normal operation and additional features when the device is in different access modes, as described in Table 3. Additional details are found in the *bq27520-G4 Technical Reference Manual*.

Table 3. *Control( )* Subcommands

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of DF checksum, hibernate, IT, etc.
DEVICE_TYPE	0x0001	Yes	Reports the device type (eg: 0x0520)
FW_VERSION	0x0002	Yes	Reports the firmware version on the device type
PREV_MACWRITE	0x0007	Yes	Returns previous *Control( )* subcommand code
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track™ configuration
OCV_CMD	0x000c	Yes	Request the gauge to take a OCV measurement
BAT_INSERT	0x000d	Yes	Forces *Flags( ) [BAT_DET]* bit set when ***OpConfig B [BIE]*** = 0
BAT_REMOVE	0x000e	Yes	Forces *Flags( ) [BAT_DET]* bit clear when ***OpConfig B [BIE]*** = 0
SET_HIBERNATE	0x0011	Yes	Forces *CONTROL_STATUS [HIBERNATE]* to 1
CLEAR_HIBERNATE	0x0012	Yes	Forces *CONTROL_STATUS [HIBERNATE]* to 0
SET_SLEEP+	0x0013	Yes	Forces *CONTROL_STATUS [SNOOZE]* to 1
CLEAR_SLEEP+	0x0014	Yes	Forces *CONTROL_STATUS [SNOOZE]* to 0
DF_VERSION	0x001F	Yes	Returns the ***Data Flash Version*** code
SEALED	0x0020	No	Places the bq27520-G4 in SEALED access mode
IT_ENABLE	0x0021	No	Enables the Impedance Track™ (IT) algorithm
RESET	0x0041	No	Forces a full reset of the bq27520-G4

FUNCTIONAL DESCRIPTION

The bq27520-G4 measures the voltage, temperature, and current to determine battery capacity and state of charge (SOC) based on the patented Impedance Track™ algorithm (Refer to Application Report SLUA450, *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* for more information). The bq27520-G4 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in series with the battery. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge.

Battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When a system load is applied, the impedance of the battery is measured by comparing the open circuit voltage (OCV) obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and chemical capacity (Qmax). The initial Qmax values are taken from a cell manufacturers' data sheet multiplied by the number of parallel cells. It is also used for the value in ***Design Capacity***. The bq27520-G4 acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the Qmax value, to determine *FullChargeCapacity( )* and *StateOfCharge( )*, specifically for the present load and temperature. *FullChargeCapacity( )* is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage( )* reaches the ***Terminate Voltage***. *NominalAvailableCapacity( )* and *FullAvailableCapacity( )* are the uncompensated (no or light load) versions of *RemainingCapacity( )* and *FullChargeCapacity( )* respectively.

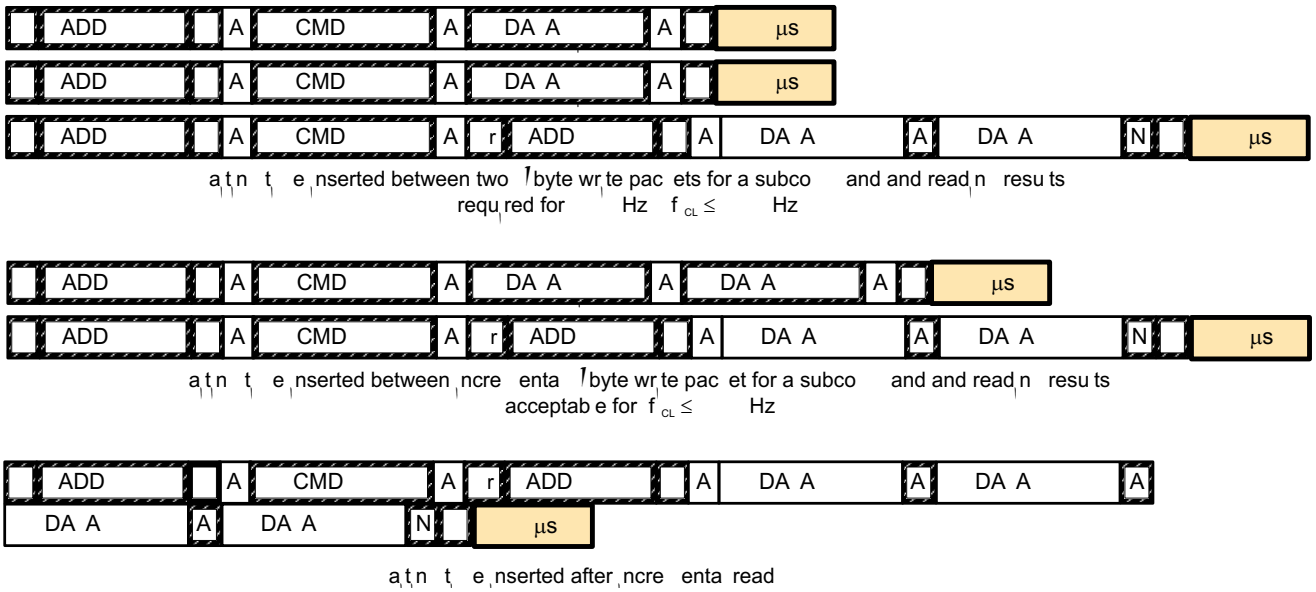
The bq27520-G4 has two *Flags( )* bits and two pins to warn the host if the battery's SOC has fallen to critical levels. If *RemainingCapacity( )* falls below the first capacity threshold specified by ***SOC1 Set Threshold***, the *Flags ( ) [SOC1]* bit is set and is cleared if *RemainingCapacity( )* rises above the ***SOC1 Clear Threshold***. If enabled via ***OpConfig C [BATLSPUEN]***, the BAT_LOW pin reflects the status of the *[SOC1]* flag bit. Also, if enabled by ***OpConfig B [BL_INT]***, the SOC_INT will toggle upon a state change of the *[SOC1]* flag bit.

As *Voltage( )* falls below the ***SysDown Set Volt Threshold***, the *Flags( ) [SYSDOWN]* bit is set and SOC_INT will toggle once to provide a final warning to shut down the system. As *Voltage( )* rises above ***SysDown Clear Voltage*** the *[SYSDOWN]* bit is cleared and SOC_INT will toggle once to signal the status change.

Additional details are found in the *bq27520-G4 Technical Reference Manual*.

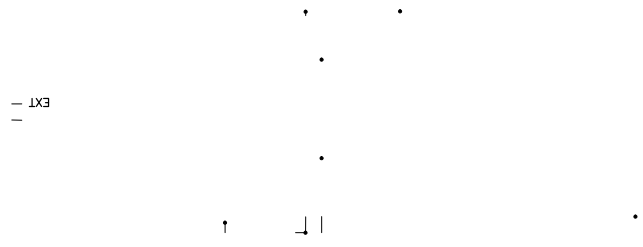
I²C Command Waiting Time

To ensure proper operation at 400 kHz, a $t_{(BUF)}$ ≥ 66 µs bus free waiting time should be inserted between all packets addressed to the bq27520-G4 . In addition, if the SCL clock frequency (f_{SCL}) is > 100 kHz, use individual 1-byte write commands for proper data flow control. The following diagram shows theco2 Tz 0 f 123.5 Tz 0 0 0 rg 54 67(



REFERENCE SCHEMATICS

SCHEMATIC



PACKAGING INFORMATION

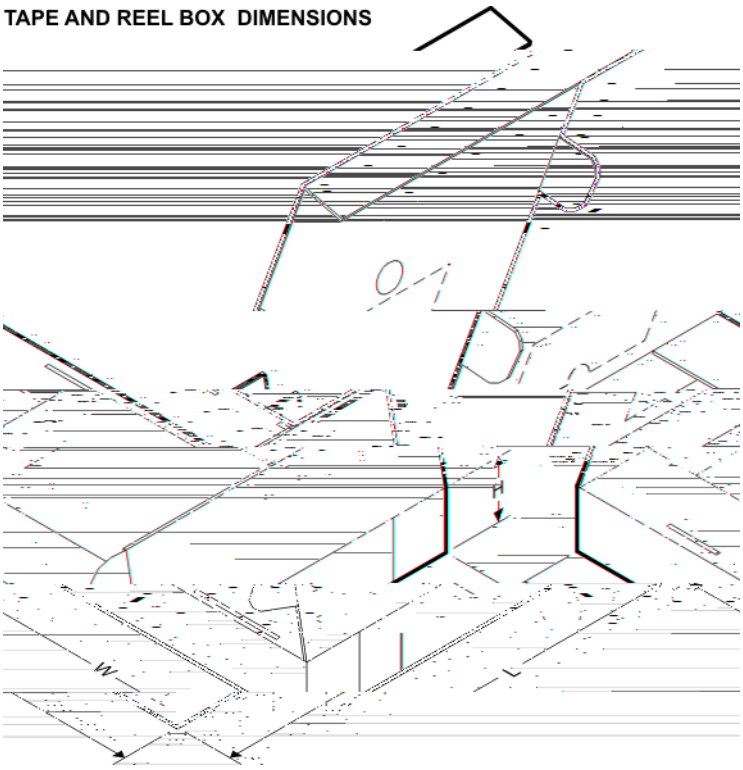
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27520YZFT-G4	DSBGA	YZF	15	250	180.0	8.4	2.1	2.76	0.81	4.0	8.0	Q1

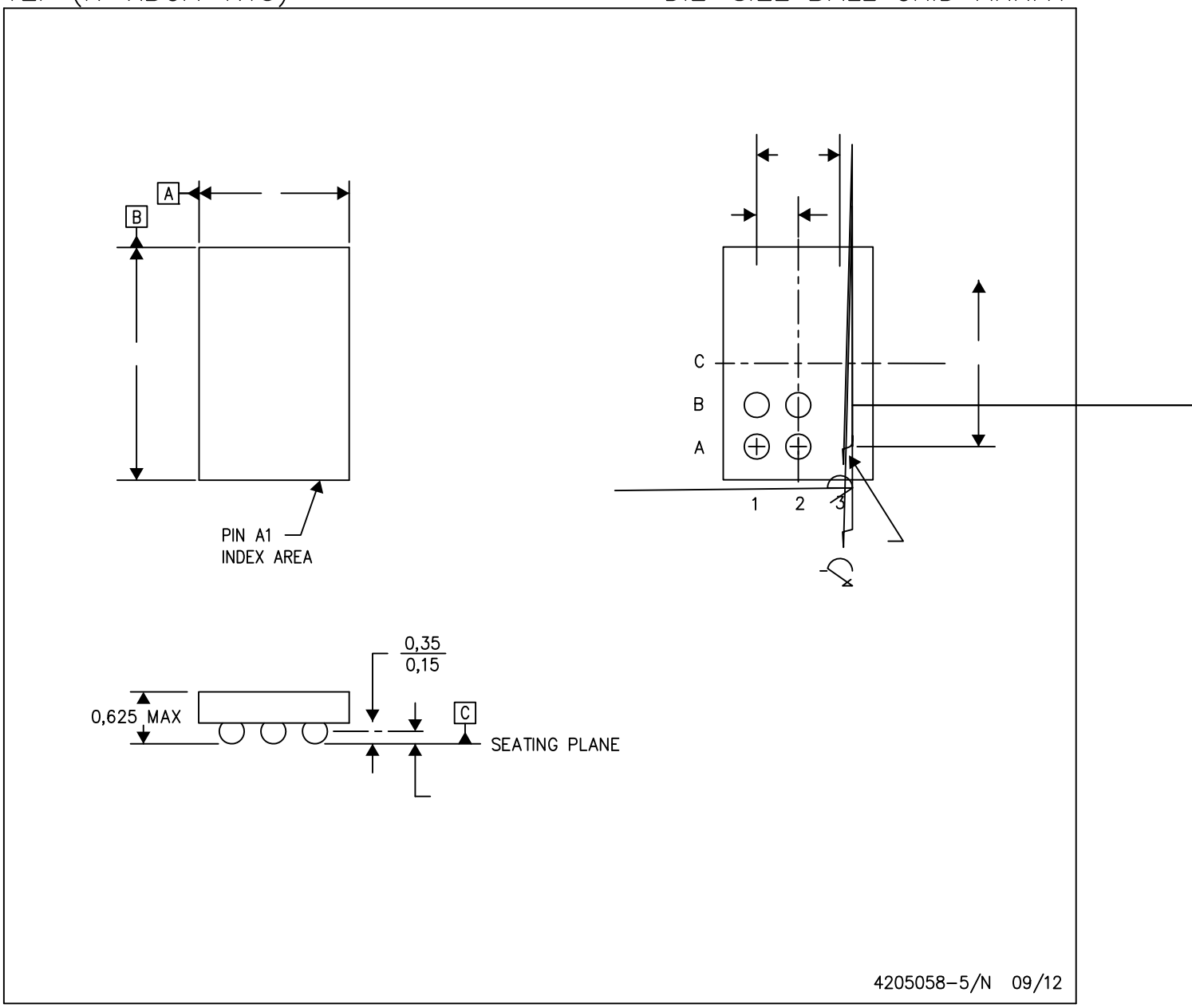
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27520YZFT-G4	DSBGA	YZF	15	250	210.0	185.0	35.0

YZF (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY



NOTES:

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265