3-Phase Brushless Motor Driver

Check for Samples: DRV3211-Q1

FEATURES

- **3-Phase Pre-drivers for N-channel MOS Field Effect Transistors (MOSFETs)**
- **Pulse Width Modulation (PWM) Frequency up to 20 kHz**
- **Fault Diagnostics**
- **Charge Pump**
- **Phase Comparators**
- **Phase Monitoring Sample and Hold Op-Amps**
- **Central Processing Unit (CPU) Reset Generator**
- **Serial Port I/F (SPI)**
- **Motor Current Sense**
- **80-pin HTQFP**
- **5-V Regulator**

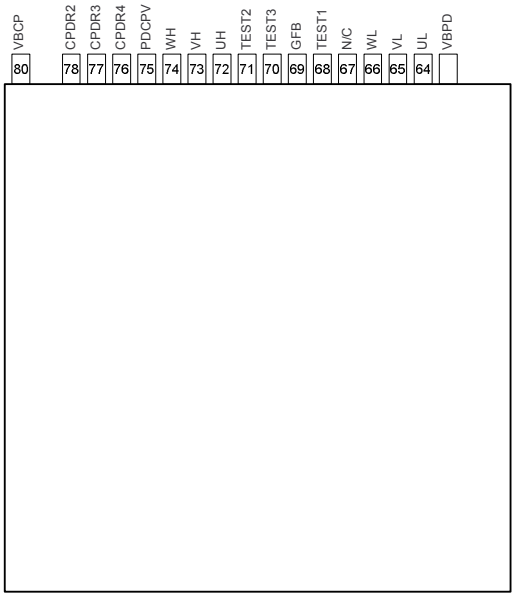
APPLICATIONS

- **Automotive**

DESCRIPTION

The DRV3211-Q1 device is a field effect transistor (FET) pre-driver designed for 3-phase motor control and its application such as an oil pump or a water pump. It is equipped with three high-side pre-FET drivers and three low-side drivers which are controlled by an external microcontroller (MCU). The power for the high side is supplied by a charge pump and no bootstrap cap is needed. For commutation, this integrated circuit (IC) sends a conditional motor drive signal and output to the MCU. Diagnostics provide undervoltage, overvoltage, overcurrent, overtemperature and power bridge faults. The motor current can be measured using an integrated current sense amplifier and comparator in a battery common-mode range, which allows the motor current to be used in a high-side current sense application. Gain is attained by external resistors. If the MCU does not have enough bandwidth, the phase monitoring sample and hold amplifiers can hold phase information until the MCU is ready to process it. The pre-driver and other internal settings can be configured through the SPI interface.

PINOUT



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BLOCK DIAGRAM

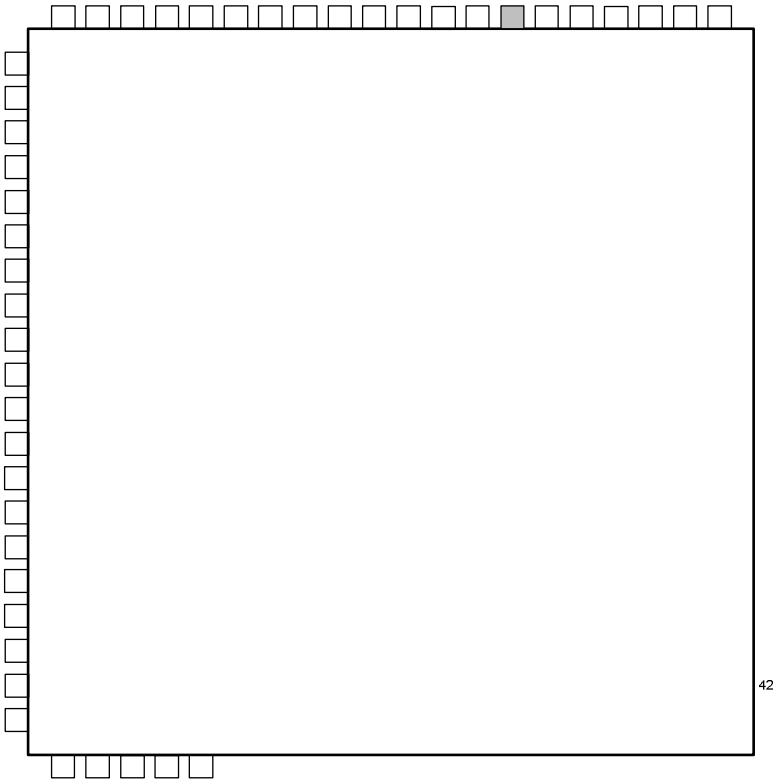

Figure 1. Top Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNITS
ESD(1)					
ESD all pins	ESD performance of all pins to any other pin	HBM model	–2	2	kV
		CDM model	–500	500	V
TEMPERATURE					
T_A	Operating temperature range		-40	125	degree
T_J	Junction temperature		-40	150	degree
T_s	Storage temperature		–55	150	degree

(1) ESD testing is performed according to the ACE-Q100 standard.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV3202-Q1	UNIT
		HTQP (80-PIN)	
θ_{JA}	Junction-to-ambient thermal resistance	23.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	7.5	
θ_{JB}	Junction-to-board thermal resistance	7.6	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	7.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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SUPPLY VOLTAGE AND CURRENT

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUT						
VB	VB Supply voltage		5.3	12	18	V
I_{VB}	VB Operating current	VB = 5.3 ~18 V, No PWM		20	35	mA

WATCHDOG

Description

The watchdog monitors the PRN signal and V_{CC} supply level and generates a reset to the MCU through the $\overline{RES}$ pin if the status of the PRN is not normal or the V_{CC} is lower than the specified threshold level. The watchdog can be disabled if $\overline{WDEN}$ is set high.

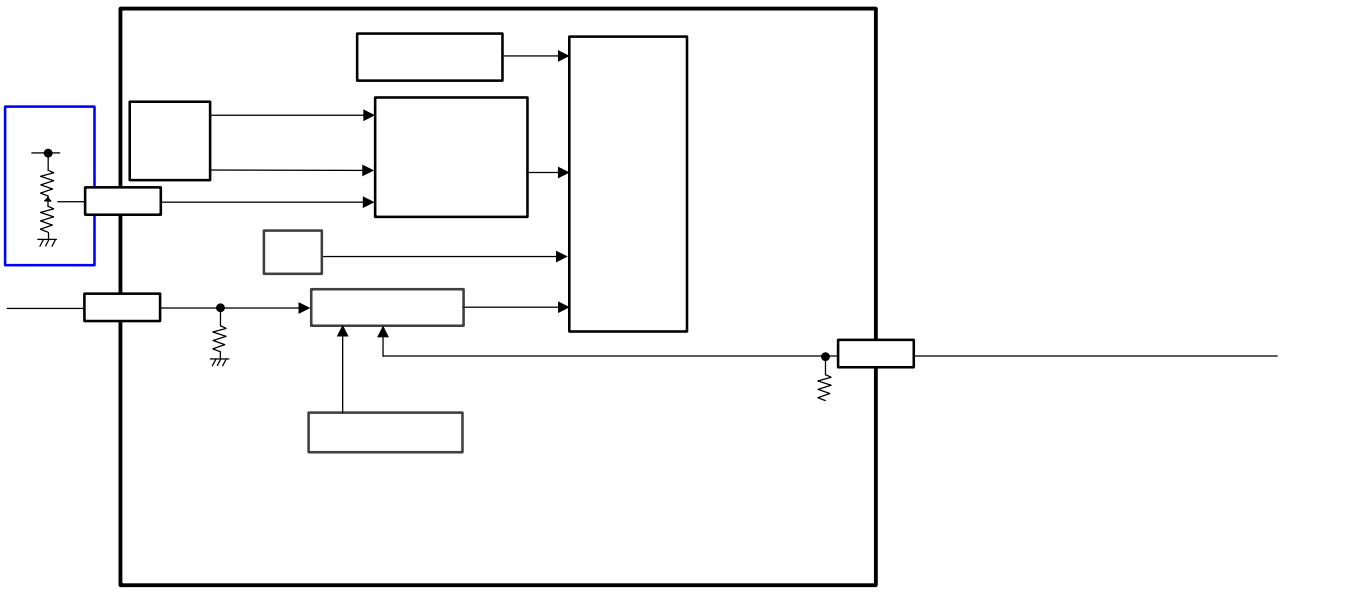
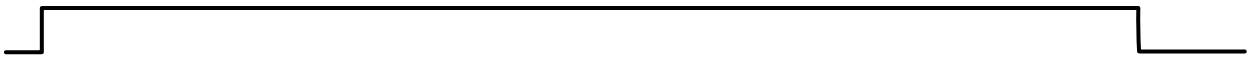


Figure 2. Watchdog Block Diagram



NOTE: $\overline{WDEN}$ = High, V_{CC} undervoltage condition sets $\overline{RES}$ = Low

Figure 3. Watchdog Timing Chart

WATCHDOG ELECTRICAL CHARACTERISTICS(1)

VB = 12 V,T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER(2)		CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG						
VSTN	Function start V_{CC} voltage $\overline{RES}$	Refer to Figure 3	–	0.8	1.3	V
t_{ON}	Power-on time $\overline{RES}$		32	40	48	ms
t_{OFF}	Clock off reset time $\overline{RES}$		64	80	96	ms
t_{RL}	Reset pulse low time $\overline{RES}$		16	20	24	ms
t_{RH}	Reset pulse high time $\overline{RES}$		64	80	96	ms
t_{RES}	Reset delay time $\overline{RES}$		30	71.5	90	µs
P_{wth}	Pulse width PRN		200	–	–	ns

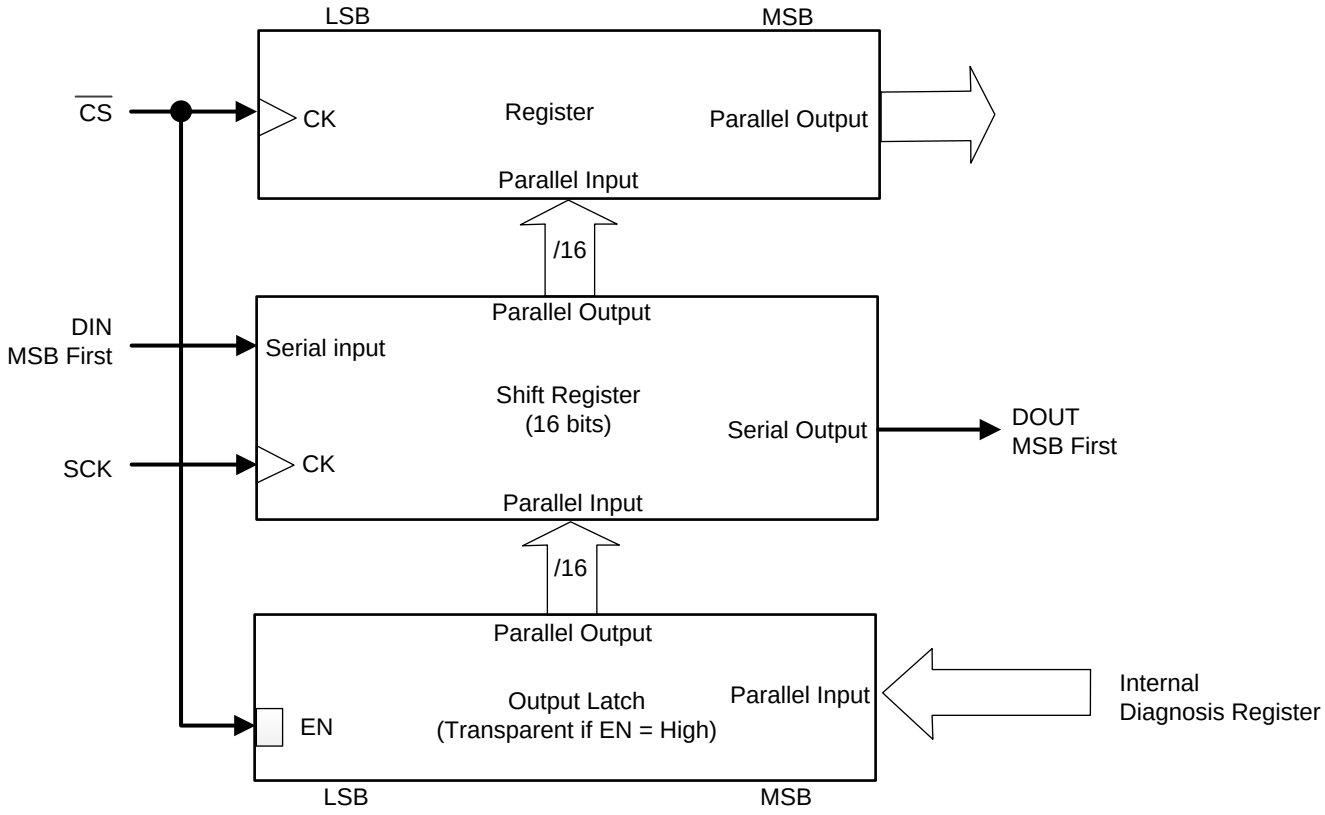
(1) The watchdog function is disabled and the timing parameters are invalid when the $\overline{WDEN}$ is at a high level.
(2) Specified by design

PRODUCT PREVIEW

SERIAL PORT I/F

Description

The SPI is used to receive an input byte from CPU and to transmit an output byte to CPU. Four signals are utilized according to the utilized



- **DIN – Serial Input Data**
  - This input signal is used to receive 16-bit data.
  - The bits are received in order from the MSB (first) to the LSB (last).
  - The pin has an internal pullup.
- **DOUT – Serial Output Data**
  - This output signal is used to transmit 16-bit data.
  - It is a 3-state output and it is in high impedance mode when $\overline{CS}$ is high.
  - The serial data bits are transmitted in order from the MSB (first) to the LSB (last).

SPI ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER[1]		CONDITIONS	MIN	TYP	MAX	UNITS
SPI						
F_{op}	Operating frequency	Refer to Figure 6	DC	–	4	MHz
T_{lead}	Enable lead time		100	–	–	ns
T_{wait}	Wait time between two successive communications		5	–	–	µs
T_{lag}	Enable lag time		100	–	–	ns
T_{pw}	SCLK pulse width		100	–	–	ns
T_{su}	Data setup time		80	–	–	ns
T_h	Data hold time		80	–	–	ns
T_{dis}	Disable time		–	–	80	ns
T_{del}	Data delay time (SCK to DOUT)	C_L = 50 pF, Refer to Figure 6	–	–	80	ns

(1) Specified by design

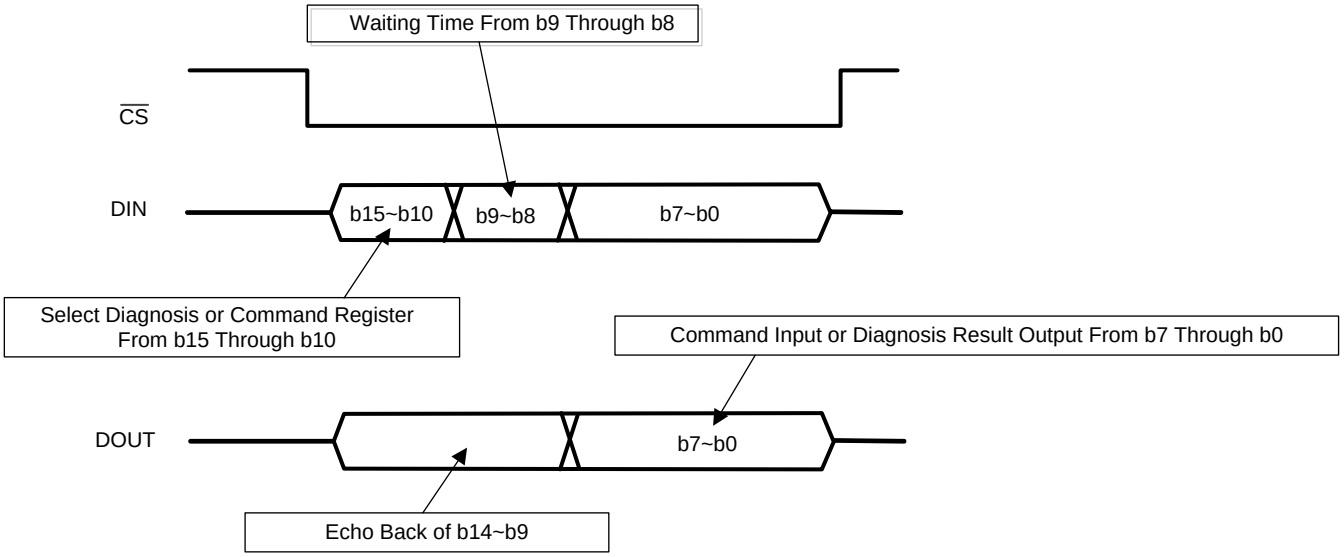


Figure 5. SPI Bit Sequence

PRODUCT PREVIEW

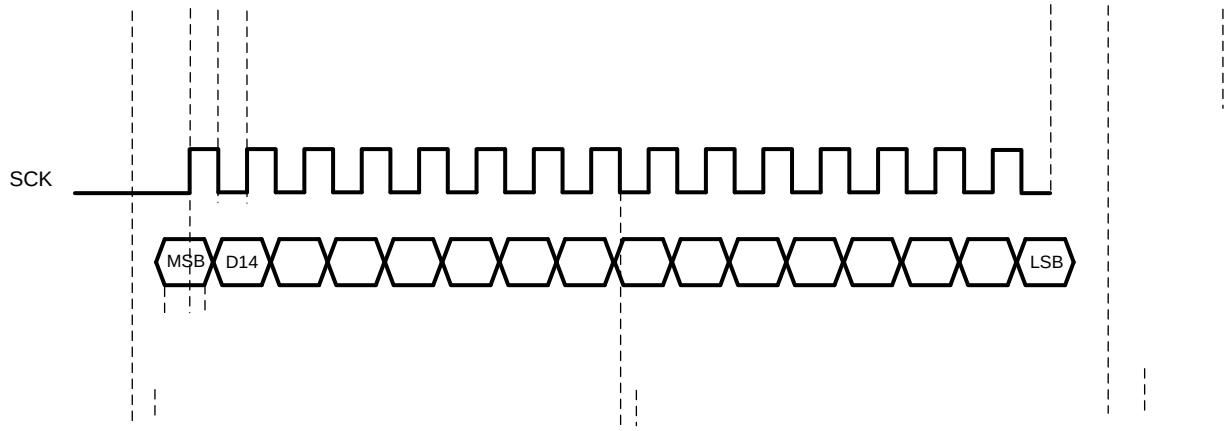


Figure 6. SPI AC Timing Definition

Table 1. SPI Bit Map (DIN)

ITEM	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
COMMAND1	0	0	0	0	0	1	–	–	SHM	SRT	–	–	–	–	–	–
COMMAND2	0	0	0	0	1	0	–	–	AG1	AG0	–	–	–	–	–	–
COMMAND3	0	0	0	0	1	1	–	–	–	–	–	–	–	–	–	–
DIAG_READ1	0	0	1	0	0	0	–	–	–	–	–	–	–	–	–	–
DIAG_READ2	0	1	0	0	0	0	–	–	–	–	–	–	–	–	–	–
DIAG_READ3	0	1	1	0	0	0	–	–	–	–	–	–	–	–	–	–

In Table 1, the B15–B10

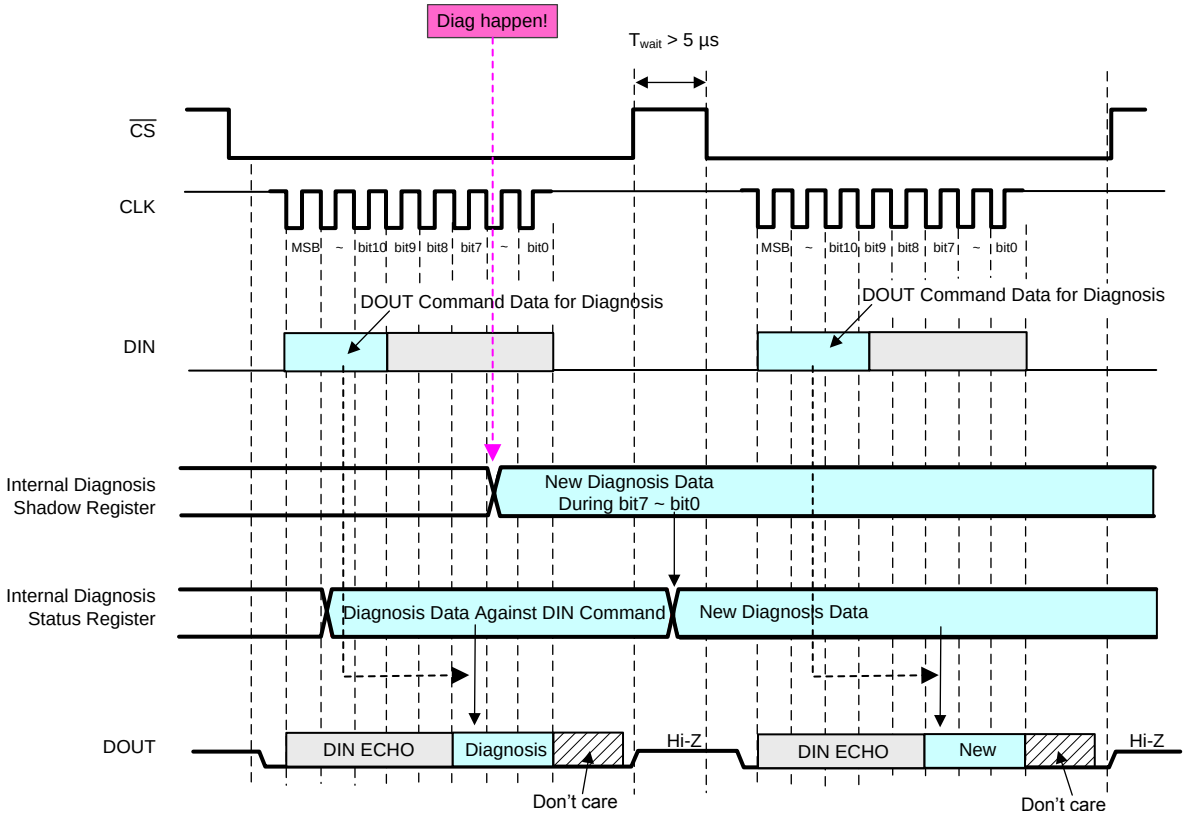


Figure 7. DIAG_READ

Internal Diagnosis Register (Status Register and Shadow Register)

If the diagnosis happens during the SPI communication, the function follows this protocol:

The diagnosis information is stored in the shadow register when the diagnosis happens.

After the output of the previous information a new diagnosis is sent from the shadow to the status register, and both registers are output through the DOUT

CHARGE PUMP

Description

The charge pump block generates the supply for high-side and low-side pre-drivers to maintain the gate voltage on the external FETs. External storage cap (CCP) and bucket caps (C1, C2) are used to support pre-driver slope and switching frequency requirements. R1 and R2 can reduce switching current if required. The charge pump has a voltage supervisor for over and undervoltage, and a selectable stop condition for pre-drivers.

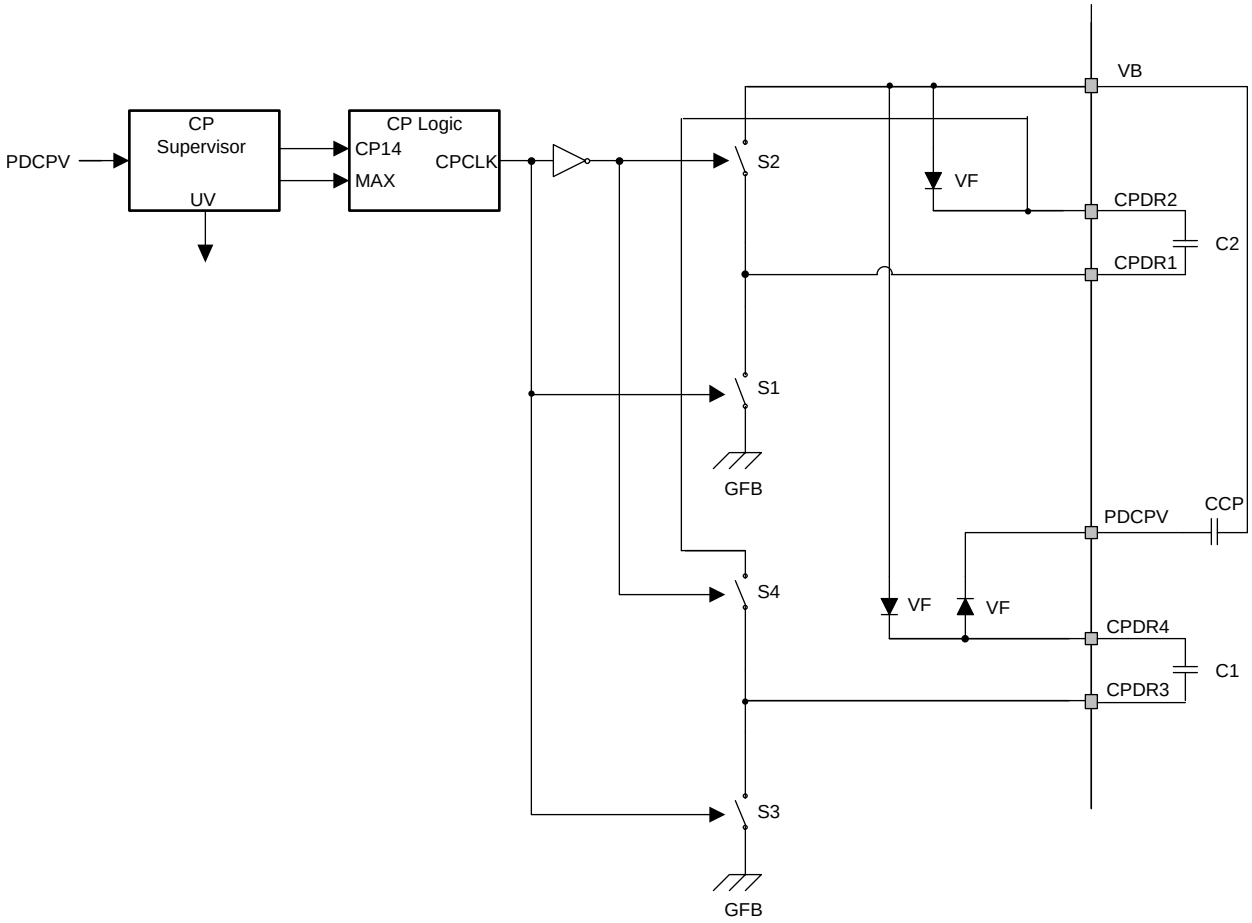


Figure 8. Charge Pump Block Diagram

CHARGE PUMP ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE PUMP						
V_{chv1_0}	Output voltage	VB = 5.3 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 7	VB + 8	VB + 9	V
V_{chv1_1}		VB = 5.3 V, I_{load} = 5 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 6	VB + 7	VB + 8	V
V_{chv1_2}		VB = 5.3 V, I_{load} = 8 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 5	VB + 6	VB + 7	V
V_{chv2_0}		VB = 12 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv2_1}		VB = 12 V, I_{load} = 11 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv2_2}		VB = 12 V, I_{load} = 18 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 12.5	VB + 13.5	VB + 15	V
V_{chv3_0}		VB = 18 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv3_1}		VB = 18 V, I_{load} = 13 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv3_2}		VB = 18 V, I_{load} = 22 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chvmax}	Maximum voltage		35	37.5	40	V
V_{chvUV}	Undervoltage detection threshold		VB + 4	VB + 4.5	VB + 5	V
T_{chv}(2)	Rise time	VB = 5.3 V, C1 = C2 = 47 nF, CCP = 2.2 µF, V_{chvUV} released		1	2	ms
R_{on}	On resistance S1~S4			8		Ω

(1) No variation of the external components
(2) Specified by design

PRE-DRIVER

Description

The pre-driver block provides three high-side pre-drivers and three low-side pre-drivers to drive external N-channel MOSFETs. The turn on side of the high-side pre-drivers supply the large N-channel transistor current to quickly charge and PMOS support output voltage up to PDCPV. The turn off side supplies the large N-channel transistor current to quickly discharge, while the low-side pre-drivers supply the large N-channel transistor current for charge and discharge. The output voltage of the low-side pre-driver is controlled by VB and it has VGS protection to make less than 18 V. The pre-driver has a stop condition in some fault conditions ($16 Error Detection).

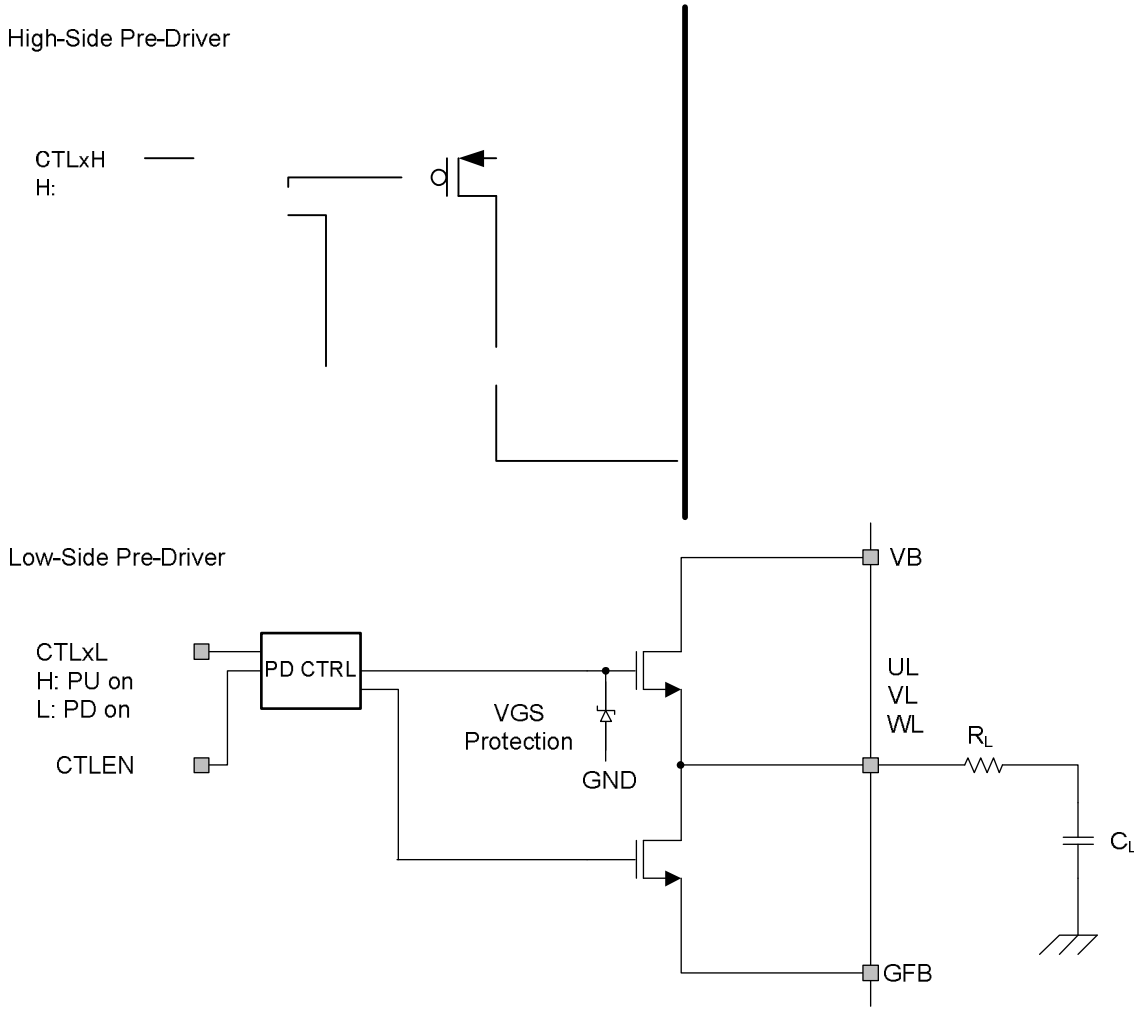


Figure 9. Pre-driver Block Diagram

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PRE-DRIVER ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER	CONDITIONS		

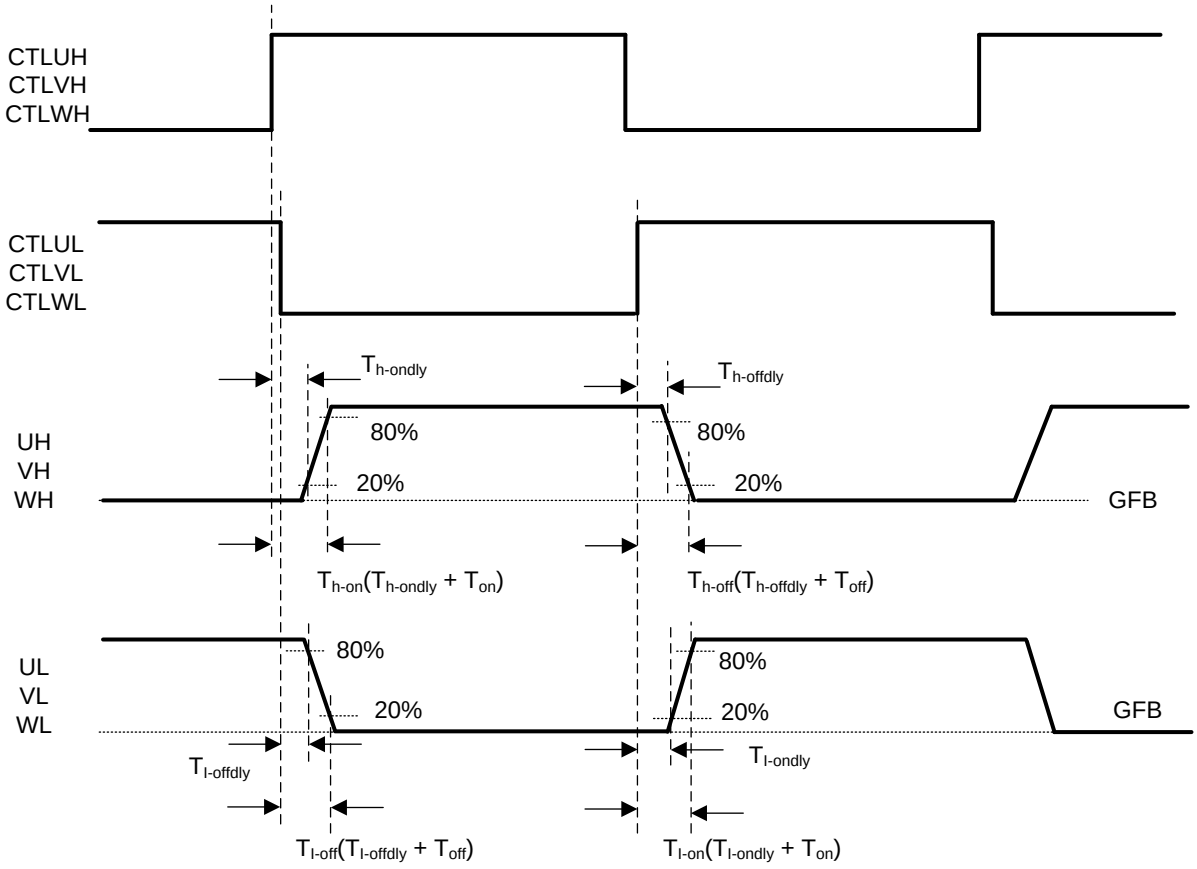

Figure 10. Delay Time from Input to Output

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PHASE COMPARATOR

Description

A 3-channel comparator module monitors the external FET by detecting voltage across the drain-source for high-side and low-side FETs. PHTM is the threshold level of comparators usable for sensorless communication. Figure 11 shows an example of the threshold level. There is no detection when CTLEN = Low.

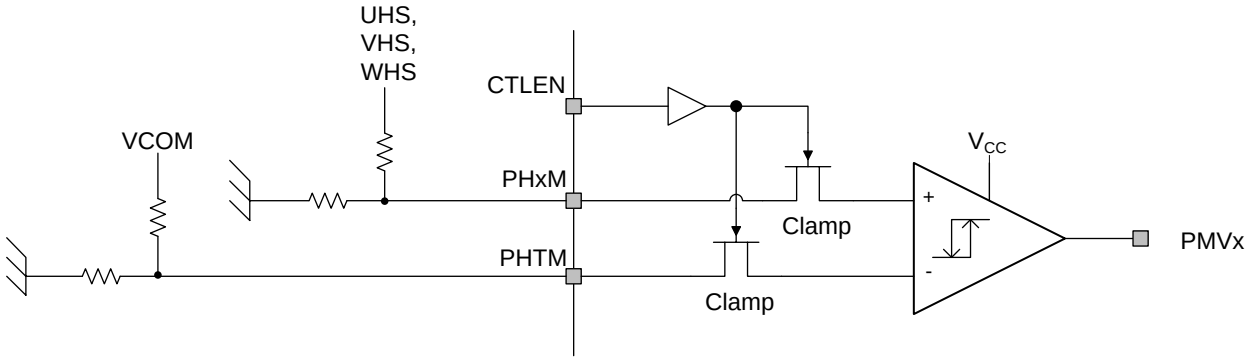


Figure 11. Phase Comparator Block Diagram

PHASE COMPARATORS ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

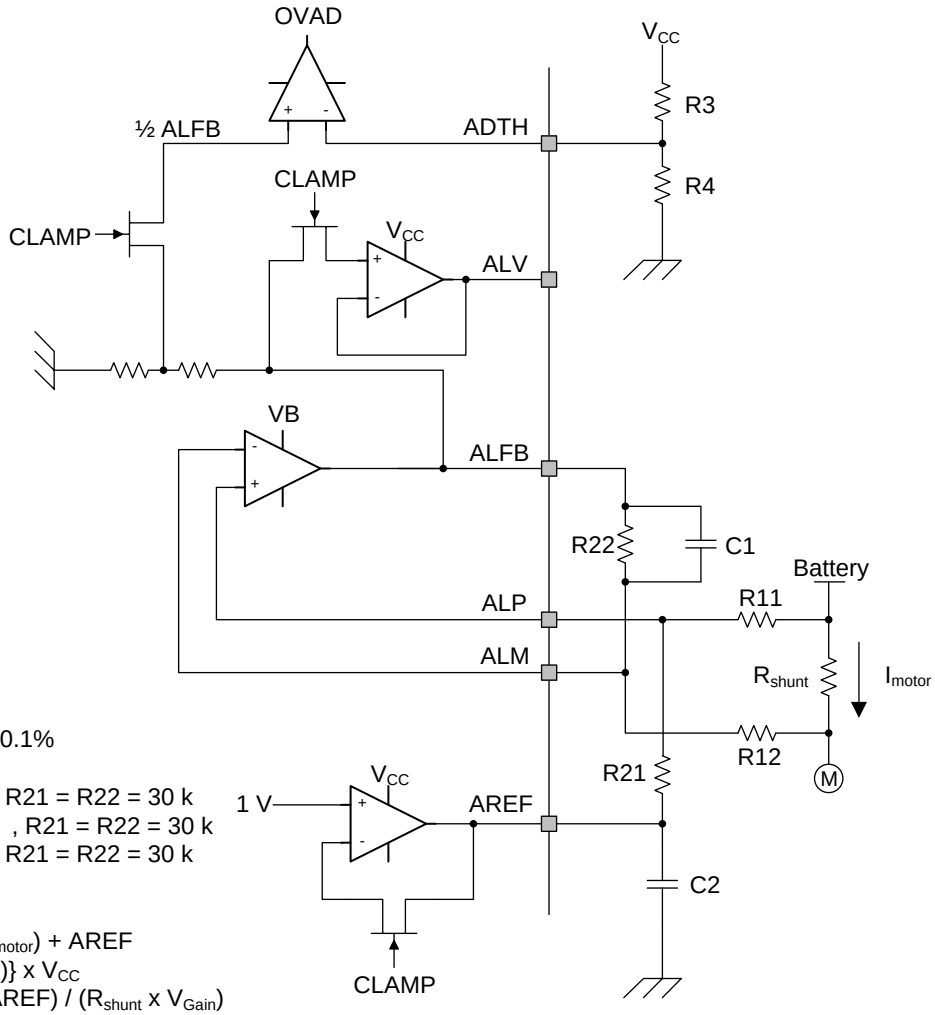
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
PHASE COMPARATOR						
V_{iofs}	Input offset voltage		–15	–	15	mV
V_{inp}	Input voltage range (PHTM)	VB = 5.3 ~18 V	1.325	–	4.5	V
V_{inm}	Input voltage range (PHxM)		–1	–	VB	V
V_{ihys}	Input hysteresis voltage		100	200	400	mV
V_{OH}	Output high voltage	I_{sink} = 2.5 mA	0.9 × V_{CC}	–	–	V
V_{OL}	Output low voltage	I_{source} = 2.5 mA	–	–	0.1 × V_{CC}	V
T_{res_tr} (1)	Response time (rising)	C_L = 100 pF	–	0.2	0.5	µs
T_{res_tf} (1)	Response time (falling)	C_L = 100 pF	–	0.4	1	µs

(1) Specified by design

MOTOR CURRENT SENSE

Description

The operational amplifier is operating with an external resistor network for higher flexibility to adjust the current measurement to application requirements. The first stage amplifier is operating with the external resistor and the output voltage up to VB at ALFB. The gain of the amplifier is adjustable by external resistors from x10 to x30. The second stage amplifier is a buffer to MCU at ALV. Current sense has a comparator for motor overcurrent (OVAD). ADTH is the overcurrent threshold level and sets the value by the external resistor as well. Figure 13 shows the curve of the detection level. ALFB is divided by 2, compare this value with ADTH. In the recommended application, zero-point adjustment is required as a large error offset in the initial condition.



*R11, R12, R21, R22 # 0.1%
*V_{Gain}
X10: R11 = R12 = 3 k , R21 = R22 = 30 k
X20: R11 = R12 = 1.5 k , R21 = R22 = 30 k
X30: R11 = R12 = 1 k , R21 = R22 = 30 k
C2 = 10 n ~ 20 nF
C1 = 0 ~ 10 pF
*ALV = V_{Gain} x (R_{shunt} x I_{motor}) + AREF
*ADTH = {R4 / (R3 + R4)} x V_{CC}
*OVAD = (2 x ADTH – AREF) / (R_{shunt} x V_{Gain})

Figure 12. Motor Current Sense Block Diagram

MOTOR CURRENT SENSE ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
MOTOR CURRENT(2) SENSE						
V_{Ofs}	Input offset voltage		–5		5	mV
V_{O_0}	Output voltage (ALV)	VB = 5.3 ~ 18 V, I_{motor} = 0 A		1		V

(1) No variation of the external components
(2) Motor current is converted to voltage in test

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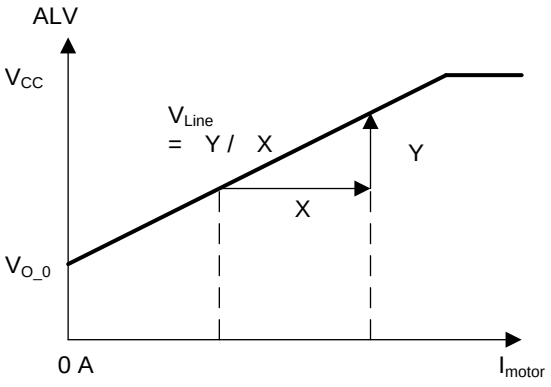

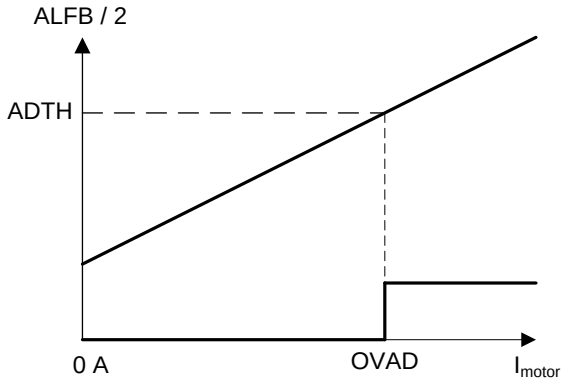

*ALFB up to VB

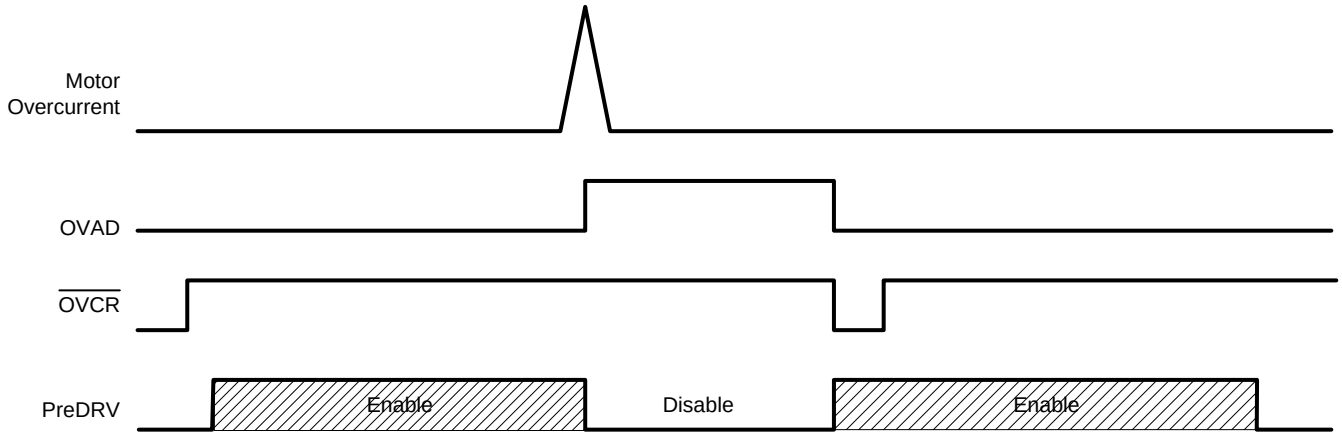

Figure 14. Motor Overcurrent Event

Table 3. Motor Overcurrent Truth Table

$\overline{RES}$	$\overline{OVCR}$	MOTOR OVERCURRENT	OVAD	PRE-DRIVER ENABLE OR DISABLE
0	–	–	0 (Clear)	Disable(1)
1	0	–	0 (Clear)(2)(3)	Enable
	1	0	Keep	Enable
		1	1 (Set)	Disable

(1) The CTLEN goes to Hi-Z because the external CPU will not drive it when $\overline{RES}$ = 0, then all the pre-drivers are turned off because CTLEN is internally pulled down.
(2) The OVAD is not set, even if a motor overcurrent error is generated during $\overline{OVCR}$ = 0.
(3) The OVAD is cleared if $\overline{OVCR}$ = 0 even when the motor overcurrent error is generated.

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PHASE AMPLIFIER (Sample and Hold Mode and Through Mode)

Description

The 3-channel amplifier module monitors the drain-source for high-side and low-side FETs. Two modes (selected by the SPI) are provided: sample and hold mode, and through mode. Sample and hold is controlled by PSSx at the external pins and PSCx connects the charging capacitor. Through mode is real-time detection and the amplifier has x1–x4 gain control.

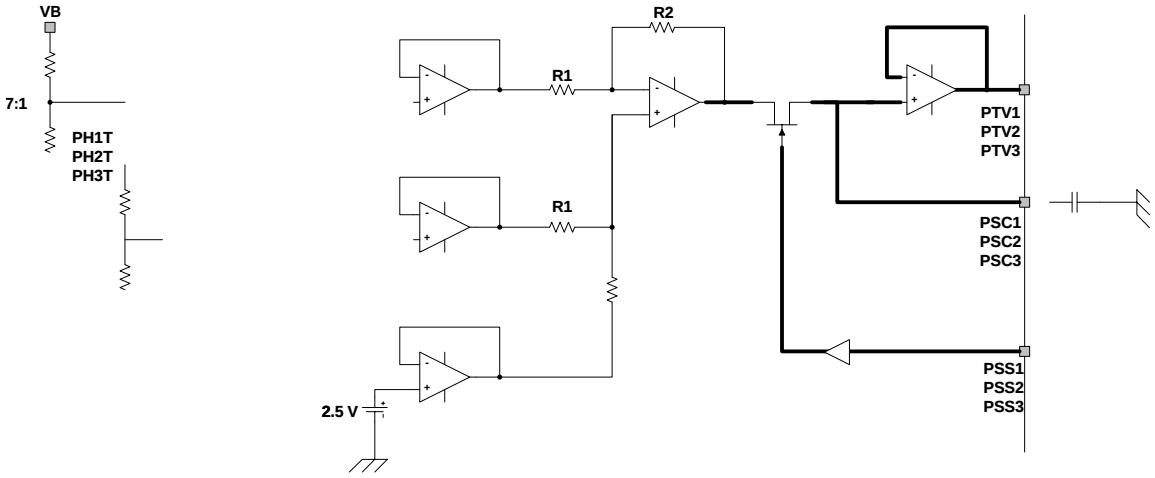


Figure 15. Sample and Hold Mode Block Diagram

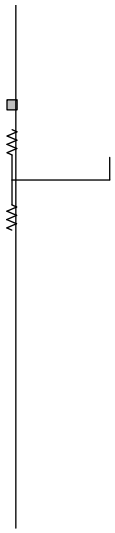


Figure 16. Through Mode Block Diagram

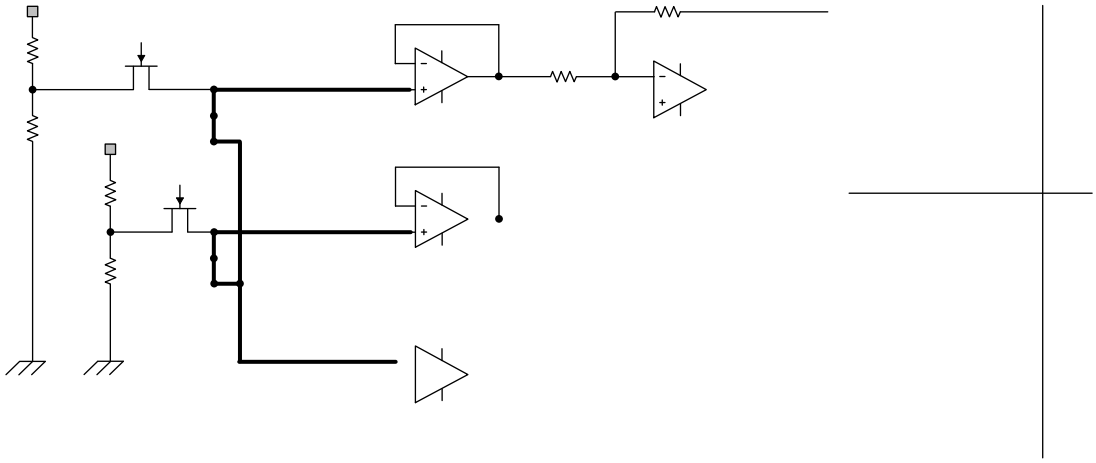


Figure 17. Short Mode (Optional) Block Diagram

PHASE AMPLIFIER ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
PHASE AMPLIFIER						
V_{ofs_SH}	Output offset voltage, sample and hold mode	VB = 5.3–18 V, Gain = 1	–50	–	50	mV
V_{ofs_TH}	Output offset voltage, through mode	VB = 5.3–18 V, Gain = 1	–50	–	50	mV
V_{in_cm}	Common mode input range	VB = 5.3–18 V, Gain = 1–4	1.5		VB – 1.5	V
V_{out_max}	Maximum output voltage	VB = 5.3–18 V, Gain = 1–4	4.5	–	–	V
V_{out_min}	Minimum output voltage	VB = 5.3–18 V, Gain = 1–4	–	–	0.5	V
V_{gain} (2)	Gain		–	1 2 3 4	–	
V_{out_SH0}	Output voltage, sample and hold mode	VB = 5.3–18 V, Gain = 1–4, PHxT = VB / 2	–	2.5	–	V
V_{out_TH0}	Output voltage, through mode	VB = 5.3–18 V, Gain = 1–4 PHxT = VB / 2	–	2.5	–	V
V_{out_SH1}	Output voltage, sample and hold mode	VB = 12 V, Gain = 1, PHxT = 1.5 V	–	1.375	–	V
V_{out_TH1}	Output voltage, through mode	VB = 12 V, Gain = 1, PHxT = 1.5 V	–	1.375	–	V
V_{out_SH2}	Output voltage, sample and hold mode	VB = 12 V, Gain = 1, PHxT = 10.5 V	–	3.625	–	V
V_{out_TH2}	Output voltage, through mode	VB = 12 V, Gain = 1, PHxT = 10.5 V	–	3.625	–	V
STL_SHTR	Settling time (rise), sample and hold mode PTVx ±1%	VB = 12 V, Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 1.5 V ≥ 10.5 V, (PTVx = 1.375 V → 3.625 V), see Figure 20		1.5	3	µs
STL_THTR	Settling time (rise), through mode PTVx ±1%	VB = 12 V, Gain = 1, PTVx = 100 pF, PHxT = 1.5 V ≥ 10.5 V, (PTVx = 1.375 V → 3.625 V), see Figure 21		1.5	3	µs
STL_SHTF	Settling time (fall), sample and hold mode PTVx ±1%	VB = 12 V, Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 10.5 V ≥ 1.5 V, (PTVx = 3.625 V → 1.375 V), see Figure 20		1.5	3	µs
STL_THTF	Settling time (fall), through mode PTVx ±1%	VB = 12 V, Gain = 1, PTVx = 100 pF, PHxT = 10.5 V ≥ 1.5V, (PTVx = 3.625 V → 1.375 V), see Figure 21		1.5	3	µs
SH Error Voltage	Falling voltage	VB = 5.3–18 V, PSC = 470 pF, TH = 1 mS, see Figure 19		5	75	mV

(1) No variation of the external components.
(2) V_{gain} is an SPI setting

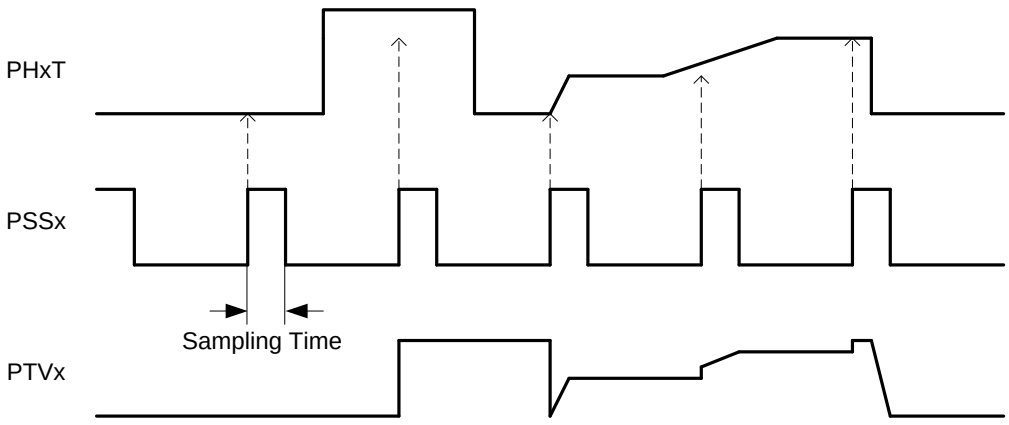


Figure 18. Sampling Timing Chart

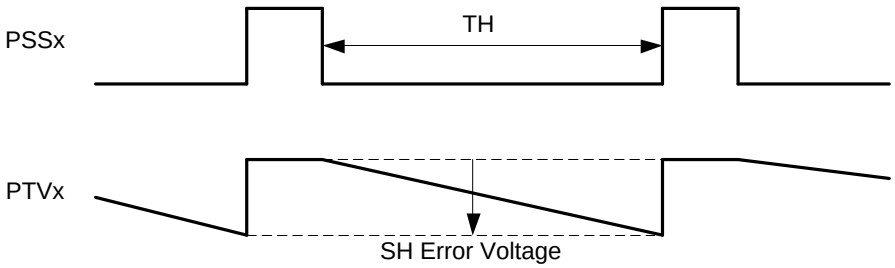


Figure 19. Holding Timing Chart

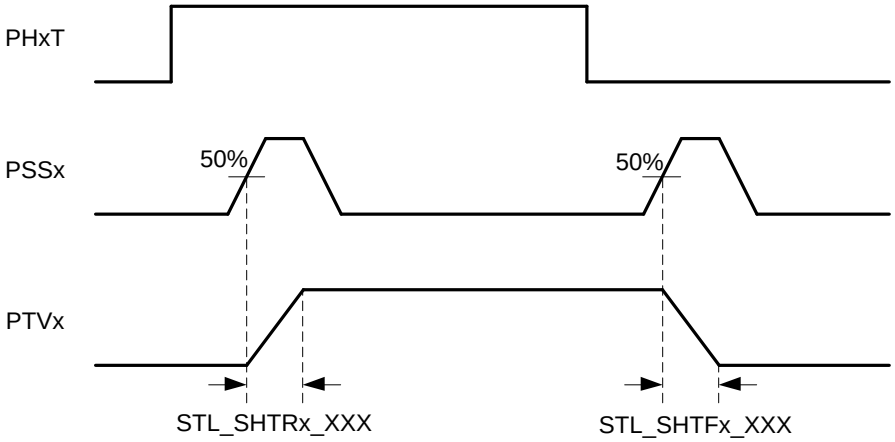


Figure 20. Settling Time Timing Chart (Sample and Hold Mode)

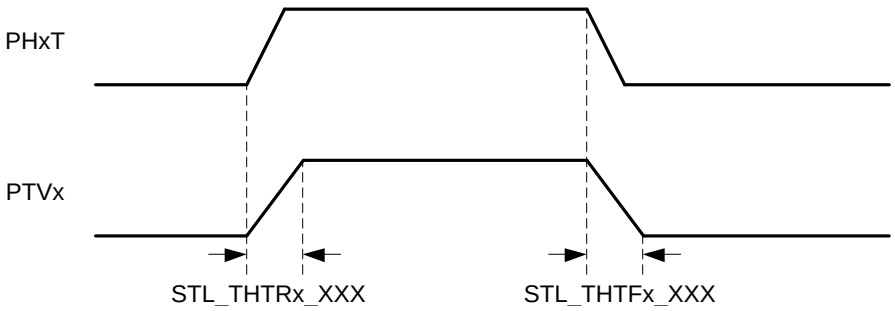


Figure 21. Settling Time Timing Chart (Through Mode)

PRODUCT PREVIEW

REGULATORS

Description

The regulator block offers a 5-V LDO and a 3.3-V LDO. The V_{CC} LDO regulates VB down to 5 V with an external PNP controlled by the regulator block. The 5-V LDO is supplied to the MCU and other components. The 5-V LDO is protected against a short to GND fault, and the external resistors R1 and R2 set the undervoltage. The V_{DD} regulator regulates VB down to 3.3-V with an internal FET and a controller.

The regulators detect the overvoltage and undervoltage events of both supplies.

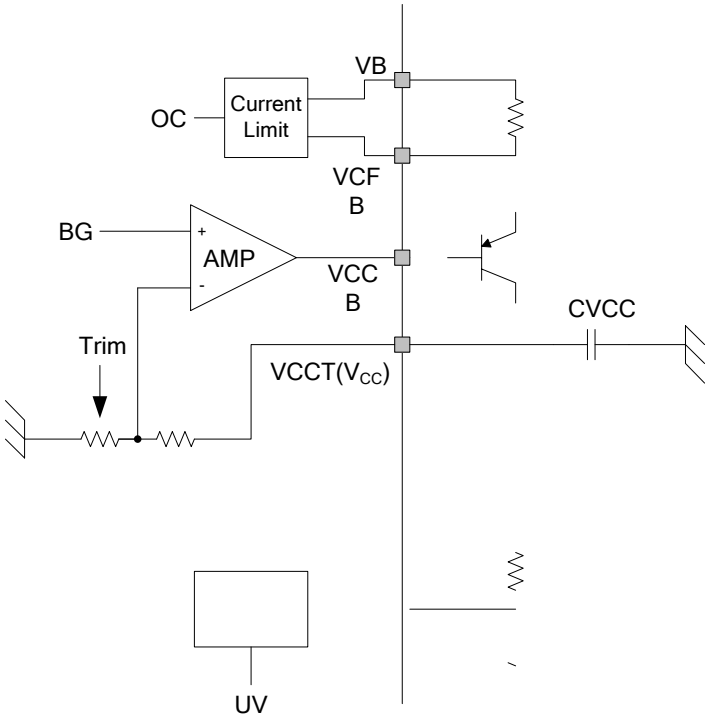


Figure 22. V_{CC} Block Diagram

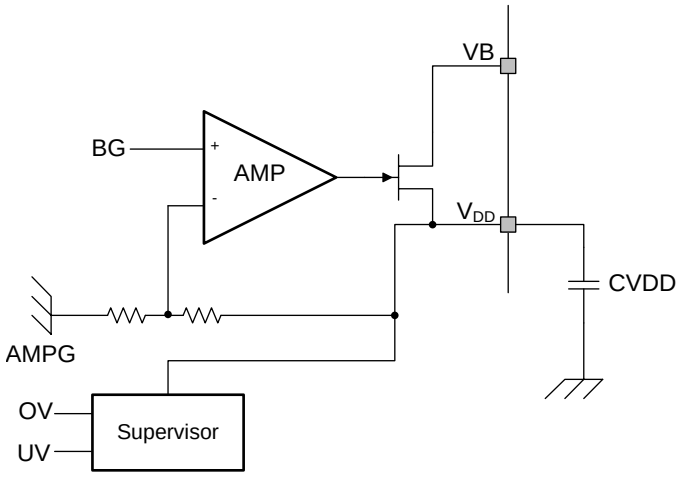


Figure 23. V_{DD} Block Diagram

V_{CC} AND V_{DD} ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}						
V_{CC}	Output voltage	VB = 5.3–18 V, I_{load} = 5–150 mA	4.9	5	5.1	V
IBVCC	Base current		1.5			mA
hfePNP	DC current gain of external VCC		100			
VLRVCC	Load regulation	VB = 5.3–18 V, I_{load} = 5–150 mA	–50	–	50	mV
CVCC	Load capacitance		22		100	µF
RVCC	ESR of external capacitance				300	mΩ
VCCUV	Undervoltage detection threshold	R1 = 7.5 kΩ, R2 = 10 kΩ, VCCUV > 4 V	3.97	4.07	4.17	V
VCCUVHYS	Undervoltage detection threshold hysteresis			100		mV
VCCOV	Overvoltage detection threshold		6	6.5	7	V
ICLVCC	Current limit	R_{sns} = 0.51 Ω	300	400	550	mA
TVCC1	Rise time	V_{CC} > UVVCC, CVCC = 22 µF		0.3	0.5	ms
TVCC2	Rise time	V_{CC} > UVVCC, CVCC = 100 µF		1	1.5	ms
V_{DD}						
V_{DD}	Output voltage	VB = 5.3–18 V, I_{load} = 0–2 mA	3	3.3	3.6	V
CVDD	Load capacitance			1		µF
VDDUV	Undervoltage detection threshold		2.2	2.3	2.4	V
VDDOV	Overvoltage detection threshold		4.1	4.3	4.5	V
T_{vdd}(2)	Rise time	V_{DD} > VDDUV, CVDD = 1 µF		75	150	µs

(1) No variation of the external components
(2) Specified by design

VB Monitor

Description

The block monitors VB overvoltage.

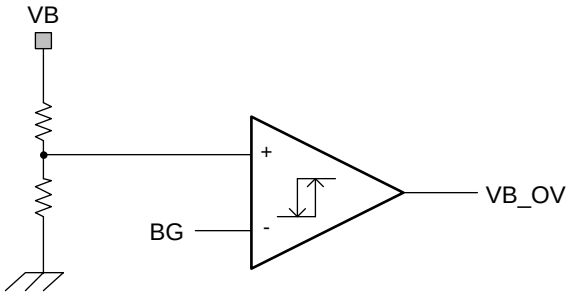


Figure 24. VB Monitor Block Diagram

VB MONITOR ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
VB MONITOR						
V_{stop}	Pre-driver stop VB voltage		26.5	27.5	28.5	V

PRODUCT PREVIEW

THERMAL SHUTDOWN

Description

The device has temperature sensors that produce a pre-driver stop condition if the chip temperature exceeds 175°.

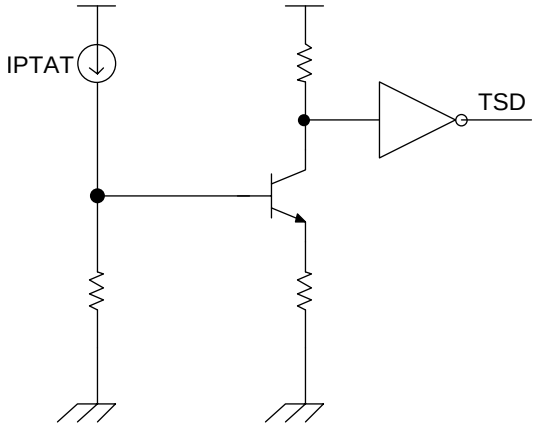


Figure 25. Thermal Shutdown Block Diagram

THERMAL SHUTDOWN ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUT DOWN					
TSD(1) Thermal shut down threshold		155	175	195	°C

(1) Specified by design

OSCILLATOR

Description

Oscillator block generates two 10-MHZ clock signals. OSC1 is the main clock used for internal logic synchronization and timing control. OSC2 is the secondary clock which is used to monitor the status of OSC1.

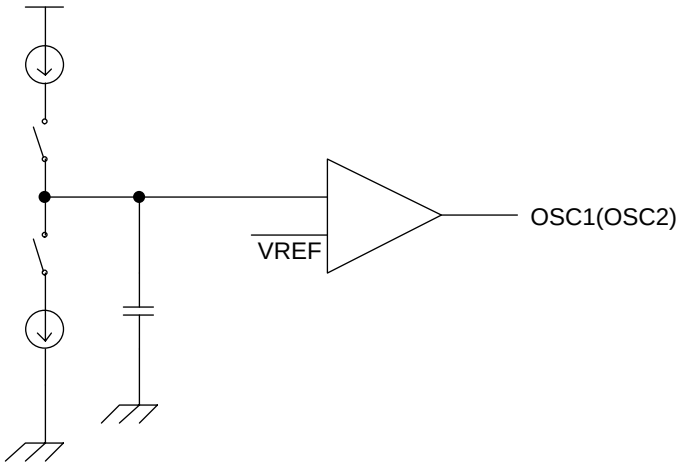


Figure 26. Oscillator Block Diagram

OSCILLATOR ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
OSC OSC frequency		9	10	11	MHz

I/O

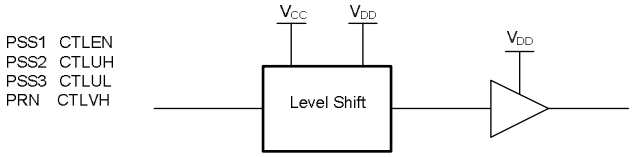


Figure 27. Input Buffer 1 Block Diagram

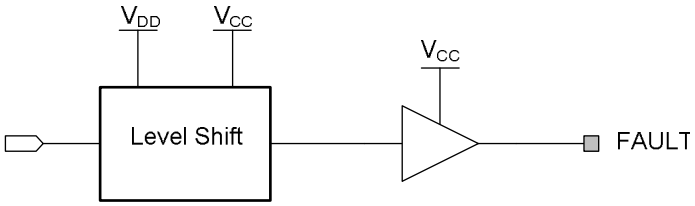


Figure 28. Output Buffer 1 Block Diagram

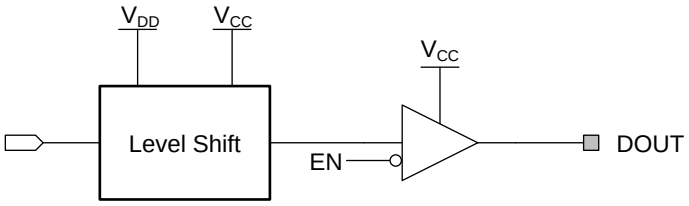


Figure 29. Output Buffer 2 Block Diagram

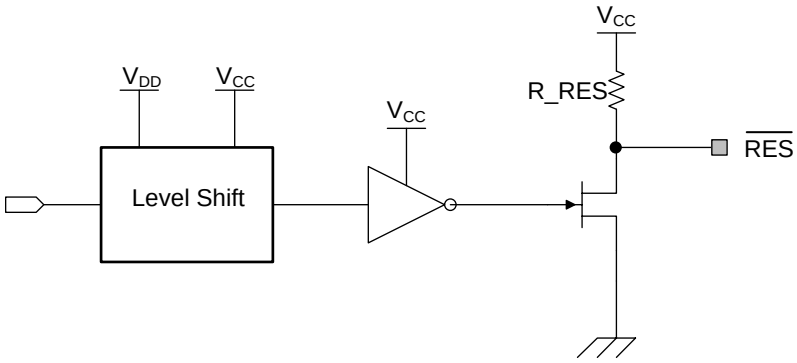


Figure 30. Output Buffer 3 Block Diagram

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

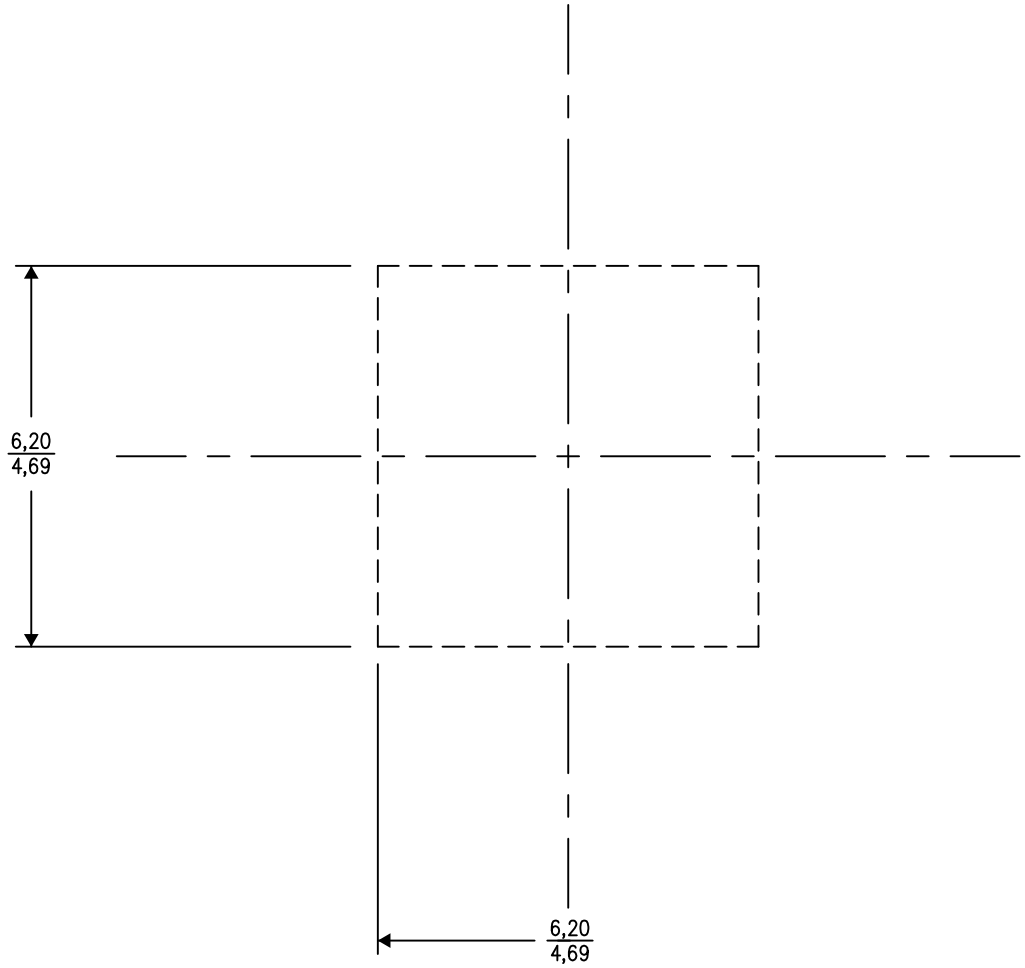
VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
INPUT BUFFER 1						
V_{IH}	Input threshold logic high		0.7 × V_{CC}			V
V_{IL}	Input threshold logic low				0.3 × V_{CC}	V
R_u	Input pullup resistance		50	100	150	kΩ
R_d	Input pulldown resistance		50	100	150	kΩ
OUTPUT BUFFER 1 AND 2						
V_{OH}	Output level logic high	I_{sink} = 2.5 mA	0.9 × V_{CC}			V
V_{OL}	Output level logic low	I_{source} = 2.5 mA			0.1 × V_{CC}	V
OUTPUT BUFFER 3						
R_RES	Pullup resistor		1.5	3	4.5	kΩ
V_{OL}	Output level logic low	I_{source} = 2 mA			0.1 × V_{CC}	V

ERROR DETECTION

Table 4. Error Detection

ITEMS	SPI	PRE-DRIVER	FAULT SIGNAL	$\overline{RES}$
VB – Overvoltage	–	STOP	L	H
CP – Overvoltage	–	STOP	L	H
CP – Undervoltage	Error Bit (CPLV)	–	L	H
V_{CC} – Overvoltage	Error Bit (VCO)	–	L	H
V_{CC} – Undervoltage	–	STOP	L	L
V_{CC} – Overcurrent	Error Bit (V_{CC})	–	H	H
Motor – Overcurrent	Error Bit (OVAD)	STOP	H	H
V_{DD} – Overvoltage	Error Bit (VDO)	–	L	H
V_{DD} – Undervoltage	–	STOP	L	L
Thermal Shut Down	Error Bit (TD)	STOP	H	H
Watchdog	–	–	L	L
EEPROM Data Check	Error Bit (EEP)	–	L	H
Clock Monitor	–	–	L	L
SPI	Error Bit (SPI)	–	L	H


6,20
4,69
6,20
4,69

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