Voltage Protection for 3-Series to 6-Series Cell Lithium-Ion/Polymer Batteries

Check for Samples: bq77PL157A4225

FEATURES

- **Single IC Li-Ion Protection for 3-Series to 6-Series Cells**
- **Stackable to Protect up to 18-Series Cells**
- **Programmable Detection Time Delay**
- **Low Power Consumption**
  - **Typical 2-µA to 2.5-µA Normal Mode**
- **Fixed 4.225 V Overvoltage Threshold**
- **Highly Accurate: ±20-mV MAX, T_A = 0°C to 50°C**
- **Output Activation for Low Side FET (Contact TI for Alternate Output Options: High/Low-side Fuse or FET)**
- **Protected Output, Power, and Ground Pins for Added Safety and Reliability**
- **Permanent or Recoverable Fault Options**
- **16-pin Small Outline Package**

APPLICATIONS

- **Primary or Secondary Level Voltage Protection for Li-Ion Battery Packs for Use in:**
  - **Power Tools**
  - **UPS Systems**
  - **E-Bikes, Scooters, and Small Mobility Vehicles**
  - **Medical Devices, Test Equipment, and Industrial Products**

DESCRIPTION

The bq77PL157 is a stackable overvoltage protection device for 3, 4, 5 or 6 series cell Li-Ion battery packs. This device incorporates a precise and accurate overvoltage detection circuit with preconfigured threshold limits. Additional features include the ability to stack multiple parts to monitor up to 18 series cells.

FUNCTION

Each series cell in a Li-Ion battery pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq77PL157 starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes state and the LVO pin becomes active.

If multiple bq77PL157 devices are stacked, the LVIN pin of the next-lower device receives the LVO pin from the above device and similarly starts a shortened delay timer before activating its OUT pin. (No additional isolation or level-shift circuitry is required.) The lowest bq77PL157 in the string is used to activate a power MOSFET located in the low side of the power path.

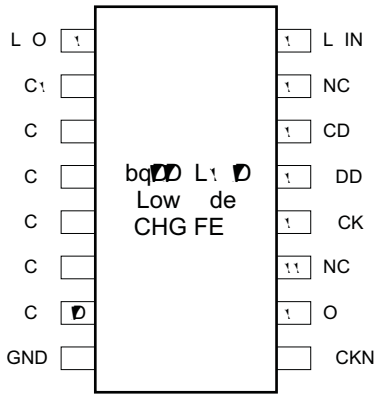
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

$V_{PROTECT}$	DEVICE	FEATURE CONFIGURATION	PACKAGING	FULL PART NAME
4.225 V	bq77PL157A	Recoverable Output	Tape and Reel	bq77PL157APWR-4225
			Tube	bq77PL157APW-4225

DEVICE INFORMATION

PW PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
CD	14	External capacitor to GND to set delay time
GND	8	Ground pin and negative end of cell stack
LVIN	16	Level-shift input (used for stacking, input is from next-higher part)
LVO	1	Level-shift output (used for stacking, route this output to next-lower part)
NC	11, 15	No connection
OUT	10	Output gate drive to external MOSFET
PCKN	9	Pack negative supply for OUT driver (connect to source of external MOSFET or GND if device not at bottom of stack)
PCKP	12	Pack positive supply for OUT driver (connect to most positive cell input of device)
VC1	2	Sense voltage input for most positive cell
VC2	3	Sense voltage input for second most positive cell
VC3	4	Sense voltage input for third most positive cell
VC4	5	Sense voltage input for fourth most positive cell
VC5	6	Sense voltage input for fifth most positive cell
VC6	7	Sense voltage input for least positive cell
VDD	13	Power supply (via RC filter)

FUNCTIONAL BLOCK DIAGRAMS

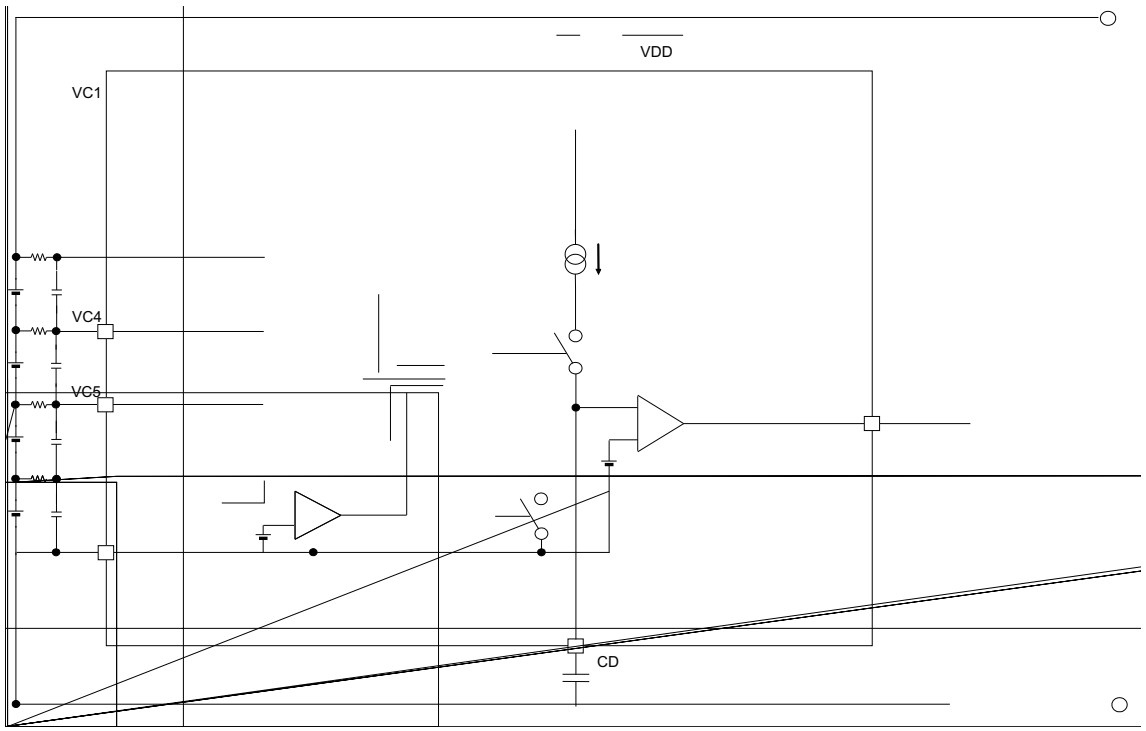


Figure 1. bq77PL157 – Low-Side Power NMOS Direct-Drive Output

ABSOLUTE MAXIMUM RATINGS

over recommended operating free-air temperature range, (unless otherwise noted)[1]

		RANGE
Supply voltage range, V_{MAX}	VDD, PCKP	–0.3 to 35 V

–0.3 to 35 V

range,V

–0.3 to 35 V

–0.3 to 35 V

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VDD	4.2		30	V
Pack positive voltage	PCKP	0		30	V
Pack negative voltage	PCKN	VDD – 30		n0 Td (voted))T=0 Td7.0ONDITI	

Figure 2. CD charge Current and Discharge Current

bq77PL157 OUTPUT

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OUT} OUT pin drive voltage	VCn – VC(n + 1), (n =1 to 5), VC6 – GND = $V_{PROTECT}$ + 25 mV, VDD = VC1, I_{OUT} = 0 to –0.1 mA, T_A = –40°C to 110°C			PCKN + 0.2	V
	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ – 25 mV, VDD = VC1, I_{OUT} = 0 to 0.1 mA, T_A = –40°C to 110°C	PCKN + 9	PCKN + 14	PCKN + 16	
V_{OUT} rise time	C_L = 5000 pF, V_{OUT}: 10% to 90%			100	µs
V_{OUT} fall time	C_L = 5000 pF, V_{OUT}: 90% to 10%			100	µs

LEVEL SHIFT FUNCTION

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_{LVL}	LVIN pull	VCn – VC(n + 1), (n = 1 to 5), VC6 –GND =					

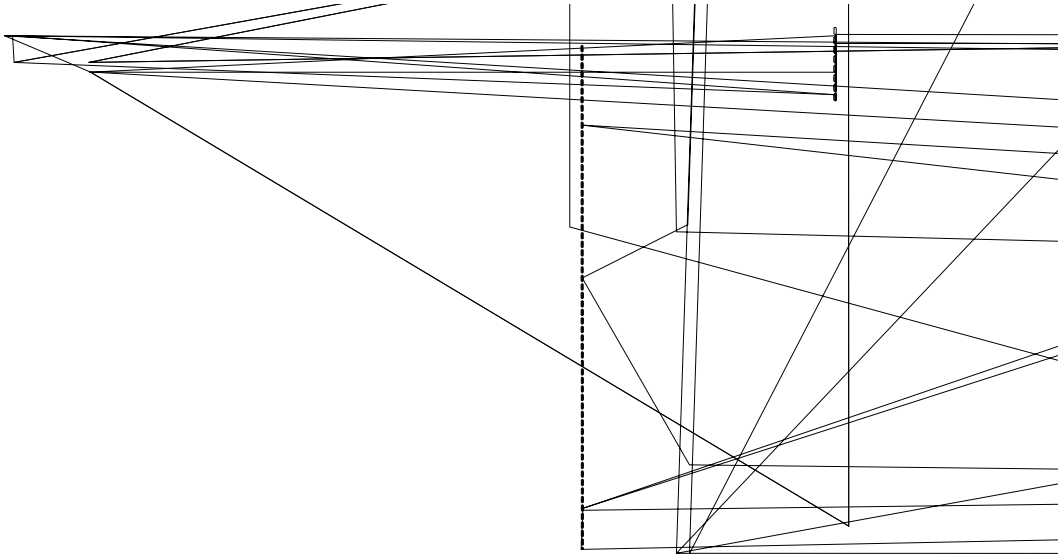


Figure 3. CD Charge Current and Discharge Current

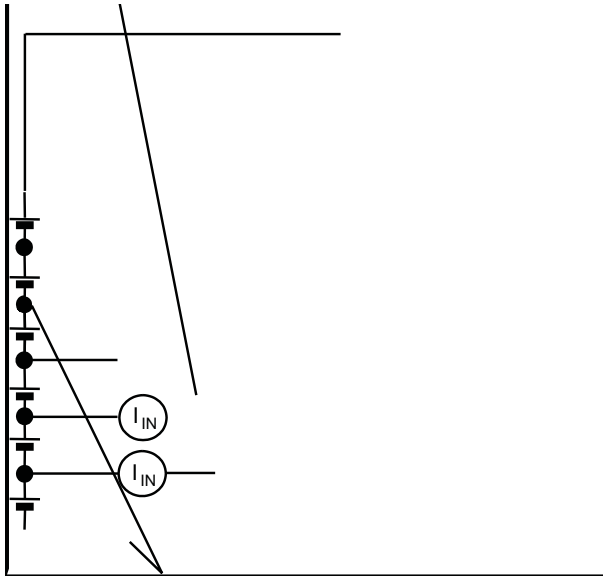


Figure 4. I_{CC}, I_{IN} Measurement Test Setup

OPERATION AND TIMING OF PROTECTION OUTPUT

From Direct Cell Inputs

When any one of the cell voltages exceeds $V_{PROTECT}$, an internal current source begins to charge capacitor C_{CD} connected to the CD pin, which acts as a delay timer. If all cell voltages fall below $V_{PROTECT}$ before V_{CD} reaches $V_{CD,TH1}$, the delay timer is reset and the OUT pin is not activated (i.e., no fault detected, output remains unchanged). An internal switch clamps the CD pin to GND, discharges the capacitor C_{CD}, and resets the full delay time for the next occurring overvoltage event.

If any cell voltage exceeds $V_{PROTECT}$ long enough for the voltage at the CD pin (V_{CD}) to reach $V_{CD,TH1}$ (1.2 V typical), then the OUT and LVO pins are activated (i.e., fault detected, output changes state), thus interrupting the circuit via the FET protection device. Once the output is activated, the CD pin is charged up to its maximum value $V_{CD,TH2}$ (2.4 V typical).

When the recovery option is selected, if all cell voltages fall below $V_{PROTECT} - V_{TH}$ (threshold hysteresis), an internal current source begins to discharge capacitor C_{CD}, also acting as a delay timer. If any cell voltage returns back above $V_{PROTECT} - V_{TH}$ before V_{CD} reaches $V_{CD,TH1}$, the delay timer is reset and the OUT and LVO pins remains active (i.e. in the fault state). The CD pin is charged back to its maximum value $V_{CD,TH2}$.

If all cell voltages remain below $V_{PROTECT} - V_{TH}$ long enough for the voltage at the CD pin to reach $V_{CD,TH1}$, then the OUT and LVO pins are deactivated (i.e. output returns to the no fault state). An internal switch clamps the CD pin to GND, discharges the capacitor C_{CD}, and resets the full delay time for the next occurring overvoltage event.

The delay time for detecting an overvoltage fault is the time between charging C_{CD} from 0 to $V_{CD,TH1}$ and can be calculated as follows:

$t_D = (V_{CD,TH1} \times C_{CD}) / I_{CH1}$
$C_{CD} = (t_D \times I_{CH1}) / V_{CD,TH1}$
where I_{CH1} = CD charge current = 0.2 µA (typical)

The recovery delay time is the time between discharging from $V_{CD,TH2}$ to $V_{CD,TH1}$. The minimum output active time (t_{OA}) can be calculated as follows:

$t_{OA} = (V_{CD,TH2} - V_{CD,TH1}) \times C_{CD}) / I_{DS1}$
$C_{CD} = (t_{OA} \times I_{DS1}) / (V_{CD,TH2} - V_{CD,TH1})$
where I_{DS1} = CD discharge current = 0.2 µA (typical)

Figure 5. Timing for Overvoltage Sensing (With Recovery Option)

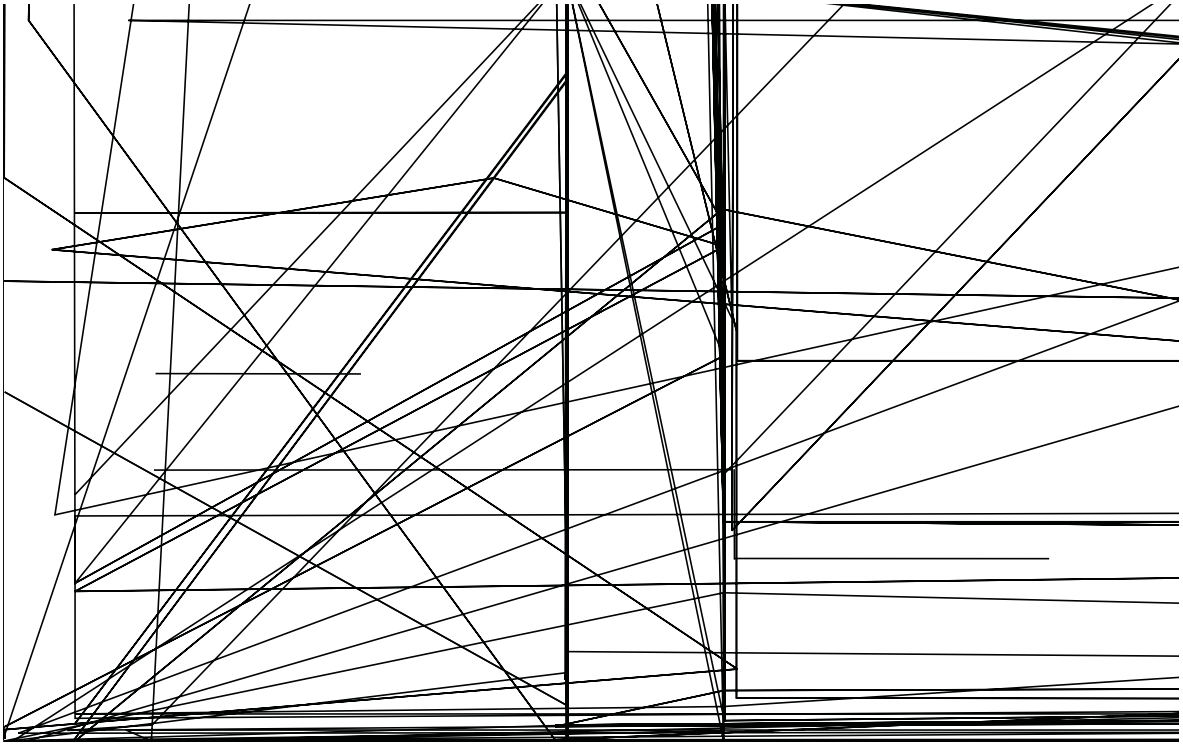


Figure 6. Timing for Overvoltage Sensing (Without Recovery Option – Permanent Latch)

From Level Shift Input

More than six cells can be monitored with multiple bq77PL157 devices by using the LVO and LVIN pins to cascade or stack multiple parts. The LVO pin from the *upper* bq77PL157 is connected to the LVIN pin of the *lower* bq77PL157. The OUT pin of the *lowest* bq77PL157 is used to control the activation element while the OUT pins of the upper bq77PL157 devices are not used.

When the LVIN pin changes from a low to high level, an internal current source begins to charge capacitor C_{CD}, connected to the CD pin, quickly. If the voltage at the CD pin, V_{CD}, reaches $V_{CD,TH1}$ (1.2 V typical), then the OUT pin and the LVO pin are both activated. Once the output is activated, the CD pin continues to charge up to its maximum value of $V_{CD,TH2}$ (2.4 V typical).

The delay time from LVIN to either LVO or OUT is minimized by quickly charging the CD pin and is approximately 10 times faster than the delay time from an overvoltage fault at the direct cell inputs. When more than two bq77PL157 devices are stacked, this delay time is additive.

The delay time per device can be calculated as follows:

$t_{DA} = (V_{CD,TH1} \times C_{CD}) / I_{CHLV}$
where IC_{HLV} = CD charge current = $10 \times I_{CH1}$ = 2 µA (typical)

When the LVIN pin changes from a high to low level, an internal switch clamps the CD pin to GND, discharging the capacitor C_{CD}. The delay time (per part) can be calculated as follows.

$t_{DIA} = (V_{CD,TH2} – V_{CD,TH1}) \times C_{CD} / I_{DSLV}$
where I_{DSLV} = CD discharge current = 90 µA (typical)

To find the total expected delay time from LVIN to OUT, a variable internal latency of approximately 4 - 12 ms should be added.

Faults detected via LVIN have the highest priority and will interrupt the timing of all lower priority faults.

Figure 7. LVIN to OUT and LVO Timing

CELL CONNECTION SEQUENCE

Unused VCx cell input pins should be connected to the most positive connected cell input pin as shown in the *Battery Connection Diagrams* section. VDD

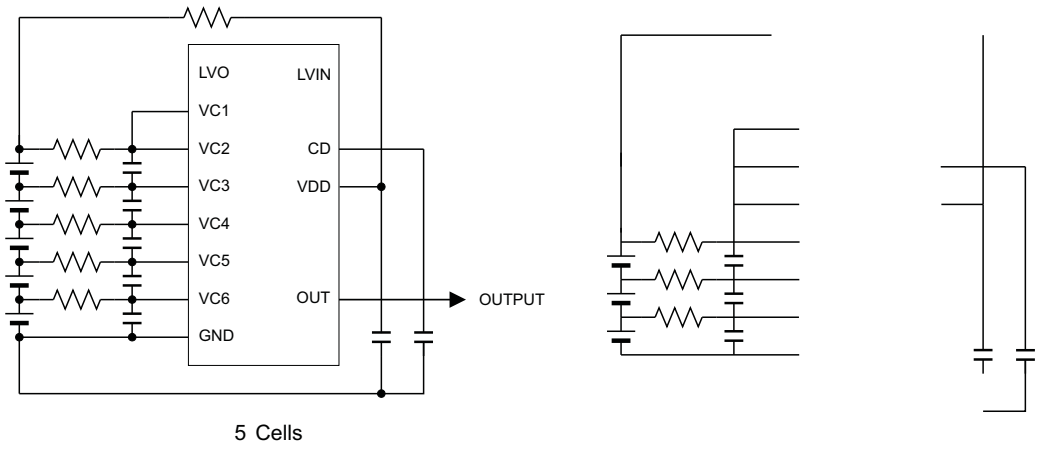
BATTERY CONNECTION DIAGRAMS

The following schematics indicate the cell connections for several battery configurations. Unused cell inputs should be connected together on the most positive end of the cell stack. **(VC1 is the most positive input.)**

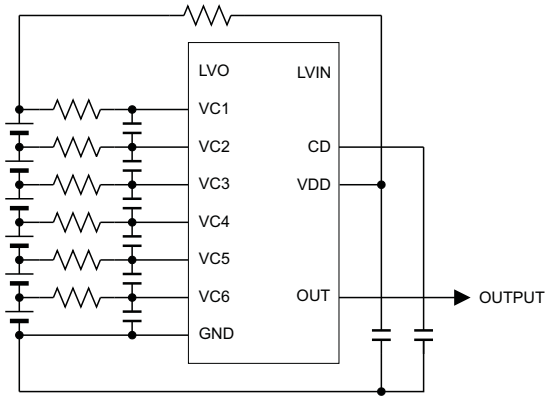
The PCKP and PCKN pins supply power to the output FET driver. PCKP is always connected to the most positive cell input of the device. PCKN for a single device or the bottom device in a stack is connected to the source terminal of the protection FET device. For an upper device in a stacked configuration, PCKN is connected to GND.

NOTE

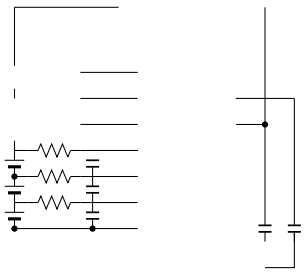
Not all connections shown. Diagrams are simplifications of full circuits and do not include key constraints when stacking these parts.



5 Cells



6 Cells



REDUCING TEST TIME

By controlling the CD pin, it is possible to reduce the time for functional test at PC board assembly:

To make a shorter overvoltage delay time, pull the CD pin over 1.2 V (typ) (MAX to VDD).

To recover from an overvoltage condition, pull the CD pin down to GND and set cell VCx < $V_{PROTECT} - V_{TH}$.

REVISION HISTORY

Changes from Original (March 2010) to Revision A **Page**

- Changed the overvoltage detection hysteresis (V_{TH}) minimum value of 100 mV to 150 mV 4

Changes from Revision A (October 2011) to Revision B **Page**

- Changed Features Item From: Fixed Overvoltage Thresholds Available From 3.75 V to 4.35 V in 25-mV Steps To: Fixed 4.225 V Overvoltage Threshold 1
- Changed the DESCRIPTION paragraph 1
- Changed the ORDERING INFORMATION section 2
- Deleted Test Conditions for $V_{PROTECT}$. Deleted the MIN and MAX values. Added a TYP value of 4.225 V 4

PACKAGING INFORMATION

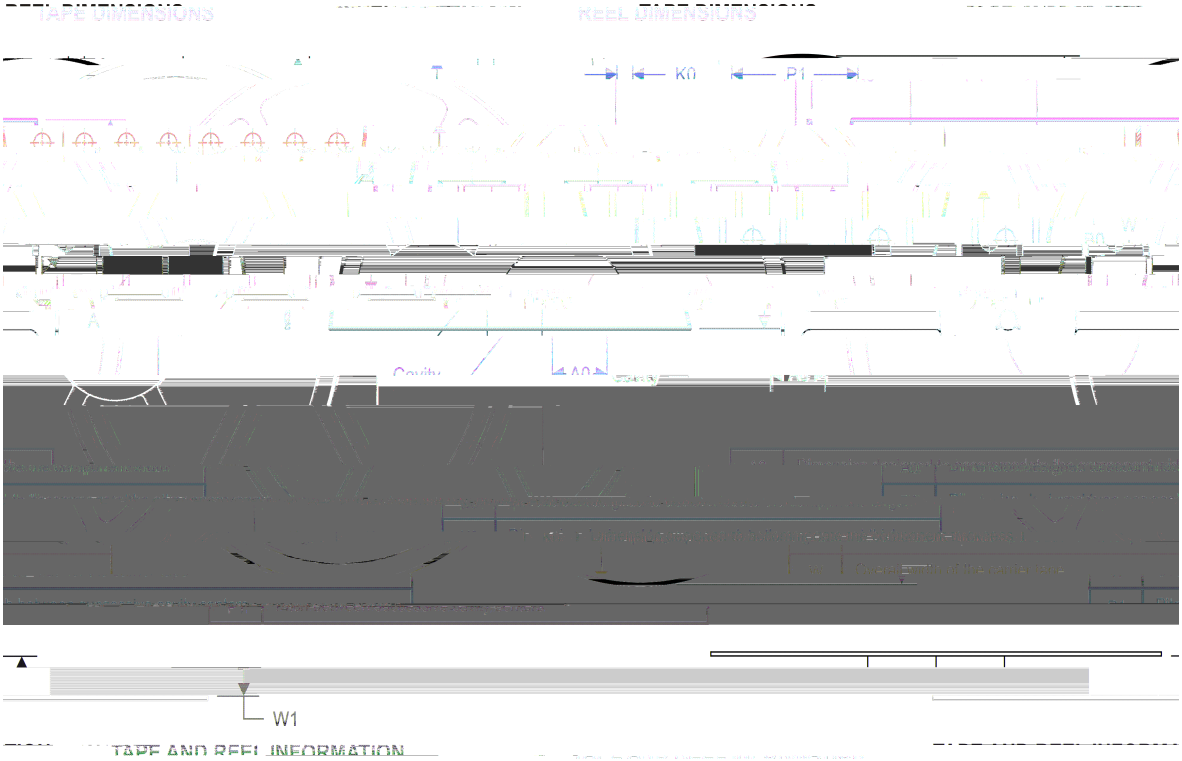
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ77PL157APW-4225	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ77PL157APWR-4225	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

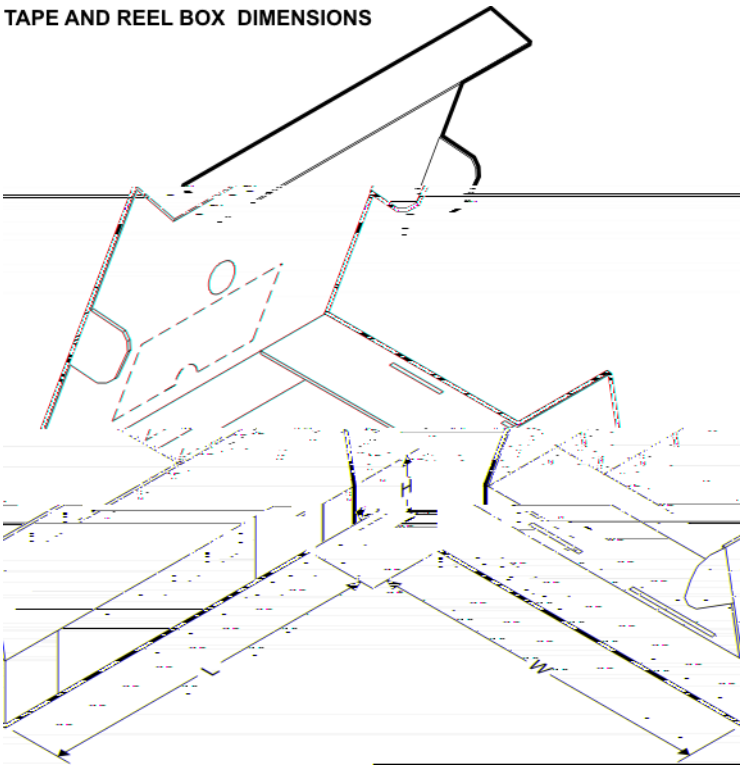
TAPE AND REEL INFORMATION



*All dimensions are nominal

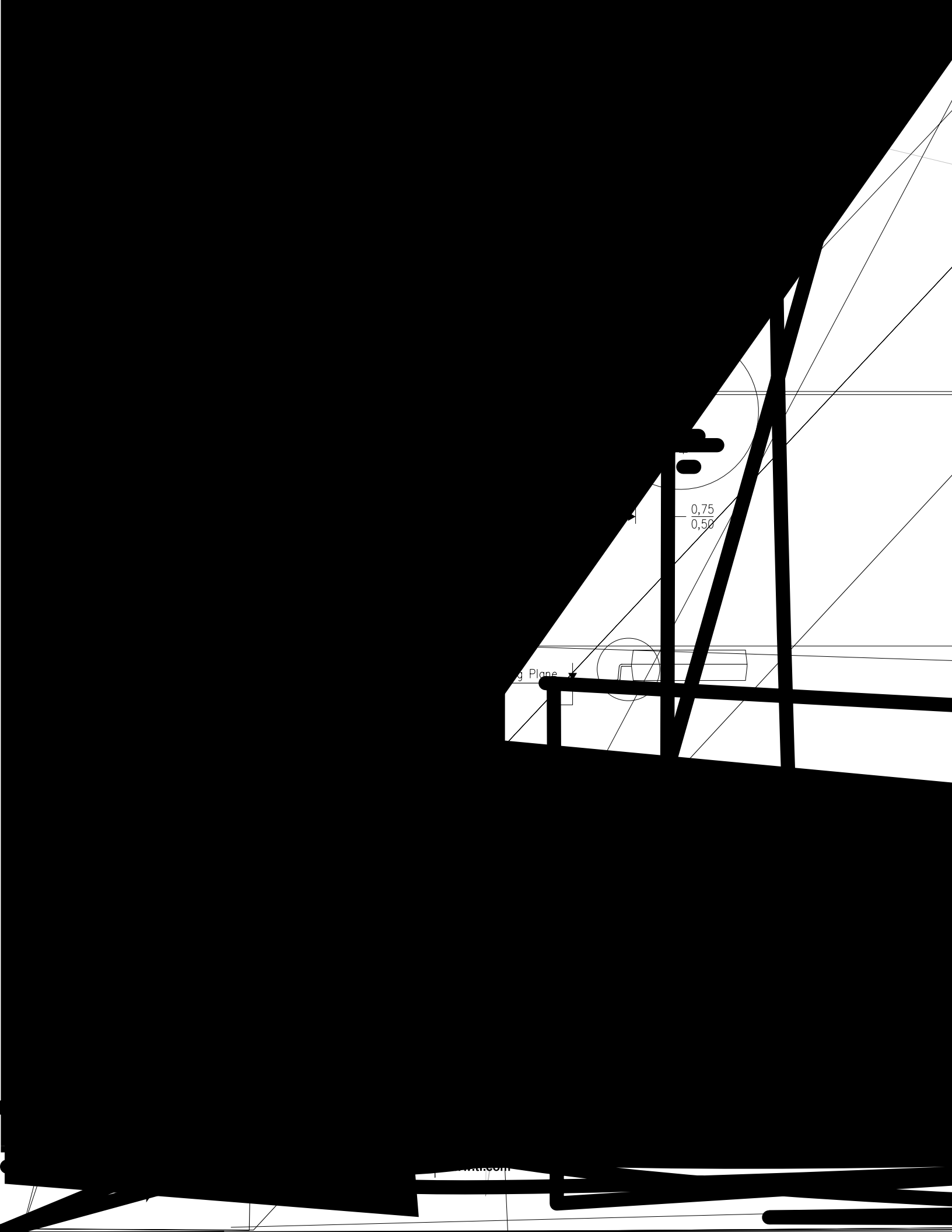
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ77PL157APWR-4225	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ77PL157APWR-4225	TSSOP	PW	16	2000	367.0	367.0	35.0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0,50