SBS 1.1-Compliant Gas Gauge and Protection Enabled With Impedance Track Œ and External Battery Heater Control

Check for Samples: bq34z651

FEATURES

- **Next Generation Patented Impedance Track Œ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries**
  - **Better Than 1% Error Over the Lifetime of the Battery**
- **Supports the Smart Battery Specification SBS v1.1**
- **Flexible Configuration for 2-Series to 4-Series Li-Ion and Li-Polymer Cells**
- **Battery Temperature Heater Control**
- **Powerful 8-Bit RISC CPU with Ultralow Power Modes**
- **Full Array of Programmable Protection Features**
  - **Voltage, Current, and Temperature**
- **Satisfies JEITA Guidelines**
- **Added Flexibility to Handle More Complex Charging Profiles**
- **Lifetime Data Logging**
- **Drives 3-, 4-, and 5-Segment LED Display for Battery-Pack Conditions**
- **Supports SHA-1 Authentication**
- **Complete Battery Protection and Gas Gauge Solution in One Package**
- **Available in a 44-Pin TSSOP (DBT) package**

APPLICATIONS

- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq34z651 SBS-compliant gas gauge and protection IC, incorporating patented Impedance Track Œ technology, is a single IC solution designed for battery-pack or in-system installation. The bq34z651 measures and maintains an accurate record of available charge in Li-Ion or Li-Polymer batteries using its integrated high-performance analog peripherals. The bq34z651 monitors capacity change, battery impedance, open-circuit voltage, and other critical parameters of the battery pack, which reports the information to the system host controller over a serial-communication bus. Together with the integrated analog front-end (AFE) short-circuit and overload protection, the bq34z651 maximizes functionality and safety while minimizing external component count, cost, and size in smart battery circuits.

The implemented Impedance Track gas gauging technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables remaining capacity to be calculated with discharge rate, temperature, and cell aging ² all accounted for during each stage of every cycle with high accuracy.

Table 1. AVAILABLE OPTIONS

T_A	PACKAGE(1)	
	44-PIN TSSOP (DBT) Tube	44-PIN TSSOP (DBT) Tape and Reel
±40 ƒC to 85 ƒC	bq34z651DBT(2)	bq34z651DBTR(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) A single tube quantity is 40 units.
(3) A single reel quantity is 2000 units.

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Impedance Track is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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THERMAL INFORMATION

THERMAL METRIC(1)		bq34z651 TSSOP 44 PINS	UNITS
$\theta_{JA, High K}$	Junction-to-ambient thermal resistance(2)	60.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	15.3	
θ_{JB}	Junction-to-board thermal resistance (4)	30.2	
Ψ_{JT}	Junction-to-top characterization parameter (5)	0.3	
Ψ_{JB}	Junction-to-board characterization parameter (6)	27.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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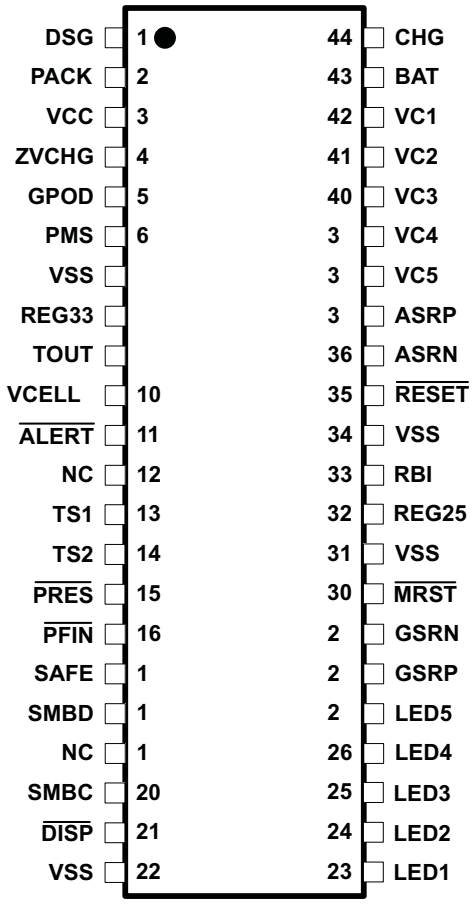
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SYSTEM PARTITIONING DIAGRAM

PACKAGE PINOUT DIAGRAM

DBT PACKAGE
(TOP VIEW)



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TERMINAL FUNCTIONS

TERMINAL		I/O(1)	DESCRIPTION
NO.	NAME		
1	DSG	O	High-side N-channel discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wake up when device is in shutdown mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input.
4	ZVCHG	O	P-channel pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. It can be configured to be used in pre-charge condition.
6	PMS	I	Pre-charge mode setting input. Connect to PACK to enable 0v pre-charge using charge FET connected at CHG pin. Connect to VSS to disable 0-V pre-charge using charge FET connected at CHG pin.
7	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
8	REG33	P	3.3-V regulator output. Connect at least a 2.2- F capacitor to REG33 and VSS.
9	TOUT	P	Thermistor bias supply output
10	VCELL+	²	Internal cell voltage multiplexer and amplifier output. Connect a 0.1- F capacitor to VCELL+ and VSS.
11	$\overline{\text{ALERT}}$	I/OD	Alert output. In case of short circuit condition, overload condition and watchdog timeout, this pin will be triggered.
12	NC	²	Not used ² leave floating.
13	TS1	IA	1st thermistor voltage input connection to monitor temperature
14	TS2	IA	2nd thermistor voltage input connection to monitor temperature
15	$\overline{\text{PRES}}$	I	Active low input to sense system insertion. Typically requires additional ESD protection.
16	$\overline{\text{PFIN}}$	I	Active low input to detect secondary protector status, and to allow the bq34z651 to report the status of the 2nd-level protection input
17	SAFE	O	Active high output to enforce additional level of safety protection; e.g., fuse blow
18	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq34z651
19	NC	²	Not used ² leave floating.
20	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq34z651
21	$\overline{\text{DISP}}$	I/OD	Display control for the LEDs. This pin is typically connected to VCC via a 100-k Ÿ resistor and a push button switch connected to VSS.
22	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
23	LED1	I	LED1 display segment that drives an external LED depending on the firmware configuration
24	LED2	I	LED2 display segment that drives an external LED depending on the firmware configuration
25	LED3	I	LED3 display segment that drives an external LED depending on the firmware configuration
26	LED4	I	LED4 display segment that drives an external LED depending on the firmware configuration
27	LED5	I	LED5 display segment that drives an external LED depending on the firmware configuration
28	GSRP	IA	Coulomb counter differential input. Connect to one side of the sense resistor.
29	GSRN	IA	Coulomb counter differential input. Connect to one side of the sense resistor.
30	$\overline{\text{MRST}}$	I	Master reset input that forces the device into reset when held low. Must be held high for normal operation. Connect to $\overline{\text{RESET}}$ for correct operation of device.
31	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
32	REG25	P	2.5-V regulator output. Connect at least a 1-mF capacitor to REG25 and VSS.
33	RBI	P	RAM/Register backup input. Connect a capacitor to this pin and VSS to protect loss of RAM/Register data in case of short circuit condition.
34	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
35	$\overline{\text{RESET}}$	O	Reset output. Connect to $\overline{\text{MSRT}}$.
36	ASRN	IA	Short circuit and overload detection differential input. Connect to sense resistor.
37	ASRP	IA	Short circuit and overload detection differential input. Connect to sense resistor.

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O(1)	DESCRIPTION
NO.	NAME		
38	VC5	IA, P	Cell voltage sense input and cell balancing input for the negative voltage of the bottom cell in cell stack.
39	VC4	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the bottom cell and the negative voltage of the second lowest cell in cell stack.
40	VC3	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second lowest cell in cell stack and the negative voltage of the second highest cell in 4-series cell applications.
41	VC2	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second highest cell and the negative voltage of the highest cell in 4-series cell applications. Connect to VC3 in 2-series

RECOMMENDED OPERATING CONDITIONS (continued)

Over operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage Range	VC(n) ±VC(n+1); n = 1,2,3,4	0		5	V
		VC1, VC2, VC3, VC4	0		V_{SUP}	V
		VC5	0		0.5	V
		ASRN, ASRP	±0.5		0.5	V
		PACK, PMS	0		25	V
$V_{(GPOD)}$	Output Voltage Range	GPOD	0		25	V
$A_{(GPOD)}$	Drain Current(1)	GPOD			1	mA
$C_{(REG25)}$	2.5-V LDO Capacitor	REG25	1			±F
$C_{(REG33)}$	3.3-V LDO Capacitor	REG33	2.2			±F
$C_{(VCELL+)}$	Cell Voltage Output Capacitor	VCELL+	0.1			±F
$C_{(PACK)}$	PACK input block resistor(2)	PACK	1			k Ÿ

(1) Use an external resistor to limit the current to GPOD to 1 mA in high voltage application.
(2) Use an external resistor to limit the in-rush current PACK pin required.

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ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted), T_A = ±40 ƒC to 85 ƒC, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 ‹F, $C_{(REG33)}$ = 2.2 ‹F; typical values at T_A = 25 ƒC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ZVCHG)}$	ZVCHG clamp voltage	BAT = 4.5 V	3.3	3.5	3.7	V
LOGIC; T_A = ±40 ƒC to 100 ƒC (unless otherwise noted)						
$R_{(PULLUP)}$	Internal pullup resistance	$\overline{ALERT}$	60	100	200	k Ÿ
		$\overline{RESET}$	1	3	6	
V_{OL}	Logic low output voltage level	$\overline{ALERT}$			0.2	V
		$\overline{RESET}$; $V_{(BAT)}$ = 7 V; $V_{(REG25)}$ = 1.5 V; $I_{(\overline{RESET})}$ = 200 A			0.4	
		GPOD; $I_{(GPOD)}$ = 50 A			0.6	
LOGIC SMBC, SMBD, $\overline{PFIN}$, $\overline{PRES}$, SAFE, ALERT, $\overline{DISP}$						
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	Output voltage high(1)	I_L = ±0.5 mA	V_{REG25} ±0.5			V
V_{OL} bits	Low-level output voltage	$\overline{PRES}$, $\overline{PFIN}$, $\overline{ALERT}$, $\overline{DISP}$; I_L = 7 mA;			0.4	V
C_I	Input capacitance			5		pF
$I_{(SAFE)}$	SAFE source currents	SAFE active, SAFE = $V_{(REG25)}$ ±0.6 V	±3			mA
$I_{lkg(SAFE)}$	SAFE leakage current	SAFE inactive	±0.2		0.2	‹A
I_{lkg}	Input leakage current				1	‹A
ADC(2)						
		ernal V	±0.2		1	
				31.5		
			6			
	Effective			15		
	Integral n				“0.03	
	Offset erro					

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ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted), T_A = ±40 ƒC to 85 ƒC, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 ‹F, $C_{(REG33)}$ = 2.2 ‹F; typical values at T_A = 25 ƒC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage(11)			±2.0		mV/ ƒC
VOLTAGE REFERENCE						
	Output voltage		1.215	1.225	1.230	V
	Output voltage drift			65		PPM/ ƒC
HIGH FREQUENCY OSCILLATOR						
$f_{(OSC)}$	Operating frequency			4.194		MHz
$f_{(EIO)}$	Frequency error (12) (13)		±3%	0.25%	3%	
		T_A = 20 ƒC to 70 ƒC	±2%	0.25%	2%	
$t_{(SXO)}$	Start-up time(14)			2.5	5	ms
LOW FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(13) (15)		±2.5%	0.25%	2.5%	
		T_A = 20 ƒC to 70 ƒC	±1.5%	0.25%	1.5%	
$t_{(LSXO)}$	Start-up time(14)				500	‹s

(11) ±53.7 LSB/ ƒC
(12) The frequency error is measured from 4.194 MHz.
(13) The frequency drift is included and measured from the trimmed frequency at $V_{(REG25)}$ = 2.5 V, T_A = 25 ƒC.
(14) The startup time is defined as the time it takes for the oscillator output frequency to be ‘3%.
(15) The frequency error is measured from 32.768 kHz.

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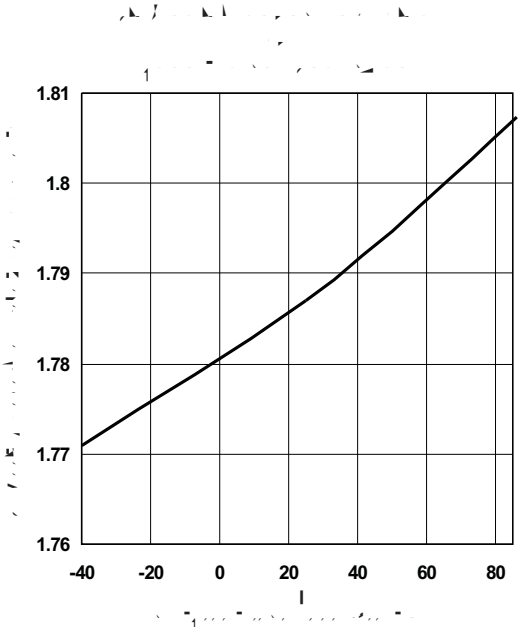
POWER-ON RESET

Over operating free-air temperature range (unless otherwise noted), T_A = ±40 ƒC to 85 ƒC, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 ‹F, $C_{(REG33)}$ = 2.2 ‹F; typical values at T_A = 25 ƒC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIT ±	Negative-going voltage input		1.7	1.8	1.9	V
VHYS	Power-on reset hysteresis		5	125	200	mV
t_{RST}	$\overline{RESET}$ active low time	Active low time after power up or watchdog reset	100	250	560	‹s



DATA FLASH CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Typical values at T_A = 25 ƒC and $V_{(REG25)}$ = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See (1)	10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				200	ms
$t_{(PAGEERASE)}$	Page-erase time				20	ms
$I_{(DDPROG)}$	Flash-write supply current			5	10	mA
$I_{(DDERASE)}$	Flash-erase supply current			5	10	mA
RAM/REGISTER BACKUP						
$I_{(RB)}$	RB data-retention input current	$V_{(RBI)}$! $V_{(RBI)MIN}$, V_{REG25} V_{IT} ±, T_A = 85 ƒC		1000	2500	nA
		$V_{(RBI)}$! $V_{(RBI)MIN}$, V_{REG25} V_{IT} ±, T_A = 25 ƒC		90	220	
$V_{(RB)}$	RB data-retention input voltage (1)		1.7			V

(1) Specified by design. Not production tested.

SMBus TIMING CHARACTERISTICS

T_A = ±40 ƒC to 85 ƒC Typical Values at T_A = 25 ƒC and V_{REG25} = 2.5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SMB)}$	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz

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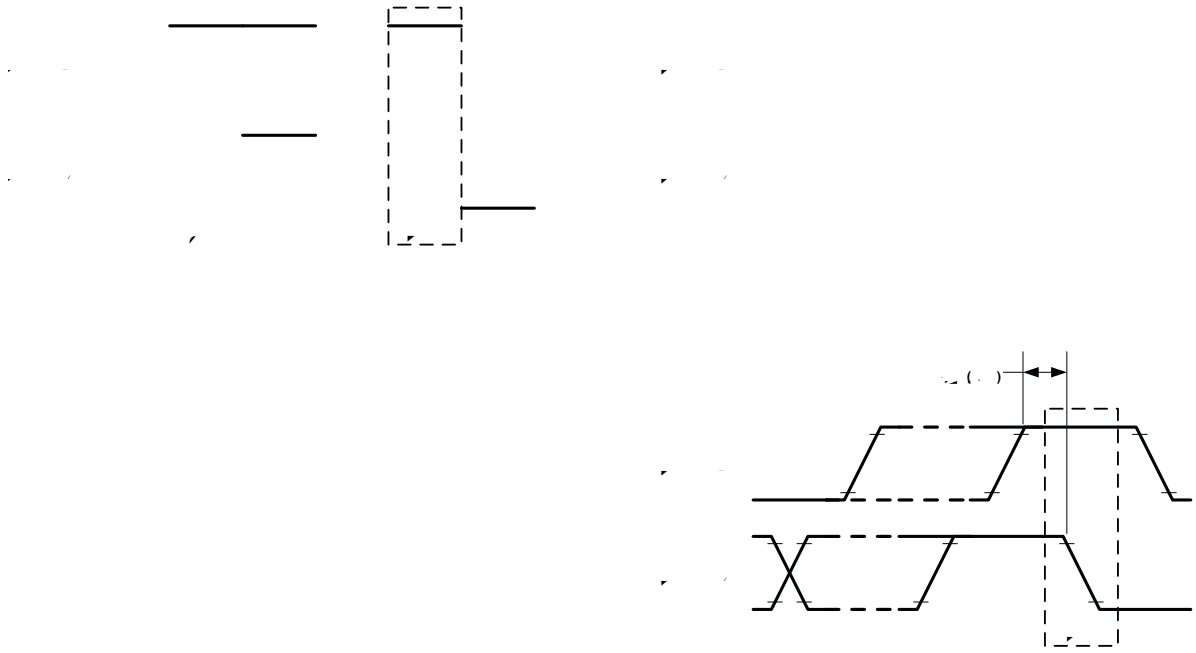
SMBus TIMING CHARACTERISTICS (continued)

T_A = –40 °C to 85 °C Typical Values at T_A = 25 °C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(MAS)}$	SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
$t_{(BUF)}$	Bus free time between start and stop (See 8/F2 9 ET BT /F2 8 Tf 100 Tz 0 0 0 rHD:DAT34 641.3 Td (4.7)Tj ET BT /F3 8 Tf 0 100 T58/F2 9 Recei62.7 6310 rg 103U(clo 641.3 Td (4.7		4.7			s

4.7 4.7



A. SCLKACK is the acknowledge-related clock pulse generated by the master.

Figure 1. SMBus Timing Diagram

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FEATURE SET

Primary (1st Level) Safety Features

The bq34z651 supports a wide range of battery and system protection features that can be easily configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq34z651 can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- 2nd-level protection IC input
- Safety overcurrent in charge and discharge
- Safety over-temperature in charge and discharge with independent alarms and thresholds for each thermistor
- Charge FET and zero-volt charge FET fault
- Discharge FET fault
- Cell imbalance detection (active and at rest)
- Open thermistor detection
- Fuse blow detection
- AFE communication fault

Charge Control Features

The bq34z651 charge control features include:

- Supports JEITA temperature ranges. [illegible]

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note (SLUA364) for further details.

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Lifetime Data Logging Features

The bq34z651 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored include:

- Lifetime maximum temperature
- Lifetime maximum temperature count
- Lifetime maximum temperature duration
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime maximum battery cell voltage count
- Lifetime maximum battery cell voltage duration
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average

CONFIGURATION

Oscillator Function

The bq34z651 fully integrates the system oscillators; therefore, no external components are required for this feature.

System

COMMUNICATIONS

The bq34z651 uses SMBus v1.1 with Master Mode and packet error checking (PEC) options per the SBS specification.

SMBus On and Off State

The bq34z651 detects an SMBus off state when SMBC and SMBD are logic-low for • 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

SBS Commands

Table 2. SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	Hex	2	0x0000	0xffff	[2]	[2]
0x01	R/W	RemainingCapacityAlarm	Integer	2	0	700 or 1000	300 or 432	mAh or 10 mWh
0x02	R/W	RemainingTimeAlarm	Unsigned integer	2	0	30	10	min
0x03	R/W	BatteryMode	Hex	2	0x0000	0xffff	[2]	[2]
0x04	R/W	AtRate	Integer	2	±32,768	32,767	[2]	mA or 10 mW
0x05	R	AtRateTimeToFull	Unsigned integer	2	0	65,535	[2]	min
0x06	R	AtRateTimeToEmpty	Unsigned integer	2	0	65,535	[2]	min
0x07	R	AtRateOK	Unsigned integer	2	0	65,535	[2]	[2]
0x08	R	Temperature	Unsigned integer	2	0	65,535	[2]	0.1 ƒK
0x09	R	Voltage	Unsigned integer	2	0	20,000	[2]	mV
0x0a	R	Current	Integer	2	±32,768	32767	[2]	mA
0x0b	R	AverageCurrent	Integer	2	±32,768	32,767	[2]	mA
0x0c	R	MaxError	Unsigned integer	1	0	100	[2]	%
0x0d	R	RelativeStateOfCharge	Unsigned integer	1	0	100	[2]	%
0x0e	R	AbsoluteStateOfCharge	Unsigned integer	1	0	100+	[2]	%
0x0f	R/W	RemainingCapacity	Unsigned integer	2	0	65,535	[2]	mAh or 10 mWh
0x10	R	FullChargeCapacity	Unsigned integer	2	0	65,535	[2]	mAh or 10 mWh
0x11	R	RunTimeToEmpty	Unsigned integer	2	0	65,534	[2]	min
0x12	R	AverageTimeToEmpty	Unsigned integer	2	0	65,534	[2]	min
0x13	R	AverageTimeToFull	Unsigned integer	2	0	65,534	[2]	min
0x14	R	ChargingCurrent	Unsigned integer	2	0	65,534	[2]	mA
0x15	R	ChargingVoltage	Unsigned integer	2	0	65,534	[2]	mV
0x16	R	BatteryStatus	Hex	2	0x0000	0xdbff	[2]	[2]
0x17	R/W	CycleCount	Unsigned integer	2	0	65,535	0	[2]
0x18	R/W	DesignCapacity	Integer	2	0	32,767	4400 or 6336	mAh or 10 mWh
0x19	R/W	DesignVoltage	Integer	2	7000	18,000	14,400	mV

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Table 3. EXTENDED SBS COMMANDS (continued)

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x6c	R	ManufBlock1	String	20	[2]	[2]	[2]	[2]
0x6d	R	ManufBlock2	String	20	[2]	[2]	[2]	[2]
0x6e	R	ManufBlock3	String	20	[2]	[2]	[2]	[2]
0x6f	R	ManufBlock4	String	20	[2]	[2]	[2]	[2]
0x70	R/W	ManufacturerInfo	String	31+1	[2]	[2]	[2]	[2]
0x71	R/W	SenseResistor	Unsigned	2	0	65G305.2 Td (0)Tj ET BT /F2 8 Tf3 ET BT /F2		

APPLICATION SCHEMATIC

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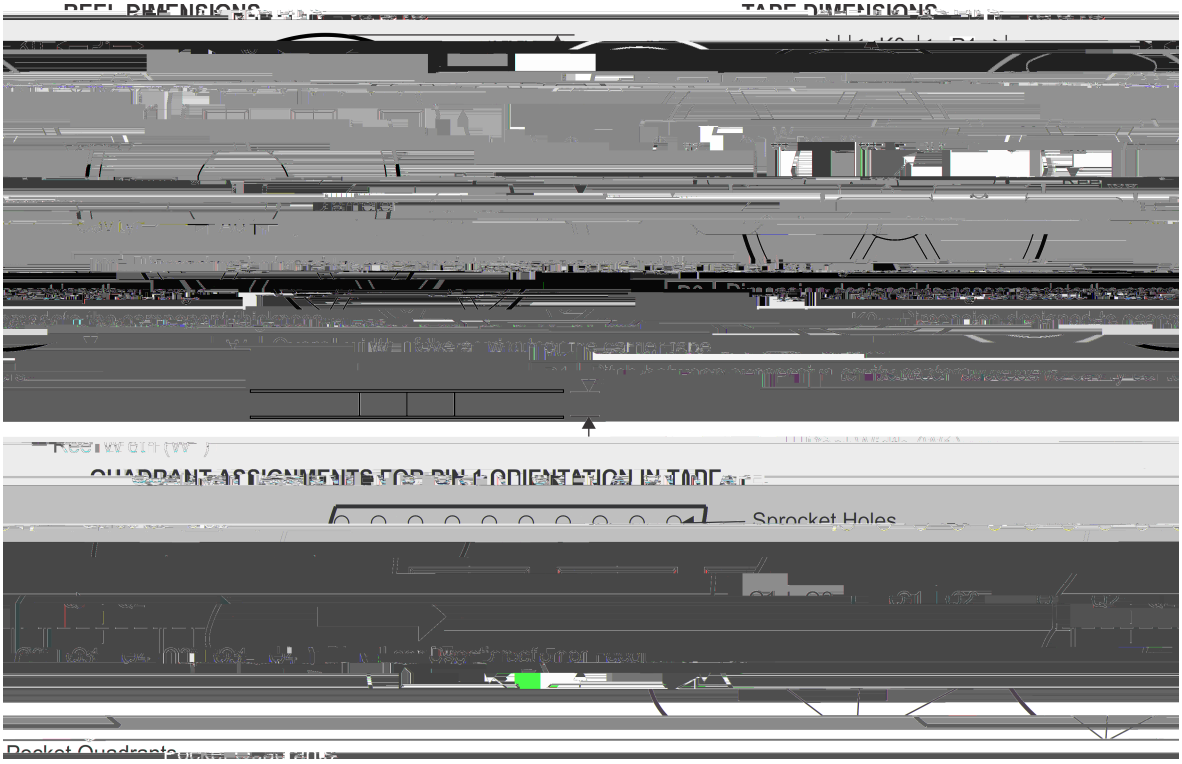
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ34Z651DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	-40 to 85	BQ34Z651	Samples
BQ34Z651DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ34Z651	Samples

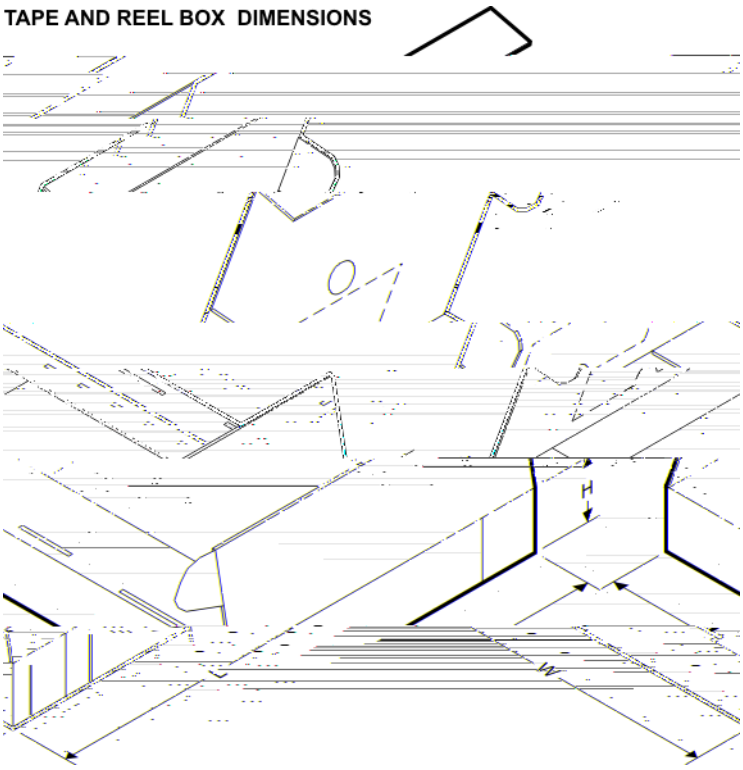
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND:

TAPE AND REEL INFORMATION



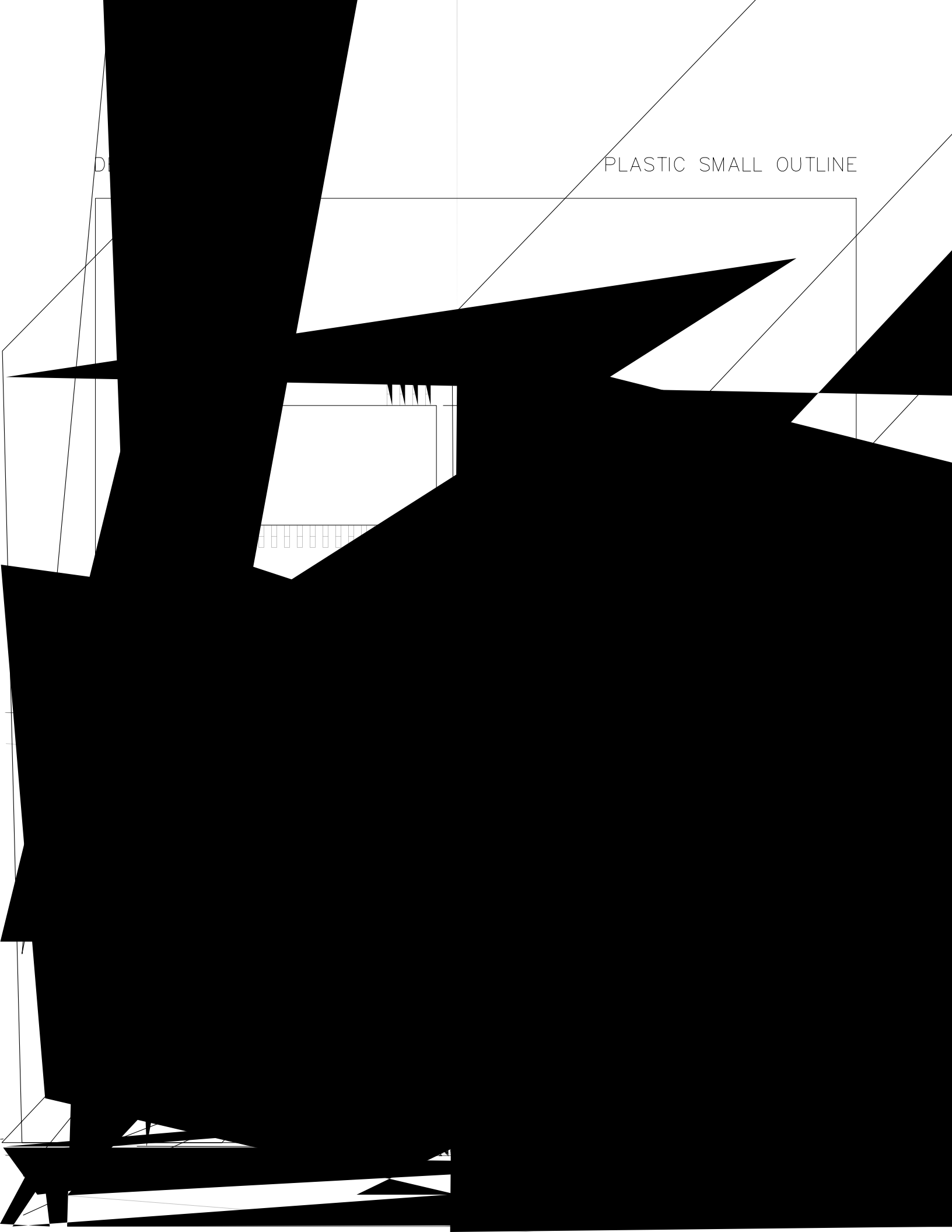
*All dimensions are nominal

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ34Z651DBTR	TSSOP	DBT	44	2000	367.0	367.0	45.0


PLASTIC SMALL OUTLINE

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