

Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

Check for Samples: [bq771600](#), [bq771601](#), [bq771602](#)

FEATURES

- 2-, 3-, and 4-Series Cell Overvoltage Protection
- External Capacitor-Programmed Delay Timer
- Fixed OVP Threshold
- High-Accuracy Overvoltage Protection:
±10 mV
- Low Power Consumption $I_{CC} \approx 1 \mu A$
($V_{CELL(ALL)} < V_{PROTECT}$)
- Low Leakage Current Per Cell Input < 100 nA
- Small Package Footprint
 - 8-pin QFN (3 mm x 4 mm)

APPLICATIONS

- Power Tools
- UPS Battery Backup
- Light Electric Vehicles
 - eBike
 - eScooter
 - Pedal Assist Bicycles

DESCRIPTION

The bq7716xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq7716xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

For quicker production-line testing, the bq7716xy device provides a Customer Test Mode with greatly reduced delay time.

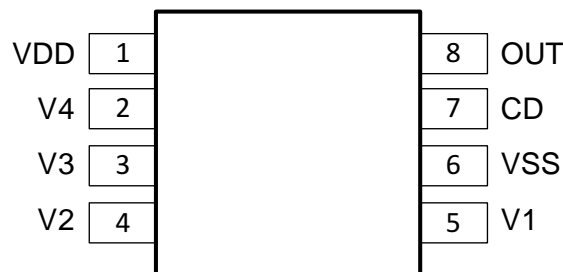


Figure 1. bq7716xy Pinout



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Drive	Tape and Reel (Large)	Tape and Reel (Small)
-40°C to 110°C	bq771600	8-pin QFN	DPJ	4.300	0.300	CMOS Active High	bq771600DPJR	bq771600DPJT
	bq771601			4.225	0.050	CMOS Active High	bq771601DPJR	bq771601DPJT
	bq771602			4.225	0.050	NCH Active Low, Open Drain	bq771602DPJR	bq771602DPJT
	bq771603 ⁽¹⁾			4.325	0.050	NCH Active Low, Open Drain	bq771603DPJR	bq771603DPJT
	bq7716xy ⁽²⁾			3.850–4.650	0–0.300	CMOS Active High or NCH Active Low, Open Drain	bq7716xyTBD	bq7716xyTBD

- (1) Product Preview only
 (2) Future Option, contact TI.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		bq7716xy	UNITS
		8 PINS	
JA	Junction-to-ambient thermal resistance	56.6	°C/W
JC(top)	Junction-to-case(top) thermal resistance	56.4	
JB	Junction-to-board thermal resistance	30.6	
JT	Junction-to-top characterization parameter	1.0	
JB	Junction-to-board characterization parameter	37.8	
JC(bottom)	Junction-to-case(bottom) thermal resistance	11.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PIN FUNCTIONS

bq771600	Pin Name	Type I/O	Description
1	VDD	P	Power supply
2	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
3	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
4	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
5	V1	I	Sense input for positive voltage of the lowest cell in the stack
6	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
7	CD	I/O	External capacitor connection for delay timer
8	OUT	OA	Output drive for overvoltage fault signal

PIN DETAILS

In the bq7716xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV} . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a threshold, the timer circuit is disabled and the CD pin returns to VSS. When the CD pin falls below a threshold, the timer circuit is disabled and the CD pin returns to VSS.

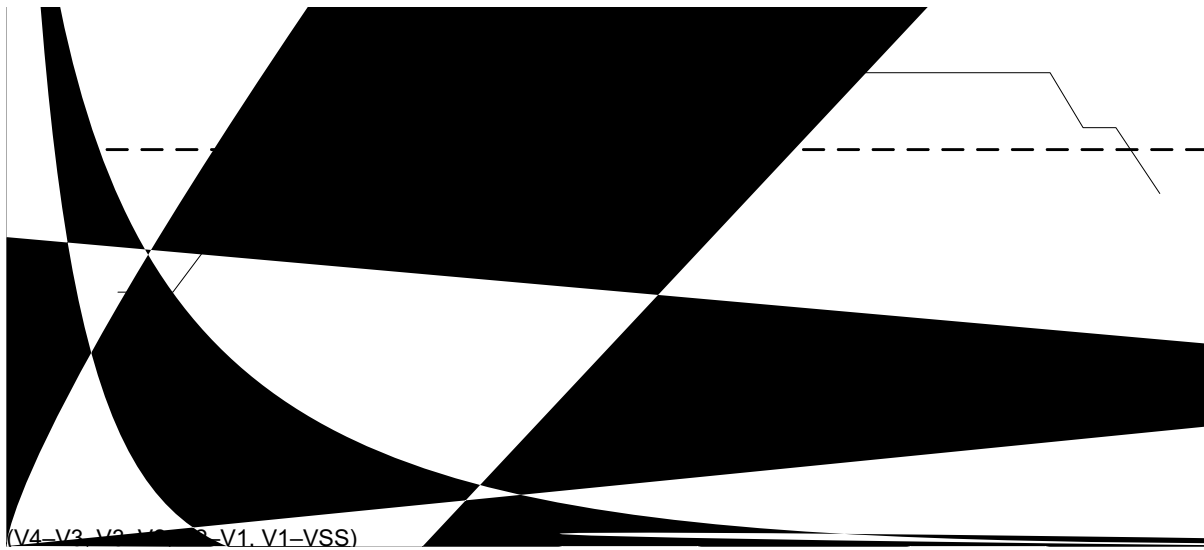


Figure 3 shows the behavior of the CD pin during an OV sequence.

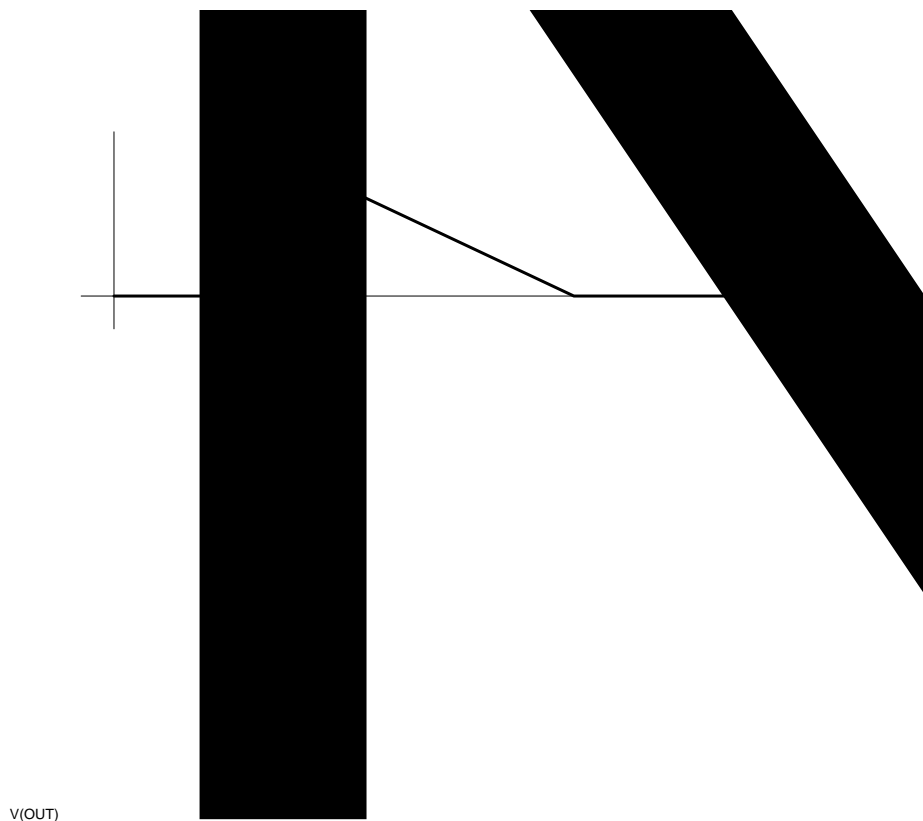


Figure 3. CD Pin Mechanism

Sense Positive Input for V_x

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

External Delay Capacitor, CD

This terminal is connected to an external capacitor that is used for setting the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

DC CHARACTERISTICS (continued)

Typical values stated where T_A

TYPICAL CHARACTERISTICS

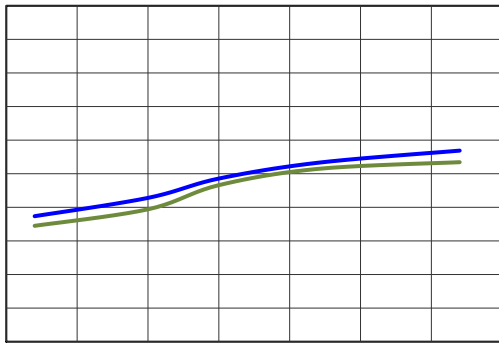


Figure 4. Overtolerance Threshold (OVT) vs. Temperature

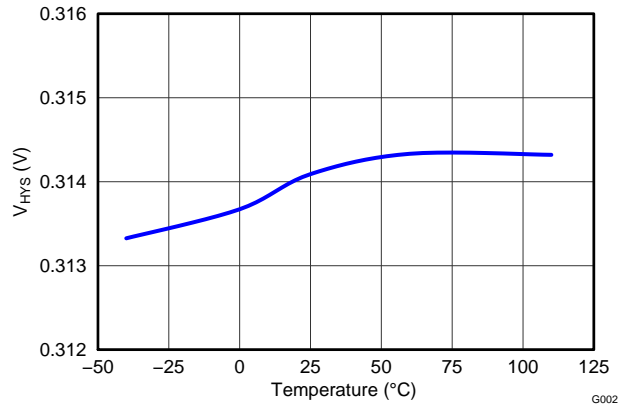


Figure 5. Hysteresis V_{HYS} vs. Temperature

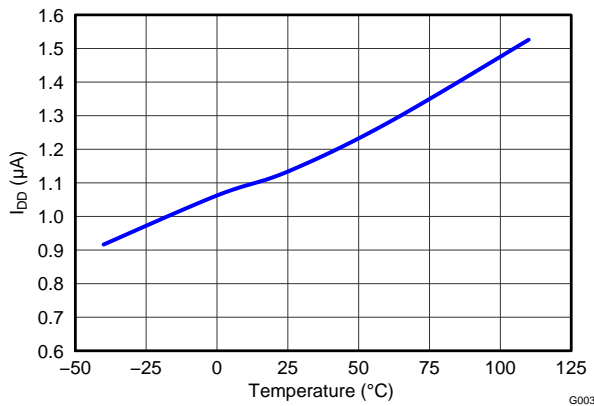


Figure 6. I_{DD} Current Consumption vs. Temperature at $V_{DD} = 16\text{ V}$

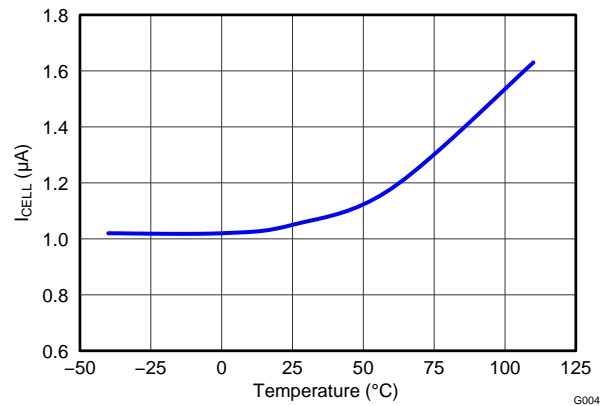


Figure 7. I_{CELL} vs. Temperature at $V_{CELL} = 9.2\text{ V}$

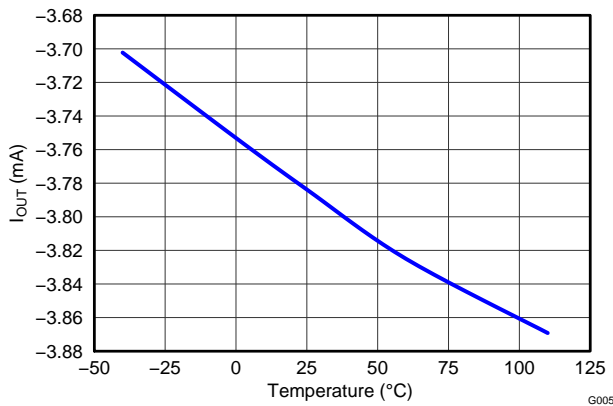


Figure 8. Output Current I_{OUT} vs. Temperature

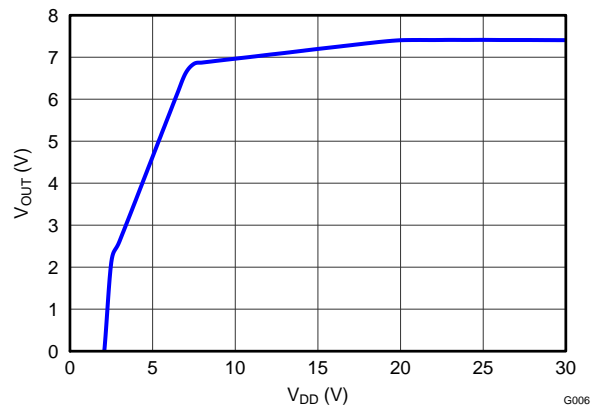


Figure 9. V_{OUT} vs. V_{DD}

APPLICATION SCHEMATIC

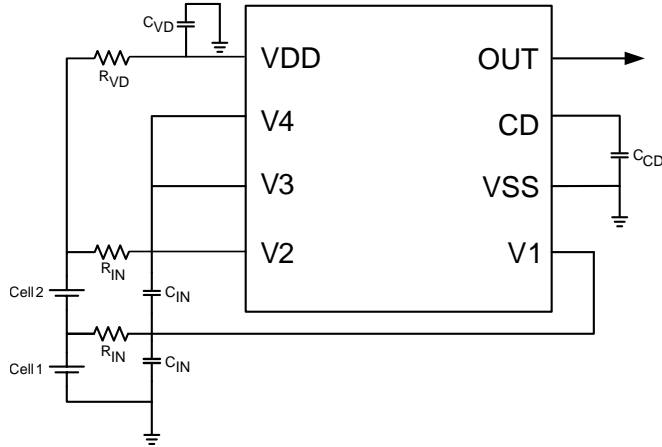


Figure 11. 2-Series Cell Configuration with Capacitor-Programmed Delay

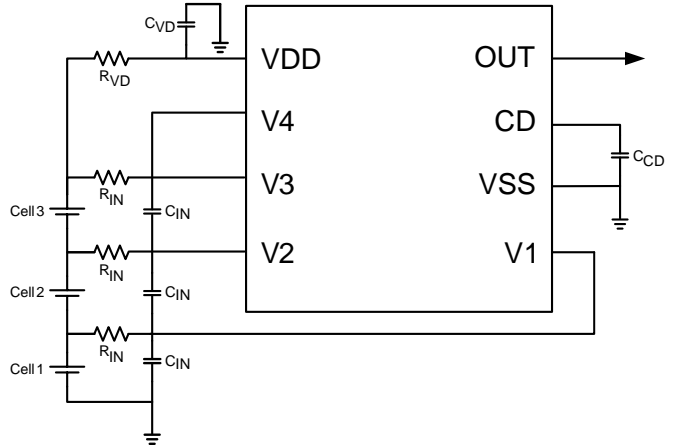


Figure 12. 3-Series Cell Configuration with Capacitor-Programmed Delay

NOTE

In these application examples of 2s and 3s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

CUSTOMER TEST MODE

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CHGDELAY)}$ value, which has a maximum of 170 ms.

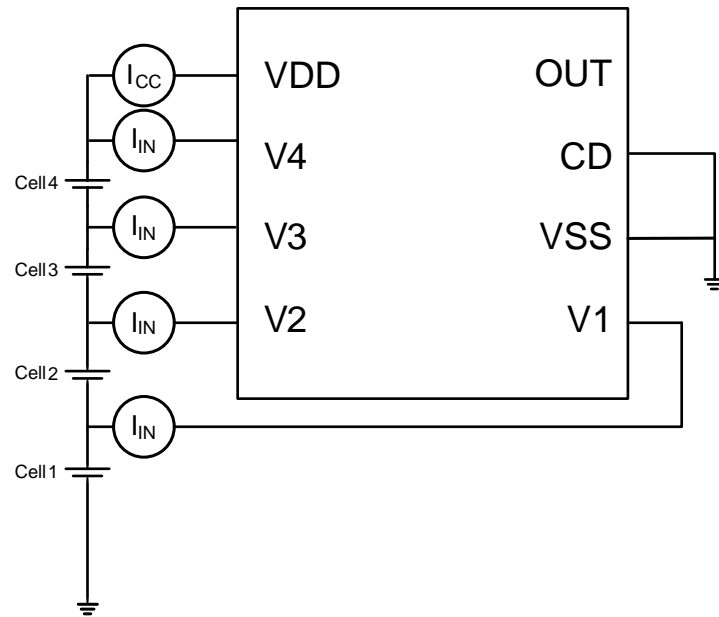
CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 13 shows the timing for the Customer Test Mode.

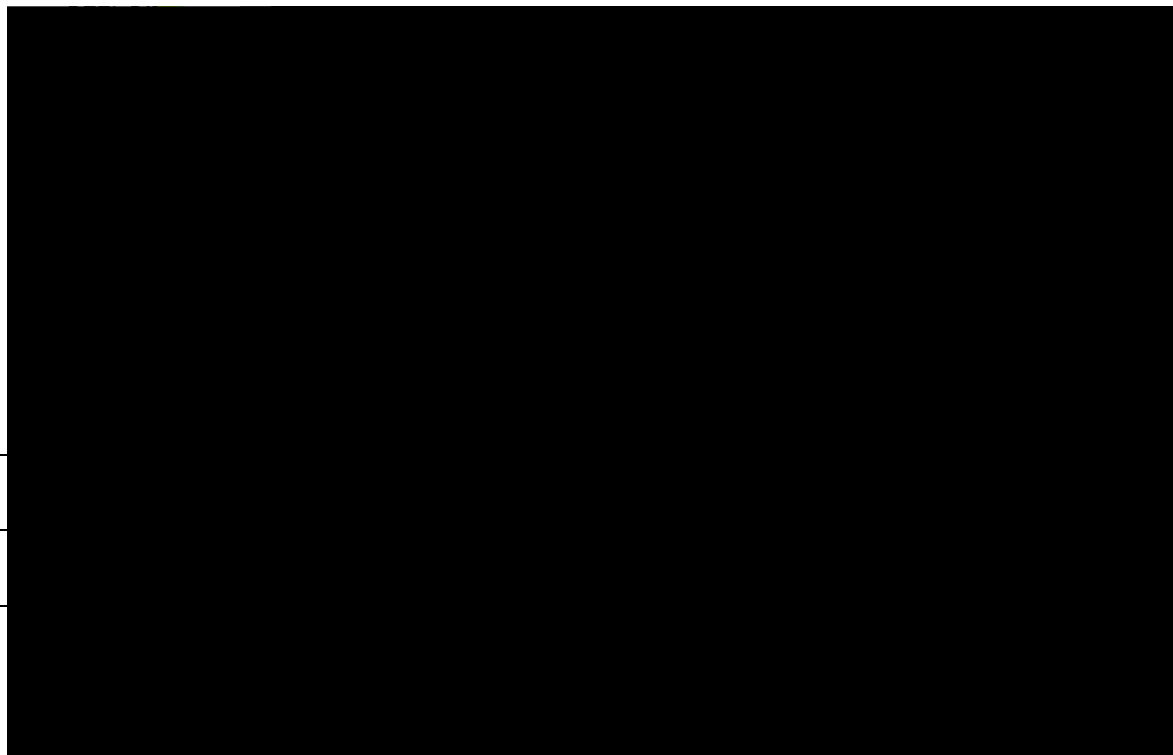


Figure 13. Timing for Customer Test Mode



In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771600DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771600DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771600DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771601DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771601DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771602DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771602DPJT	WSON	DPJ	8	250	210.0	185.0	35.0

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