Hi-performance Regulator IC Series for PCs

PGOOD IC for PC

BD4140HFV

No.09030EBT18

●Description

BD4140HFV is 1ch reset IC for watching the voltage. The detected voltage is 0.5V, and it is available to several kinds of voltage with additional external resistance. For the independent supply voltage (VCC), the “L” level of voltage is guaranteed in case the watching input voltage is also low.

●Features

1) Open drain output type
2) Built in Under Voltage LockOut (UVLO) circuit
3) HVSOF5 package : 1.6×1.6×0.6(mm)

●Applications

Laptop PC, Desktop PC, LCD-TV, Printer, STV, Digital appliances

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	BD4140HFV	Unit
Terminal voltage	VCC, IN, DLY, PGOOD	6 *1	V
Power Dissipation	Pd	0.67 *2	W
PGOOD Capacity Current	IPGOOD	5	mA
Operating temperature range	Topr	-10～+100	℃
Storage temperature range	Tstg	-55～+150	℃
Junction Temperature	Tjmax	+150	℃

*1 Do not however exceed Pd.
*2 Reduced by θ_{ja}= 186.6℃W for increase in Ta of 1℃ over 25℃.
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 1 layer. (copper foil density :2%))
*3 Reduced by θ_{ja}= 185.2℃W for increase in Ta of 1℃ over 25℃
(when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB which has 1 layer.)

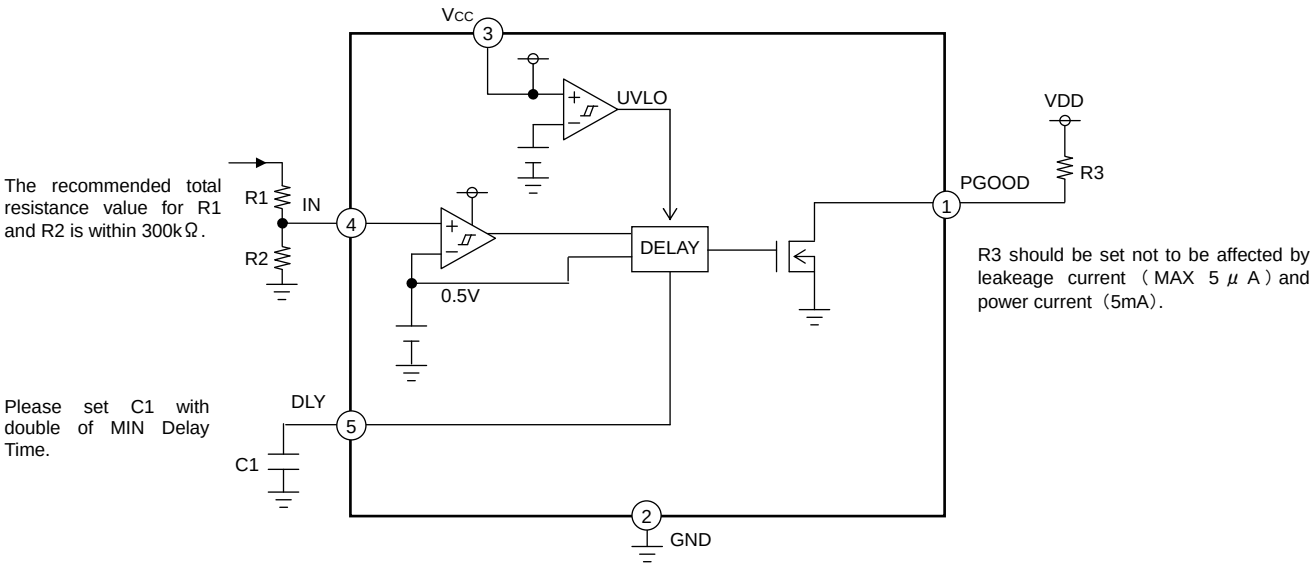
●Operating Conditions (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Terminal voltage	VCC	3.0	5.5	V
	IN	-0.3	V_{CC}-2	V
	PGOOD	-0.3	5.5	V
	DLY	-0.3	V_{CC}	V

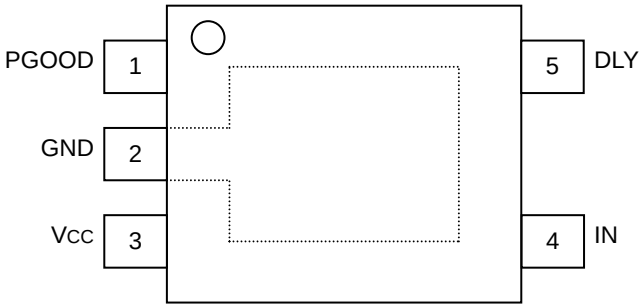
●ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta=25℃, VCC=5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Bias Current	Icc	-	5	10	μA	-
Detected Voltage	VDET	491	500	509	mV	IN sweep up
Hysteresis Voltage	VHYS	-	10	-	mV	IN sweep down
Delay Current	IDLY	150	250	350	nA	IN=0.6V
PGOOD Output ON Resistance	RVOUT	-	100	200	Ω	IN=0V
PGOODOutput Leak Current	IOUT	-	0	5	μA	IN=0.6V

●Block Diagram



●Pin Layout



●Pin Function Table

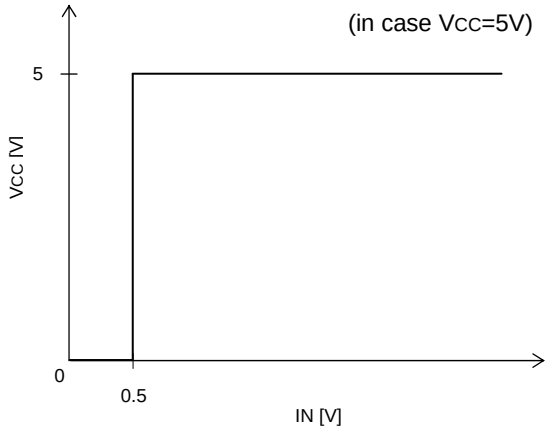
PIN No.	PIN Name	PIN Function
1	PGOOD	Reset Output Pin (Power Good Signal)
2	GND	Ground Pin
3	Vcc	Power Supply Input Pin
4	IN	Watching Voltage Input Pin
5	DLY	Capacitor connected pin for setting delay time
Bottom	FIN	Substrate

●Explanation of Operation

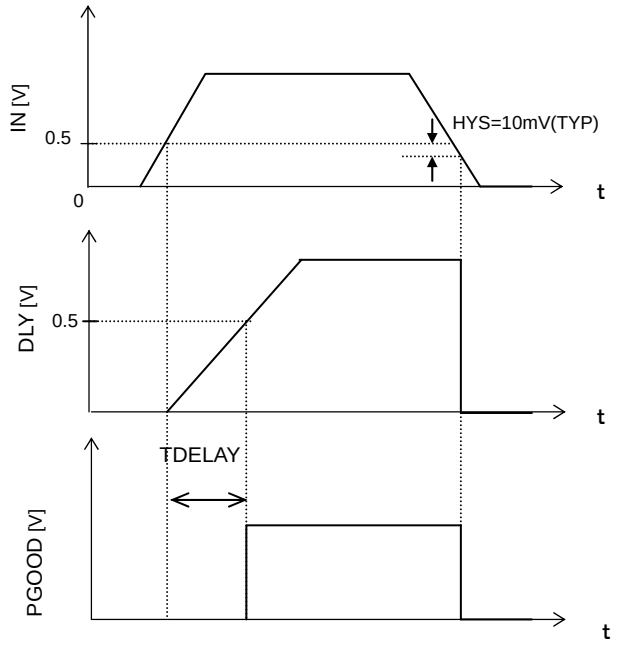
BD4140HFV is 1ch reset IC with independent supply voltage.

The following voltage is available to input VCC voltage before the watching input voltage.

(Input-output voltage characteristic)



(Detected delay time setting)



T_{DELAY} is calculated with formula below.

$$T_{DELAY}\,[sec] = \frac{C_{EXT}\,[\mu F] \times 0.5}{0.25\,[\mu A]}$$

$$= 2 \times C_{EXT}[pF] \times 10^{-6}$$

$$C_{EXT}\,[pF] = T_{DELAY}\,[sec] / (2 \times 10^{-6})$$

(Example) When using the 4700pF capacitor,

$$T_{DELAY}\,[sec] = 2 \times 4700\,[pF] \times 10^{-6}$$

$$= 9400 \times 10^{-6} = 9.4\,[ms]$$

(Example) When setting 2ms Delay,

$$C_{EXT} = 2\,[ms] \times 0.25\,[uA] / 0.5$$

$$= \frac{2 \times 10^{-3} \times 0.25 \times 10^{-6}}{0.5}$$

$$= 1 \times 10^{-9}$$

$$= 1000[pF]$$

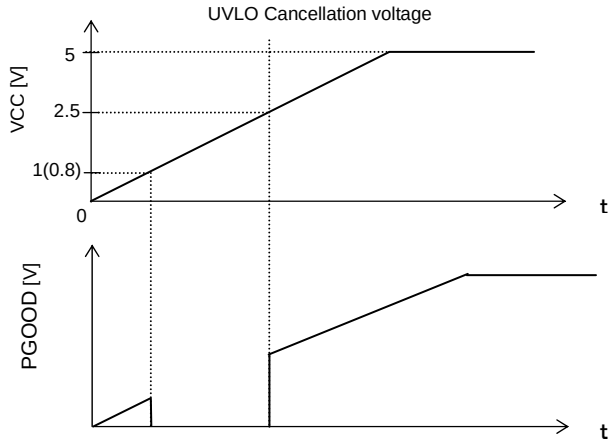
<VCC starting>

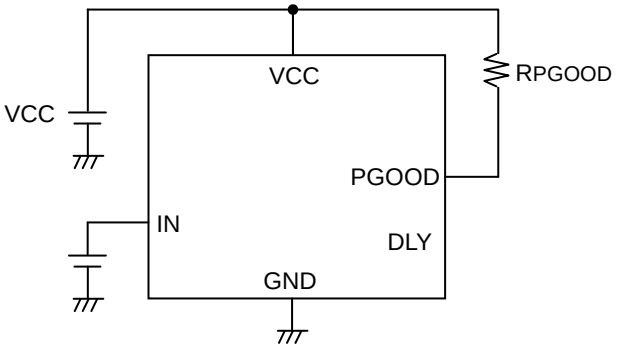
① When VCC is below the minimum operation voltage, PGOOD pin will be at H level.
(The meaning of the minimum operation voltage is : When the starting of VCC, PGOOD output voltage become within 10% of VCC voltage, and the value will be around 0.8VTYP(RPGOOD=100kΩ) and 1.0VTYP(RPGOOD=10kΩ). But note that this value is reference.)

② If VCC value exceeds the minimum operation voltage, by the VCC reached UVLO cancellation voltage (2.5V TYP), PGOOD output become at L level.

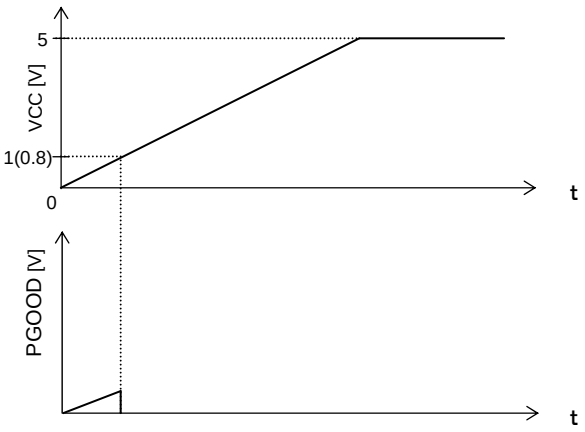
③ If VCC exceeds UVLO cancellation voltage, when the input voltage of IN pin is over the detected voltage, PGOOD pin will be at H level, and when the input voltage of IN pin is below the detected voltage, PGOOD pin will be at L level.

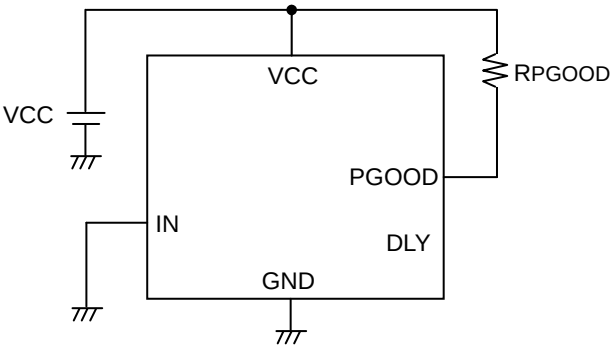
(PGOOD=OK)





(PGOOD=NG)

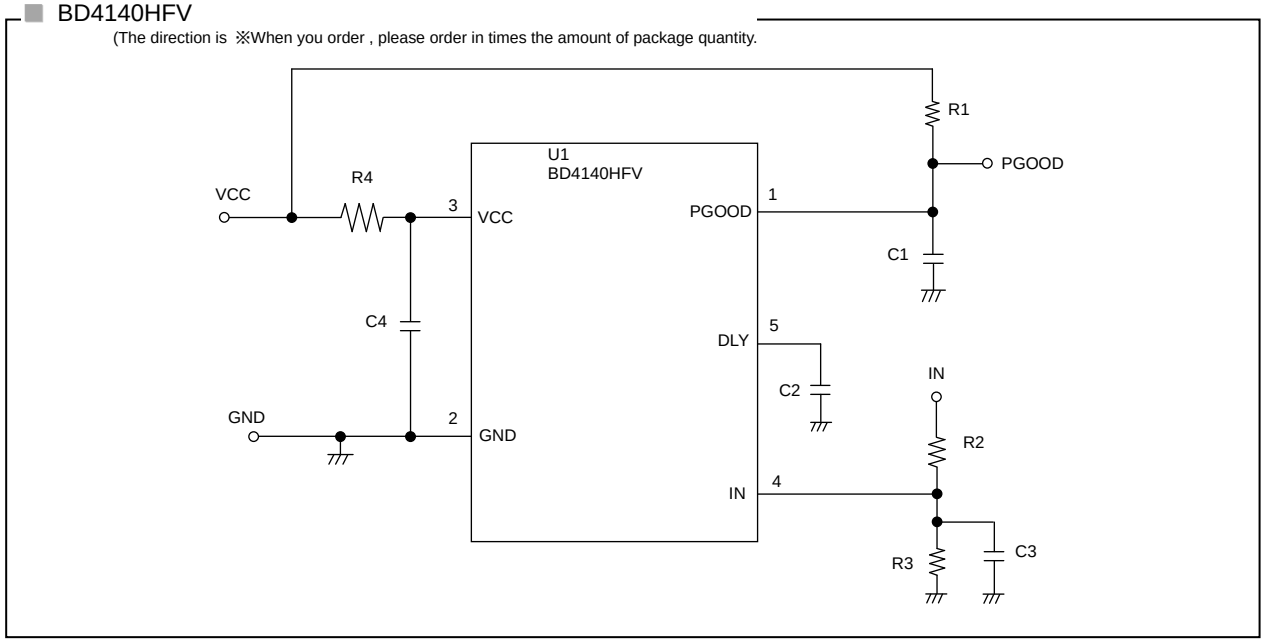




●Evaluation Board Circuit

■ BD4140HFV

(The direction is ※When you order , please order in times the amount of package quantity.



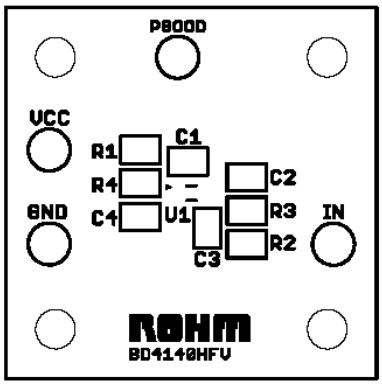
■ **BD4140HFV Evaluation Board Standard Component List (at detecting 0.5V)**

Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD4140HFV
C1	-	-	-
C2	1000pF	murata	GRM1552C1H102JA01
C3	-	-	-
C4	-	-	-

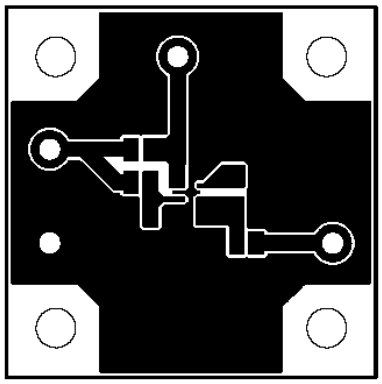
Component	Rating	Manufacturer	Product Name
R1	100kΩ	ROHM	
R2	0Ω	-	jumper
R3	-	-	-
R4	0Ω	-	jumper

■ **BD4140HFV Evaluation Board Layout**

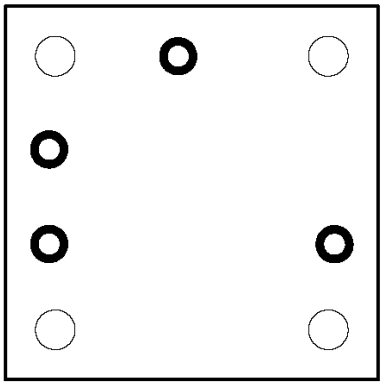
Silk screen (Top)



TOP Layer



Bottom Layer



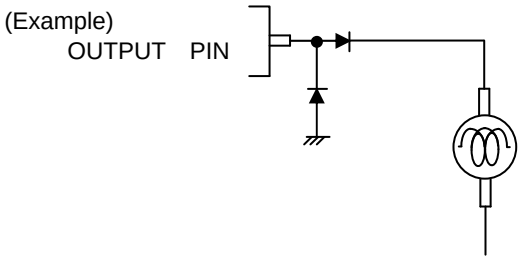
●Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Power supply lines

Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.



3. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

4. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

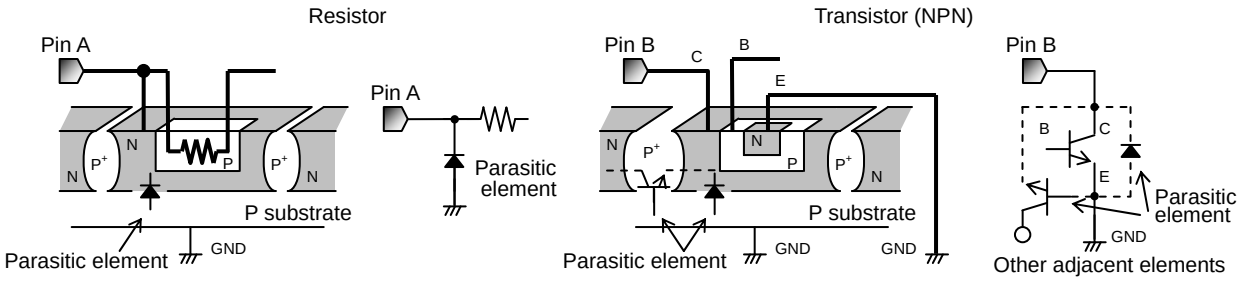
7. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

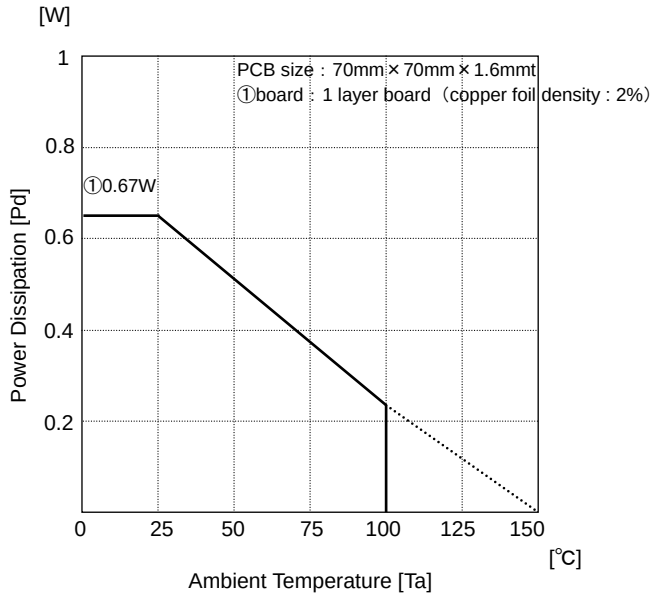
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



●Power Dissipation Characteristics

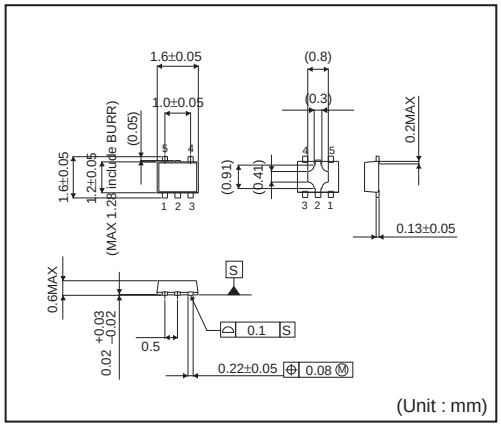
◎HVSOF5



●Ordering part number

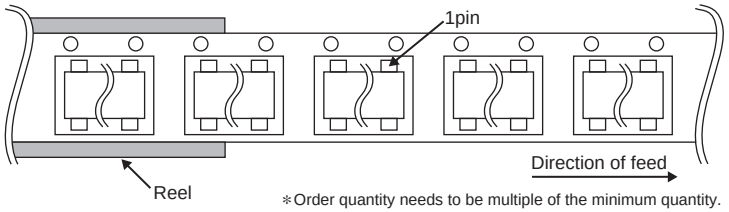
B	D	4	1	4	0	H	F	V	-	T	R
Part No.		Part No.				Package FV : HVSOF5				Packaging and forming specification TR: Embossed tape and reel	

HVSOF5



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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