These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Table 1. AVAILABLE OPTIONS

T_A	PACKAGE(1)	
	44-PIN TSSOP (DBT) Tube	44-PIN TSSOP (DBT) Tape and Reel
–40°C to 85°C	bq34z653DBT(2)	bq34z653DBTR(3)

(1) For the most current package and ordering information, see the Package Option Adm p b ackage"m Package

TYPICAL APPLICATION

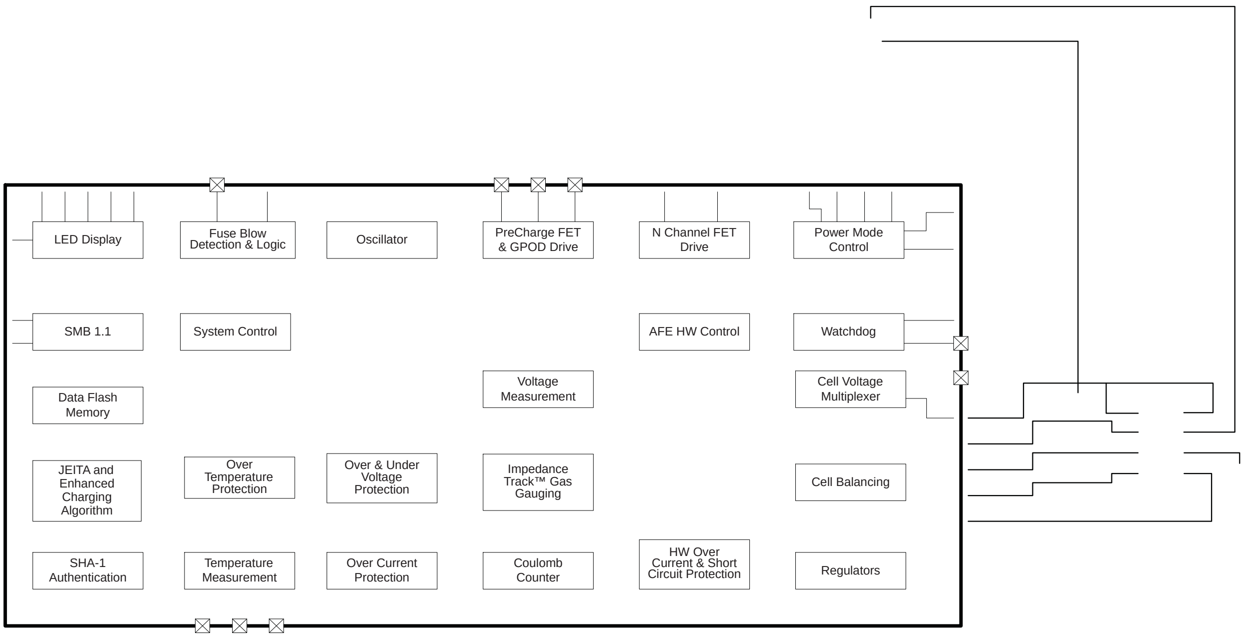


Figure 1. System Partitioning Diagram

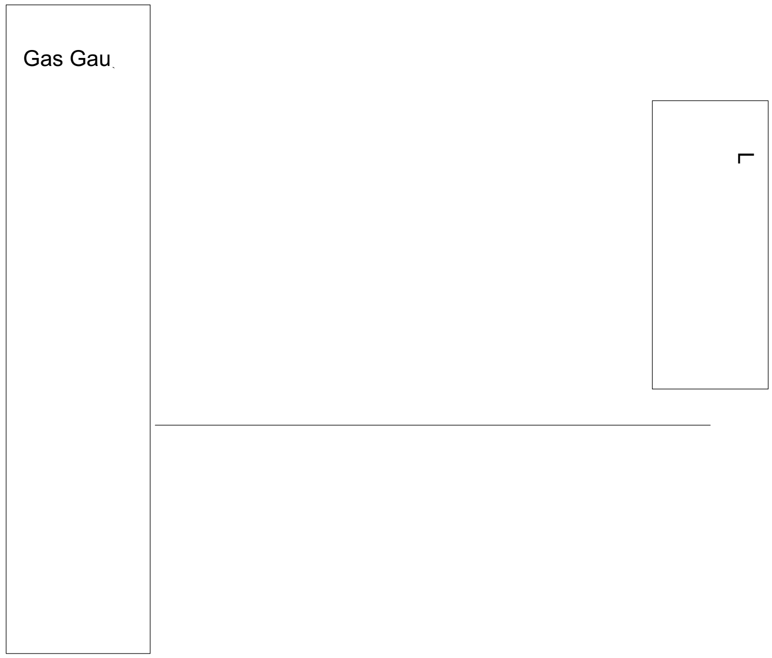
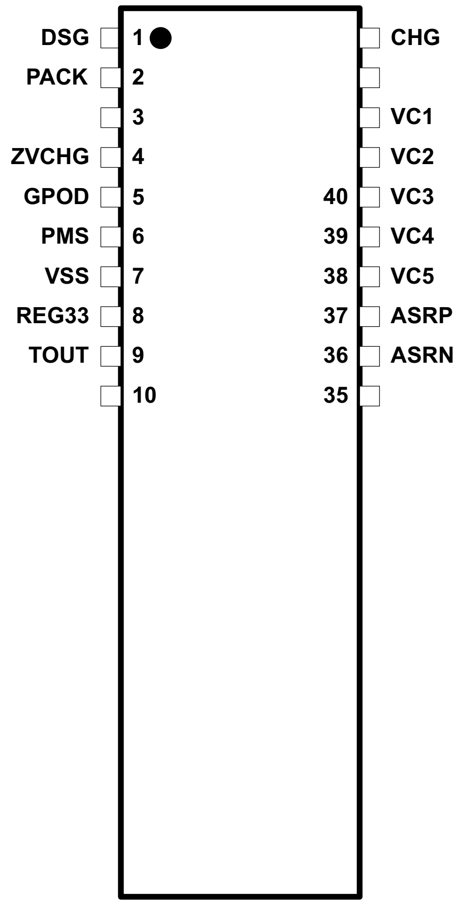


Figure 2. Typical LCD Implementation

PACKAGE PINOUT DIAGRAM

DBT PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O (1)	DESCRIPTION
NO.	NAME		
1	DSG	O	High-side N-channel discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wake up when device is in SHUTDOWN mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input.
4	ZVCHG	O	P-channel pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. It can be configured to be used in pre-charge condition.
6	PMS	I	PRE-CHARGE mode setting input. Connect to PACK to enable 0v pre-charge using charge FET connected at CHG pin. Connect to VSS to disable 0-V pre-charge using charge FET connected at CHG pin.
7	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
8	REG33	P	3.3-V regulator output. Connect at least a 2.2-μF capacitor to REG33 and VSS.
9	TOUT	P	Thermistor bias supply output
10	VCELL+	—	Internal cell voltage multiplexer and amplifier output. Connect a 0.1µF-capacitor to VCELL+ and VSS.
11	$\overline{\text{ALERT}}$	I/OD	Alert output. In case of short circuit condition, overload condition and watchdog timeout, this pin will be triggered.
12	COM	O	Output/open drain: LCD common connection

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

PIN FUNCTIONS (continued)

PIN NO.	PIN NAME	I/O[1]	DESCRIPTION
13	TS1	IA	1st thermistor voltage input connection to monitor temperature
14	TS2	IA	2nd thermistor voltage input connection to monitor temperature
15	PRES	I	Active low input to sense system insertion. Typically requires additional ESD protection.
16	PFIN	I	Active low input to detect secondary protector status, and to allow the bq34z653 to report the status of the 2nd-level protection input
17	SAFE	O	Active high output to enforce additional level of safety protection; e.g., fuse blow
18	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq34z653
19	NC	—	
19	ᵌA א ess andthe bq34z653		
19	~~NC~~	—	us to ´4zè ᴰ l
1/	m ᴑ "	traضto ad	do monifedth tomE ! • a in ᵐ bq] l

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature (unless otherwise noted) (1)

		PIN	UNIT
V_{SS}	Supply voltage range	BAT, VCC	–0.3 V to 34 V
		PACK, PMS	–0.3 V to 34 V
		VC(n) – VC(n+1); n = 1, 2, 3, 4	–0.3 V to 8.5 V
		VC1, VC2, VC3, VC4	–0.3 V to 34 V
		VC5	–0.3 V to 1 V
V_{IN}	Input voltage range	$\overline{PFIN}$, SMBD, SMBC. LED1, LED2, LED3, LED4, LED5, $\overline{DISP}$	–0.3 V to 6 V
		TS1, TS2, SAFE, VCELL+, $\overline{PRES}$, $\overline{ALERT}$	–0.3 V to $V_{(REG25)}$ + 0.3 V
		$\overline{MRST}$, GSRN, GSRP, RBI	–0.3 V to $V_{(REG25)}$ + 0.3 V
		ASRN, ASRP	–1 V to 1 V
V_{OUT}	Output voltage range	DSG, CHG, GPOD	–0.3 V to 34 V
		ZVCHG	–0.3 V to $V_{(BAT)}$
		TOUT, $\overline{ALERT}$, REG33	–0.3 V to 6 V
		$\overline{RESET}$	–0.3 V to 7 V
		REG25	–0.3 V to 2.75 V
I_{SS}	Maximum combined sink current for input pins	$\overline{PRES}$, $\overline{PFIN}$, SMBD, SMBC, LED1, LED2, LED3, LED4, LED5	50 mA
T_A	Operating free-air temperature range		–40°C to 85°C
T_F	Functional temperature		–40°C to 100°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage	VCC, BAT	4.5		25	V
$V_{(STARTUP)}$	Minimum startup voltage	VCC, BAT, PACK	5.5			V
V_{IN}	Input Voltage Range	VC(n) – VC(n+1); n = 1,2,3,4	0		5	V
		VC1, VC2, VC3, VC4	0		V_{SUP}	V
		VC5	0		0.5	V
		ASRN, ASRP	–0.5		0.5	V
		PACK, PMS	0		25	V
$V_{(GPOD)}$	Output Voltage Range	GPOD	0		25	V
$A_{(GPOD)}$	Drain Current (1)	GPOD			1	mA
$C_{(REG25)}$	2.5-V LDO Capacitor	REG25	1			µF
$C_{(REG33)}$	3.3-V LDO Capacitor	REG33	2.2			µF
$C_{(VCELL+)}$	Cell Voltage Output Capacitor	VCELL+	0.1			µF
$C_{(PACK)}$	PACK input block resistor (2)	PACK	1			kΩ

(1) Use an external resistor to limit the current to GPOD to 1 mA in high voltage application.
(2) Use an external resistor to limit the in-rush current PACK pin required.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(NORMAL)}$	Firmware running			550		µA
$I_{(SLEEP)}$	SLEEP mode	CHG FET on; DSG FET on		124		µA
		CHG FET off; DSG FET on		90		µA
		CHG FET off; DSG FET off		52		µA
$I_{(SHUTDOWN)}$	SHUTDOWN mode			0.1	1	µA
SHUTDOWN WAKE; T_A = 25°C (unless otherwise noted)						
$I_{(PACK)}$	SHUTDOWN exit at $V_{STARTUP}$ threshold				1	µA
SRx WAKE FROM SLEEP; T_A = 25°C (unless otherwise noted)						
$V_{(WAKE)}$	Positive or negative wake threshold with 1.00 mV, 2.25 mV, 4.5 mV and 9 mV programmable options		1.25		10	mV
$V_{(WAKE\_ACR)}$	Accuracy of $V_{(WAKE)}$	$V_{(WAKE)}$ = 1 mV; $I_{(WAKE)}$= 0, RSNS1 = 0, RSNS0 = 1;	–0.7		0.7	mV
		$V_{(WAKE)}$ = 2.25 mV; $I_{(WAKE)}$ = 1, RSNS1 = 0, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0;	–0.8		0.8	
		$V_{(WAKE)}$ = 4.5 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0;	–1.0		1.0	
		$V_{(WAKE)}$ = 9 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1;	–1.4		1.4	
$V_{(WAKE\_TCO)}$	Temperature drift of $V_{(WAKE)}$ accuracy			0.5		%/°C
$t_{(WAKE)}$	Time from application of current and wake of bq34z653			1	10	ms
WATCHDOG TIMER						
t_{WDTINT}	Watchdog start up detect time		250	500	1000	ms
t_{WDWT}	Watchdog detect time		50	100	150	µs
2.5-V LDO; $I_{(REG33OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG25)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG25OUT)}$ ≤ 16 mA; T_A = –40°C to 100°C	2.41	2.5	2.59	V
$\Delta V_{(REG25TEMP)}$	Regulator output change with temperature	$I_{(REG25OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2		%
$\Delta V_{(REG25LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG25OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG25LOAD)}$	Load Regulation	0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 2 mA		7	25	mV
		0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 16 mA		25	50	
$I_{(REG25MAX)}$	Current Limit	Drawing current until REG25 = 2 V to 0 V	5	40	75	mA
3.3-V LDO; $I_{(REG25OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG33)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ ≤ 25 mA; T_A = –40°C to 100°C	3	3.3	3.6	V
$\Delta V_{(REG33TEMP)}$	Regulator output change with temperature	$I_{(REG33OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2		%
$\Delta V_{(REG33LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG33LOAD)}$	Load Regulation	0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 2 mA		7	17	mV
		0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 25 mA		40	100	
$I_{(REG33MAX)}$	Current Limit	Drawing current until REG33 = 3 V	25	100	145	mA
		Short REG33 to VSS, REG33 = 0 V	12		65	
THERMISTOR DRIVE						
$V_{(TOUT)}$	Output voltage	$I_{(TOUT)}$ = 0 mA; T_A = 25°C		$V_{(REG25)}$		V

[redacted]

ELECTRICAL CHARACTERISTICS (continue[redacted]

Over operating free-air temperature range (unless otherw[redacted]
$V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS-300<(TEST)-d <00241.61 -1.8 Td <0024>T0(CONDI24>Tj 56000039000115 0.4<0024>M		

ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

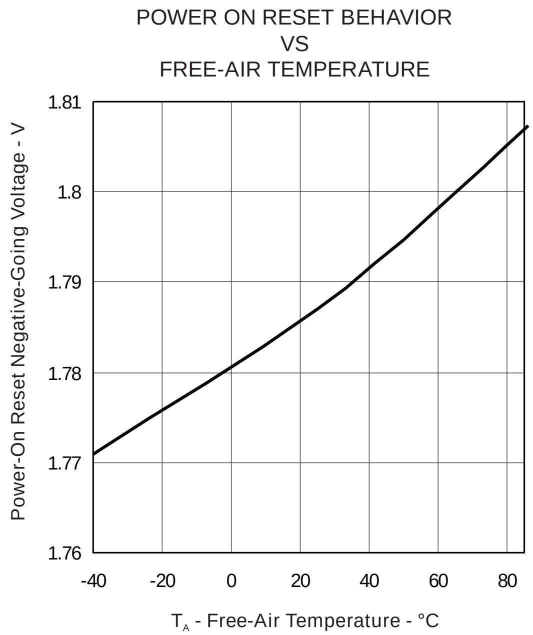
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Effective input resistance[10]	T_A = 25°C to 85°C	2.5			MΩ
INTERNAL TEMPERATURE SENSOR						
$V_{(TEMP)}$	Temperature sensor voltage[11]			–2.0		mV/°C
VOLTAGE REFERENCE						
	Output voltage		1.215	1.225	1.230	V
	Output voltage drift			65		PPM/°C
HIGH FREQUENCY OSCILLATOR						
$f_{(OSC)}$	Operating frequency			4.194		MHz
$f_{(EIO)}$	Frequency error [12] [13]		–3%	0.25%	3%	
		T_A = 20°C to 70°C	–2%	0.25%	2%	
$t_{(SXO)}$	Start-up time[14]			2.5	5	ms
LOW FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error[13] [15]		–2.5%	0.25%	2.5%	
		T_A = 20°C to 70°C	–1.5%	0.25%	1.5%	
$t_{(LSXO)}$	Start-up time[14]				500	µs

(10) The CC input is a switched capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.
(11) –53.7 LSB/°C
(12) The frequency error is measured from 4.194 MHz.
(13) The frequency drift is included and measured from the trimmed frequency at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(14) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.
(15) The frequency error is measured from 32.768 kHz.

POWER-ON RESET

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 µF, $C_{(REG33)}$ = 2.2 µF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIT–	Negative-going voltage input		1.7	1.8	1.9	V
VHYS	Power-on reset hysteresis		5	125	200	mV
t_{RST}	$\overline{\text{RESET}}$ active low time	Active low time after power up or watchdog reset	100	250	560	µs



DATA FLASH CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Typical values at T_A = 25°C and $V_{(REG25)}$ = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See [1]	10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				200	ms
$t_{(PAGEERASE)}$	Page-erase time				20	ms
$I_{(DDPROG)}$	Flash-write supply current			5	10	mA
$I_{(DDERASE)}$	Flash-erase supply current			5	10	mA
RAM/REGISTER BACKUP						
$I_{(RB)}$	RB data-retention input current	$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT–}$, T_A = 85°C		1000	2500	nA
		$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT–}$, T_A = 25°C		90	220	
$V_{(RB)}$	RB data-retention input voltage[2]		1.7			V

(1) Specified by design. Not production tested.
(2) Specified by design. Not production tested.

SMBus TIMING CHARACTERISTICS

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

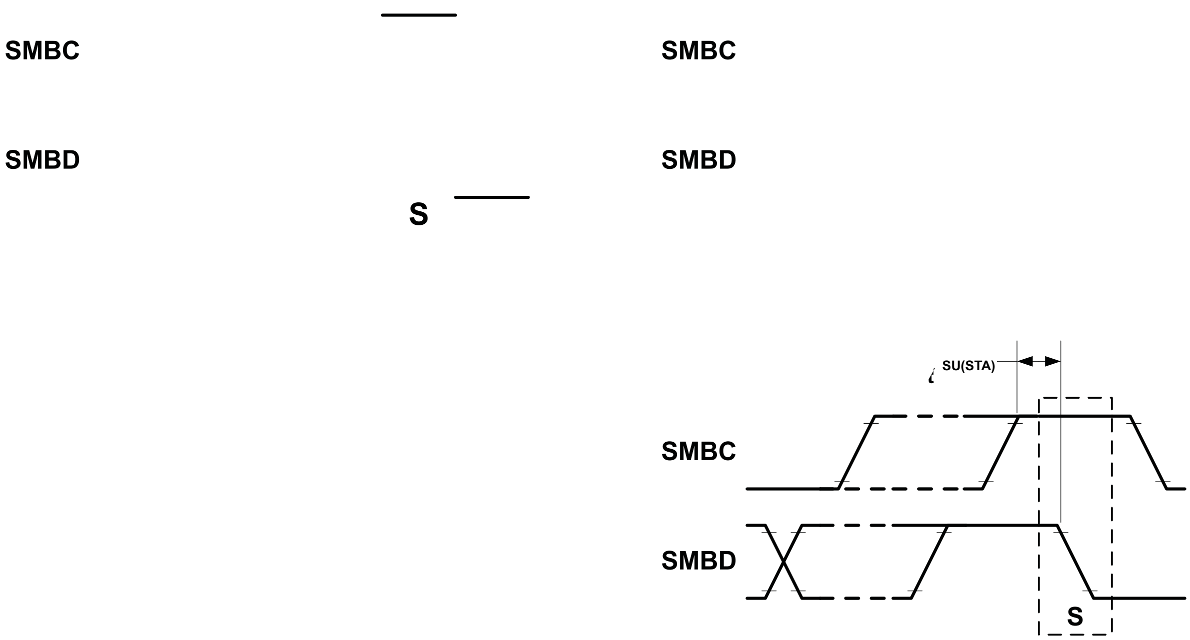
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SMB)}$	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
$f_{(MAS)}$	SMBus master clock frequency	MASTER mode, No clock low slave extend		51.2		kHz
$t_{(BUF)}$	Bus free time between start and stop (See Figure 3.)		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start (See Figure 3.)		4			µs
$t_{(SU:STA)}$	Repeated start setup time (See Figure 3.)		4.7			µs
$t_{(SU:STO)}$	Stop setup time (See Figure 3.)		4			µs
$t_{(HD:DAT)}$	Data hold time (See Figure 3.)	RECEIVE mode	0			ns
		TRANSMIT mode	300			

SMBus TIMING CHARACTERISTICS (continued)

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SU:DAT)}$	Data setup time (See Figure 3.)		250			ns
$t_{(TIMEOUT)}$	Error signal/detect (See Figure 3.)	See (1)	25		35	µs
$t_{(LOW)}$	Clock low period (See Figure 3.)		4.7			µs
$t_{(HIGH)}$	Clock high period (See Figure 3.)	See (2)	4		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{(LOW:MEXT)}$	Cumulative clock low master extend time (See Figure 3.)	See (4)			10	ms
t_f	Clock/data fall time	See (5)			300	ns
t_r	Clock/data rise time	See (6)			1000	ns

(1) The bq34z653 times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving bq34z653 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{(LOW:MEXT)}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time t_r = VILMAX – 0.15) to (VIHMIN + 0.15)
(6) Fall time t_f = $0.9V_{DD}$ to (VILMAX – 0.15)



A. SCLKACK is the acknowledge-related clock pulse generated by the master.

Figure 3. SMBus Timing Diagram

FEATURE SET

Primary (1st Level) Safety Features

The bq34z653 supports a wide range of battery and system protection features that can be easily configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq34z653 can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- 2nd-level protection IC input
- Safety overcurrent in charge and discharge
- Safety over-temperature in charge and discharge with independent alarms and thresholds for each thermistor
- Charge FET and zero-volt charge FET fault
- Discharge FET fault
- Cell imbalance detection (active and at rest)
- Open thermistor detection
- Fuse blow detection
- AFE communication fault

Charge Control Features

The bq34z653 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges, and for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Determines the chemical state of charge of each battery cell using Impedance Track, and can reduce the charge difference of the battery cells in a fully charged state of the battery pack, gradually using the cell balancing algorithm during charging. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms
- Battery heater control to allow battery charging in low ambient temperatures

Gas Gauging

The bq34z653 uses the Impedance Track Technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge discharge learning cycle required.

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note (SLUA364) for further details.

Lifetime Data Logging Features

The bq34z653 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored include:

- Lifetime maximum temperature
- Lifetime maximum temperature count
- Lifetime maximum temperature duration
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime maximum battery cell voltage count
- Lifetime maximum battery cell voltage duration
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average discharge current
- Lifetime maximum average discharge power
- Lifetime average temperature

Authentication

The bq34z653 supports authentication by the host using SHA-1.

Power Modes

The bq34z653 supports three different power modes to reduce power consumption:

- In NORMAL mode, the bq34z653 performs measurements, calculations, protection decisions and data updates in 1-second intervals. Between these intervals, the bq34z653 is in a reduced power stage.
- In SLEEP mode, the bq34z653 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq34z653 is in a reduced power stage. The bq34z653 has a wake function that enables exit from SLEEP mode when current flow or failure is detected.
- In SHUTDOWN mode, the bq34z653 is completely disabled.

CONFIGURATION

Oscillator Function

The bq34z653 fully integrates the system oscillators; therefore, no external components are required for this feature.

System Present Operation

The bq34z653 periodically verifies the $\overline{PRES}$ pin and detects that the battery is present in the system via a low state on a $\overline{PRES}$ input. When this occurs, the bq34z653 enters NORMAL operating mode. When the pack is removed from the system and the $\overline{PRES}$ input is high, the bq34z653 enters the battery-removed state, disabling the charge, discharge, and ZVCHG FETs. The $\overline{PRES}$ input is ignored and can be left floating when non-removal mode is set in the data flash.

BATTERY PARAMETER MEASUREMENTS

The bq34z653 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

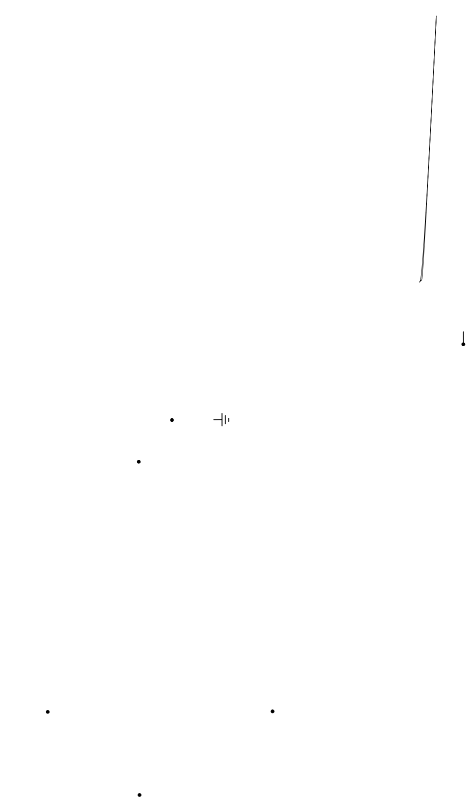
Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq34z653 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$

Table 3. EXTENDED SBS COMMANDS (continued)

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x6c	R	ManufBlock1	String	20	—	—	—	—
0x6d	R	ManufBlock2	String	20	—	—	—	—
0x6e	R	ManufBlock3	String	20	—	—	—	—
0x6f	R	ManufBlock4	String	20	—	—	—	—
0x70	R/W	ManufacturerInfo	String	31+1	—	—	—	—
0x71	R/W	SenseResistor	Unsigned integer	2	0	65,535	—	μΩ
0x72	R	TempRange	Hex	2	—	—	—	—
0x73	R	LifetimeData1	String	32+1	—	—	—	—
0x74	R	LifetimeData2	String	8+1	—	—	—	—
0x77	R/W	DataFlashSubClassID	Hex	2	0x0000	0xffff	—	—
0x78	R/W	DataFlashSubClassPage1	Hex	32	—	—	—	—
0x79	R/W	DataFlashSubClassPage2	Hex	32	—	—	—	—
0x7a	R/W	DataFlashSubClassPage3	Hex	32	—	—	—	—
0x7b	R/W	DataFlashSubClassPage4	Hex	32	—	—	—	—
0x7c	R/W	DataFlashSubClassPage5	Hex	32	—	—	—	—
0x7d	R/W	DataFlashSubClassPage6	Hex	32	—	—	—	—
0x7e	R/W	DataFlashSubClassPage7	Hex	32	—	—	—	—
0x7f	R/W	DataFlashSubClassPage8	Hex	32	—	—	—	—

APPLICATION SCHEMATIC



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ34Z653DBT	ACTIVE	TSSOP	DBT	44	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-250C-1 YEAR	
BQ34Z653DBTR	ACTIVE	TSSOP	DBT	44	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is o(bume) 1 leadframe. The component isanTsi 16.444 Tm [in speci Th

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ34Z653DBTR	TSSOP	DBT	44	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

[redacted]

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ34Z653DBTR	TSSOP	DBT	44	2000	367.0	367.0	45.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265