These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

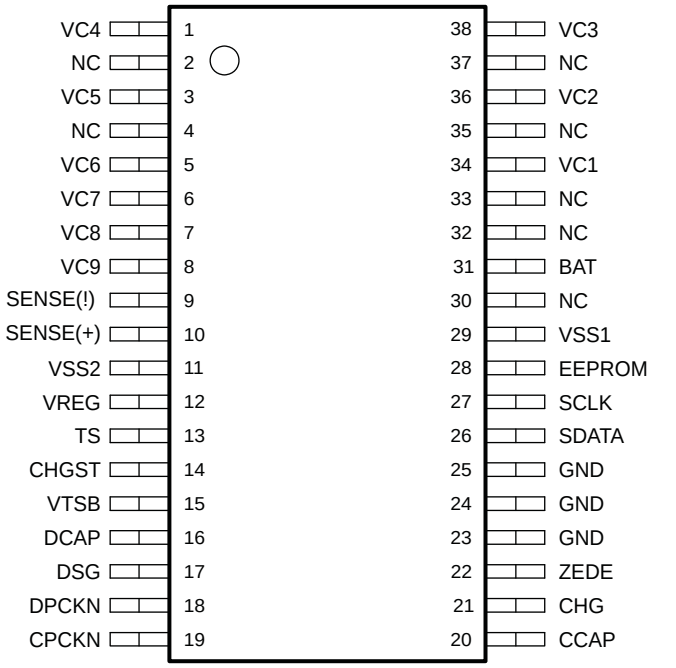
PIN DETAILS

PIN FUNCTIONS (38-Pin Package)

PIN		DESCRIPTION
NAME	NO.	
BAT	31	Power supply voltage, tied to highest cell(+)
CCAP	20	Energy storage capacitor for charge FET drive
CHG	21	Charge FET (n-channel) gate drive
CHGST	14	Charger-status input, used to detect charger connection/wakeup
CPCKN	19	Pack – charger negative terminal (charger return)
DCAP	16	Energy storage capacitor for discharge FET drive
DPCKN	18	Pack – discharge negative terminal (load return)
DSG	17	Discharge FET (n-channel) gate drive
EEPROM	28	EEPROM programming voltage input. Connect to VSS for normal operation.
GND	23, 24, 25	Logic ground (not for power return or analog reference). Tie to VSS.
NC	2, 4, 30, 32, 33, 35, 37	No connect (DO NOT CONNECT) externally. Failure to leave NC pins open can cause faulty operation.
SCLK	27	Serial-communication clock input used for EEPROM programming
SDATA	26	Serial-communication data input/output used for EEPROM programming (open-drain)
SENSE(+)	10	Current-sense input
SENSE(–)	9	Current-sense input
TS	13	Temperature sensing input
VC1	34	Sense-voltage input terminal for most-positive cell
VC2	36	Sense-voltage input terminal for second-most-positive cell
VC3	38	Sense-voltage input terminal for third-most-positive cell
VC4	1	Sense-voltage input terminal for fourth-most-positive cell
VC5	3	Sense-voltage input terminal for fifth-most-positive cell
VC6	5	Sense-voltage input terminal for sixth-most-positive cell
VC7	6	Sense-voltage input terminal for seventh-most-positive cell
VC8	7	Sense-voltage input terminal for eighthmost-positive (most-negative) cell
VC9	8	Most-negative cell(–) terminal (BAT–)
VREG	12	Integrated 3.3-V regulator output
VSS1	29	Analog ground (substrate reference)
VSS2	11	Analog ground (substrate reference)
VTSB	15	Thermistor bias supply (sourced from VREG)
ZEDE	22	*Zero Delay* test mode pin. Enables serial communications interface and minimizes protection delay times when connected to logic high. Connect to VSS for normal operation. A strong connection is recommended.

PIN DIAGRAM – bq77908 – 38-Pin SSOP DBT PACKAGE

DBT PACKAGE
(TOP VIEW)



P0034-05

FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PACKAGING
bq77908DBT	TSSOP	50-piece tube
bq77908DBTR	TSSOP	2000-piece reel

THERMAL INFORMATION (continued)

THERMAL METRIC[1]		bq77908 DBT 38 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter[7]	33.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[8]	N/A	°C/W

(7) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
Supply voltage		BAT[1]	5.6[2]		35[3]	V
V_I	Input voltage range	Cell differential, VCx to VC(x + 1), (x = 1 to 8)	1.4		4.375	V
		Cell input VCx, x = 1 – 8			(9 – x) × 4.375 V	
		Cell input VC9	–1		1	
V_{IH}	Logic-level input, high	SCLK, SDATA, EEPROM, ZEDE	0.8 × V_{REG}			V
V_{IL}	Logic-level input, low				0.2 × V_{REG}	V
VSENSE(+)	Voltage applied at SENSE(±) pins		VSS – 1		VSS + 1	V
VSENSE(–)			–0.2		BAT	V
R_{VCX}	Recommended VCx nominal input resistance		50	100	1000	Ω
I_{REG}	Regulator current				10	mA
I_{CB}	Cell balancing current				50	mA
C_{VCX}	Recommended VCx nominal input filter capacitance				1	µF
R_{CPCKN}, R_{DPCKN}	Recommended isolation-pin input resistance			100		Ω
R_{LDRM_DET}	Pulldown for load-removal detection			50		kΩ
C_{VREG}	External 3.3-V REG capacitor		1			µF
	EEPROM number of writes				3	times
T_{OPR}	Operating temperature	Meeting all specification limits	–25		85	°C
T_{FUNC}	Functional temperature	Operational but may be out of spec limits, no damage to part	–40		100	°C
C_{CCAP}, C_{DCAP}	External capacitance on CCAP and DCAP pins[4]		0.1	1		µF
R_P	Serial communication interface pullup resistance[5]	SCLK, SDATA		2.2		kΩ

(1) The voltage rate of change at the BAT pin should be limited to a maximum of 1 V per µs in order to prevent unwanted device shutdown.
(2) Minimum voltage assumes 4-cell connection at 1.4 V/cell.
(3) Maximum voltage assumes 8-cell connection at 4.375 V/cell.
(4) C_{CCAP} and C_{DCAP} act as charge reservoirs for the CHG and DSG pins when driving large protection FETs. Minimum value is required for stability, independent of the CHG and DSG loading.
(5) Pullups for configuration of device during pack manufacturing. SCLK and SDATA should be pulled high or low in application.

[redacted]

ELECTRICAL CHARACTERISTICS (continued)

Vcell(n) = 1.4 to 4.375 for all cells, T_A = –25°C to 85ºC, BAT = 5.6 to 35 V; Typical values stated where T_A = 25°C and BAT = 28.8 V (unless otherwise noted)

If UV_REC = 0, the DSG FET is re-enabled when **all** the cell voltages increase back above the V_{UV} threshold level plus the hysteresis value; there is no time-delay part of the recovery. In this case, when UV_REC = 0 and under high load currents, the Vcell voltages could recover to >UV + hyst very quickly, re-enabling the FETs and allowing the high load current to persist. Care should be taken when using this UV_REC = 0 mode, as the power MOSFETs could oscillate rapidly.

CAUTION

Care should be taken to properly set overcurrent and cell undervoltage trip thresholds, because it is possible that a fully charged pack with a continuous high discharge load can oscillate in and out of the undervoltage condition. This may result in overheating of the cells or protection MOSFETs due to the potentially high-duty-cycle operation.

If UV_REC = 1, the DSG FET is re-enabled when **all** the cell voltages increase back above the V_{UV} threshold level plus the hysteresis value **AND** the load is removed.

Current is interrupted by opening the FETs, and at this point the cell voltages may quickly recover above the UV + hyst levels if the battery pack is not completely depleted. However, the external load may remain attached. When the external load is removed, the IC detects load removal and reconnects the DSG FET.

If UV_REC_DLY = 1 and any cell remains below the VUV threshold level plus the hysteresis for longer than 8 seconds, the device enters SHUTDOWN mode. If UV_REC_DLY = 0, the device does **not** enter the SHUTDOWN mode from the cell undervoltage fault condition.

The LDO is turned off during the SHUTDOWN mode. Insertion into a charger is required to recover from the SHUTDOWN mode.

Charger detection methods are discussed in later sections, such as *Application Information*.

Overcurrent in Discharge (OCD) Detection

The OCD detection feature senses an overload current by measuring the voltage across the sense resistor. When an overload condition is detected, both of the power FETS are disabled to prevent damage to the cells and FET components. Criteria for fault recovery depend on the state of the SOR (EEPROM bit). Overcurrent trip level (V_{OCD}) and blanking time delay (t_{OCD}) are programmable via EEPROM bits OCDT and OCDD to match individual application requirements.

Short Circuit in Discharge (SCD) Detection

The SCD detection function senses severe discharge current by measuring the voltage across the sense resistor. When a short circuit is detected, both of the power FETs are disabled to prevent damage to the cells and FET components. Criteria for fault recovery depend on the state of the of the SOR (EEPROM bit). Short-circuit trip level (V_{SCD}) and blanking time delay (t_{SCD}) are programmable via EEPROM bits SCDT and SCDD to match individual application requirements.

Load Removal Detection/OCD and SCD Fault Recovery

The part includes an internal high-impedance connection between the DPCKN and VSS pins of approximately 1.5 MΩ. An external load (for example power tool motor winding), if still connected to the pack terminals, would present a very low impedance relative to the high internal pulldown resistance.

NOTE

If the external load presents additional capacitance, then an external pulldown may be required between the DPCKN and VSS pins. This extra pulldown does not increase battery load current when the external load is removed.

If the DSG power FET is disabled after an overload or short-circuit event, the voltage at the DPCKN is

approximately equivalent to the BAT voltage potential while an external load (e.g., power tool motor) is present at the pack terminals. When the external load is removed, the high-value internal resistance pulls down the DPCKN potential to the internal VSS level. An internal comparator monitors the DPCKN terminal voltage during the protection state. When the DPCKN voltage falls to < V_{OPEN_LOAD} (approximately 2 V), the load removal is detected. Fault recovery from an OCD or SCD event depends on the state of the SOR EEPROM bit.

If SOR = 0, the FETs are re-enabled only after the external load removal is detected.

If SOR = 1, the FETs are re-enabled after the load is removed **and** a charger insertion is detected.

(Details of charger presence detection methods are discussed in later

- Because an open cell connection results in a floating VCx input, a UV or an OV fault may be detected before the open-cell fault due to their shorter fault filter times. Furthermore, the OV or UV condition may not be stable and the fault may recover during the open-cell check interval (i.e., the FETs may toggle). In all cases the open-cell fault is detected within the open-cell fault filter time and the FETs are shut off until the recovery conditions are satisfied. .
- The LDO shuts down following the detection of an open-cell fault, provided that a charger is not detected. When the pack is awakened following this, the open-cell fault is initially cleared (FETs closed) and must be re-evaluated over the filter time before the fault is again registered. Charger detection inhibits LDO shutdown; however, once the charger is disconnected, the LDO then shuts down, provided that the recovery conditions have not yet been satisfied.

Additional Fault Protection Functions

The brownout protection functionality is discussed in the *IC Internal Power Control* section of this document. Thermistor fault detection, charger/thermistor interface and control are discussed in the *Application Information* section.

IC INTERNAL POWER CONTROL

Power-On Reset/UVLO

On initial application of power to the BAT pin, the IC internal power supply rail begins to ramp up. The IC contains an internal undervoltage lockout (UVLO)/power-on reset (POR) circuit that prevents operation until the BAT voltage is sufficient to ensure predictable start-up and operation. All power for the IC internal circuitry is derived from the BAT pin. The UVLO/POR start-up threshold is specified in the parametric table as $V_{STARTUP}$. Once the BAT voltage has exceeded this level, the internal LDO regulator and control circuitry are enabled and continue to operate even if BAT falls below VSTARTUP. If the BAT pin falls below the operational range given under *Recommended Operating Conditions*, the device powers down.

On initial power up, the state of the output MOSFET drive pins (CHG and DSG) is indeterminate until the voltage on BAT reaches the $V_{STARTUP}$ threshold. No load should be applied during this period.

BAT Holdup/Brownout Protection Functionality

The BAT pin is used to power the IC internal circuitry, and should be supplied through a diode and held up with a capacitor(1) placed near the IC as shown in the application diagrams (see Figure 2 CELL BALANCING FUNCTION). The external diode prevents discharge of the IC power rail during external transients on the PACK(+) node.

This allows the bq77908 to maintain proper control of the pack and system during brownout conditions.

Brownout is defined as a situation during which the stack voltage collapses to a voltage below the minimum operating voltage of the IC (~5.6 V) for a short duration (~1 s). A typical application case is shown below. Additional examples are provided in the *Application Information* section later in this document.

If there are short-duration sags in the PACK(+) voltage (typically due to high load transients), the operating current for the IC is momentarily provided by the external capacitor. Assuming that there is no external load on the VREG (LDO output) pin, the IC draws approximately 50-µA average current from the capacitor. The holdup time before the IC goes into shutdown mode depends on the initial pack voltage. For a normal *low battery* initial condition using a 4-cell stack, the cells may be in the range of 3 V/cell or 12 V total for the pack voltage. If a load transient occurs at this point, and the pack voltage sags down to below the IC POR threshold, the voltage at the BAT pin is held above 5 V for slightly greater than one second using a 10-µF capacitor.

Waveforms typical of a load transient during low pack voltage conditions are shown as follows. In the first load transient, the PACK(+) rail momentarily collapses but the load is disconnected before the holdup time limit is exceeded. In the second load transient, the load is left on for a duration exceeding the holdup capability, so when the IC operating voltage reaches the gate-drive undervoltage limit, the external power FETs are disabled to disconnect the load.

(1) The capacitor should be sized according to the application requirements. A typical value would be 10 µF.

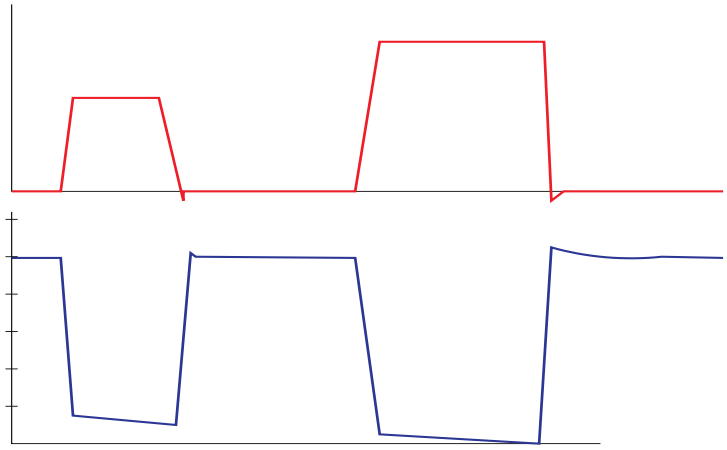


Figure 1. Load Transient Examples

BAT Voltage Peak Detection/Transient Suppression

The use of an external diode and holdup capacitor allows the IC to provide controlled operation during brownout conditions. However, when the battery pack is at a high level, a different issue must be considered.

During normal operation of power equipment, load transients may induce high-voltage pulses on the PACK(+) rail that exceed the steady-state dc voltage output of the battery pack. In some cases, these transient voltages can exceed the battery rail by several volts. The voltage at the BAT pin may be *held up* to these higher voltages for a longer duration because the diode prevents the capacitor from discharging back into the cell stack after the transient pulses decay. When the dc level of the battery pack voltage is near 35 Vdc, high-current load disconnection may cause transients that would exceed the absolute maximum ratings of the device.

The BAT pin incorporates an internal Zener clamp that dissipates any transient voltage at the BAT pin that exceeds 50 V. This internal clamp has very limited energy absorption ability. Therefore, additional external circuitry is required for transient suppression, depending on the application environment. A Zener or equivalent rated at <5 Ω and >3 W is recommended.

BAT Voltage Rate of Change

In addition to providing the holdup function, the filter components at the BAT pin serve to limit the maximum voltage rate of change. The voltage rate of change at the BAT pin should be limited to a maximum of 1 V per µs in order to prevent unwanted device shutdown.

Figure 2. Example 5-Cell, Series FET Configuration Schematic Using bq77908

Waveforms illustrative of load transients during high pack voltage conditions are shown here.

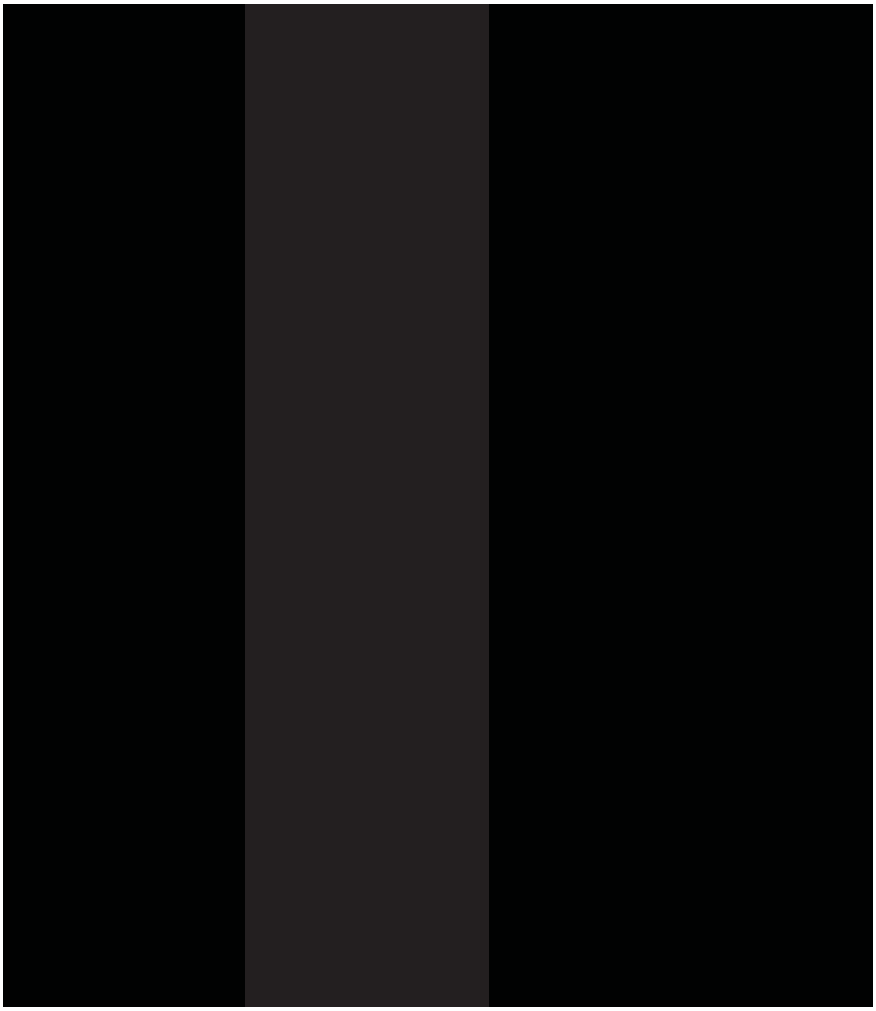


Figure 3. High-Voltage Load-Transient Waveforms

FET Gate Drive Control

As noted in the previous section, the BAT voltage at the IC pin is held up slightly longer than the external PACK(+) voltage using the external diode/capacitor to feed the BAT rail. Thus, if the BAT pin voltage at the IC sags, the external voltage sag will have exceeded the holdup time, and the IC is no longer able to operate for an extended period of time. At this point, the DSG and CHG gate drive outputs are actively driven low. The FET driver stages use two additional external capacitors (connected at the CCAP and DCAP pins) to maintain a local power reservoir dedicated to the gate drive circuitry, as the system (BAT) voltage may be collapsing during the time that the FETs are being turned off. The FETs are turned off when the voltage at the CCAP and/or DCAP pins falls below V_{GATE_UV}.

By turning off the FETs quickly, the system avoids the condition of insufficient gate drive due to low battery voltage. (If the FET gate drive is not high enough, the power components may not be in their linear operating region, and could overheat due to resistive losses at high load currents).

In the case of a system undervoltage condition, both FETs are disabled within 500 µs maximum; in all cases the FET fall time is less than fall time specified in the *Electrical Characteristics* section (FET Drive). During initial power up, once the UVLO threshold has been reached and the IC powers up fully, the rise time of the FET gate drive signal is also < 200 µs. This assumes a nominal gate capacitance of 50 nF as specified in the *Electrical Characteristics* tables.

NOTE

Selection of power FETs should consider the resistive losses that may occur during the undefined voltage range during power up from a complete collapse of battery voltage and holdup capacitance.

INITIAL POWER UP

Cell Connection

The IC design allows connection of the cells in any order. For EEPROM programming, only the VSS and BAT terminals must be connected to allow the device to communicate using the serial communication interface.

For normal pack assembly, the recommended connection procedure is to s o11..3 1.44 ny

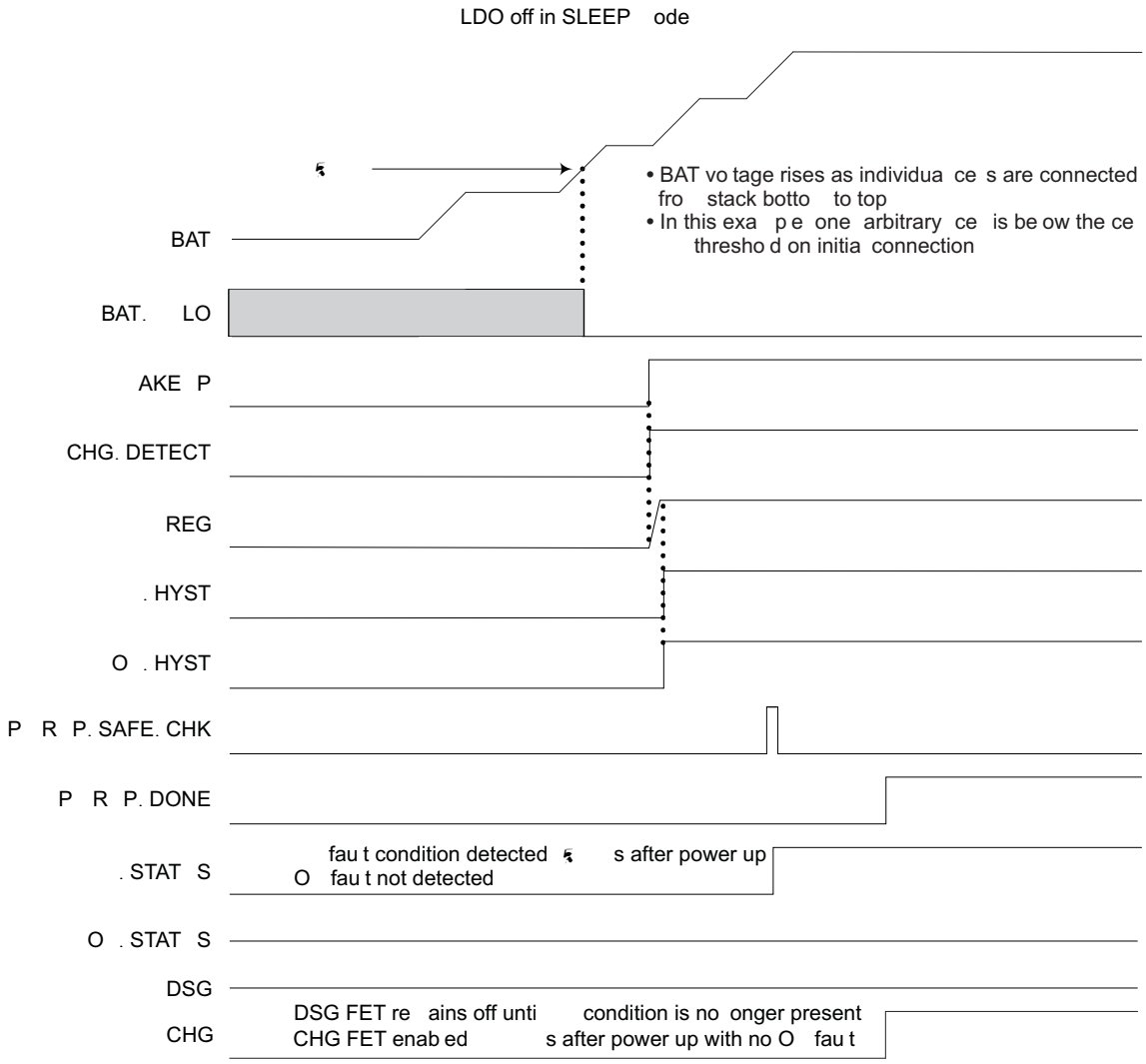


Figure 4. Initial Power Up With Single-Cell UV Fault

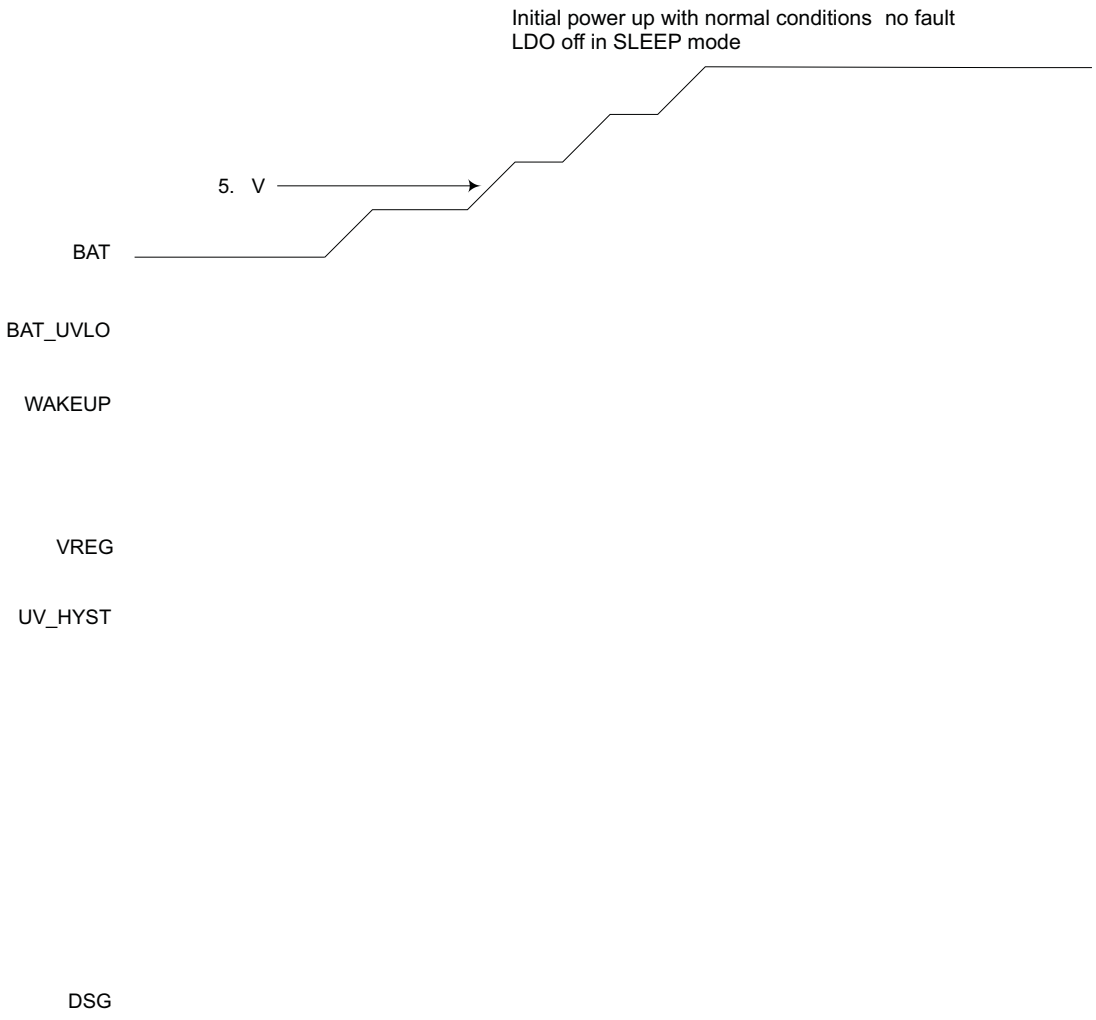


Figure 5. Initial Power Up With Normal Conditions (No Fault)

Table 2. Fault Detection, Action, and Recovery Condition Summary

Fault Condition	Fault Detection Parameter	Filter Time	Action Taken			EEPROM Config (if Applicable)	Recovery Conditions
			FET		MODE		
			CHG	DSG			
CELL OVERVOLTAGE	Any cell > V_{OV}	t_{OV}	OFF	ON	OV FAULT protection state	OV_TS_CTRL = 0	All cells < OV-hyst
					EXT CHGR DISABLE (TS pin→low)	OV_TS_CTRL = 1	
CELL UNDER-VOLTAGE	Any cell < V_{UV}	t_{UV}	OFF(1)(2)	OFF	UV FAULT protection state(3)	UV_REC bit = 0	1) Both FETS ON when all cells >UV + hyst (4) 2) CHG FET enabled immediately if charger detected
			OFF(5)(2)	OFF	UV FAULT protection state(3)	UV_REC bit = 1	1) Both FETs enabled when all cells >UV + hyst AND load removed 2) CHG FET enabled immediately if charger detected
PACK OVER-TEMPERATURE	Pack temperature out of range, $V_{TS} < V_{HOT}$	(1-2) × t_{THERM_CHECK}	OFF	OFF	OT FAULT protection state	TMP_REC bit = 0	V_{TS} > VHOT + hysteresis(6)
			OFF	OFF		TMP_REC bit = 1	V_{TS} > VHOT + hysteresis(6) and load removed
OVERCURRENT IN DISCHARGE	(V_{SC} – VSS) > V_{OCD}	t_{OCD}	OFF	OFF	OCD FAULT protection state	SOR bit = 0	Both ON when load removed
						SOR bit = 1	Both ON when load removed **AND** charger detected
SHORT CIRCUIT IN DISCHARGE	(V_{SC} – VSS) > V_{SCD}	t_{SCD}	OFF	OFF	SCD FAULT protection state	SOR bit = 0	Both ON when load removed
						SOR bit = 1	Both ON when load removed **AND** charger detected
SHORT CIRCUIT IN CHARGE	(V_{SS} – V_{SC}) > V_{SCC}	t_{SCC}	OFF	OFF	SCD FAULT protection state	N/A	Charger removed
OPEN THERMISTOR	V_{TS} > V_{TH_OPEN}	(1 to 2) × t_{THERM_CHECK}	OFF	OFF	OPEN THERM / UNDERTEMP protection state	N/A	V_{TS} < V_{TH_OPEN} – V_{TH_HYST}(6)
SHORTED THERMISTOR	V_{TS} < V_{TH_SHORT}	(1 to 2) × t_{THERM_CHECK}	OFF	OFF	SHUTDOWN (low-power state)		Charger detected and V_{TS} > V_{TH_SHORT} + V_{TH_HYST} (6)(7)(8)
OPEN CELL INPUT	Cell-to-pin impedance > R_{OPEN_CELL}	(1 to 2) × $t_{OPEN\_CELL\_CHECK}$	OFF	OFF	SHUTDOWN (low-power state)		Charger detected and open-cell condition absent > filter time(9)

(1) The LDO is turned off in the SHUTDOWN mode. *When the LDO is disabled, the CHG FET drive output is OFF by default, as all outputs of the device are disabled.*

(2) Regardless of EEPROM setting, if a battery pack in the UV protection state is inserted into a charger, (charger presence is detected), the CHG FET is turned ON to allow recharge of the pack. The DSG FET is turned on after UV recovery, as noted in Table 2 (conditions based on EEPROM setting).

(3) **a)** If UV_REC_DLY = 1 and any cell remains < UV + hyst for longer than 8 seconds, the device enters SHUTDOWN mode and requires insertion into charger to recover. If UV_REC_DLY = 0, the device does not enter SHUTDOWN mode from the UV FAULT protection state.

b) The LDO is turned off in the SHUTDOWN mode. *Charger insertion is required to recover from the SHUTDOWN mode.*

CAUTION: Care should be taken when using UV_REC = 0, because the power MOSFETs can oscillate when high load currents cause repeated cell UV conditions, which could result in overheating of cells or MOSFETs.

(4) If the UV_HYST_INH bit = 1, then the hysteresis threshold is inhibited and recovery occurs whenever the cells exceed the UV threshold (without hysteresis). If UV_HYST_INH = 1, the UV_REC bit should also be configured = 1. Otherwise, UV fault / recovery modes may chatter without hysteresis.

(5) If the LDO is left ON, the CHG FET is disabled when the fault condition occurs and re-enabled as soon as a charger is attached. The DSG FET does not re-enable until the UV condition is cleared (Vcell > Vuv + hysteresis).

(6) Recovery occurs within t_{THERM_CHECK} after recovery conditions are met.

(7) If a thermistor short occurs while charger is not detected, the FETs initially are re-enabled when charger is detected. If short condition is still present t_{THERM_CHECK} after charger detection and CHG_TMP_DIS = 0, the FETs re-open until the short condition is removed. If CHG_TMP_DIS = 1, the FETs remain enabled regardless of the short condition.

(8) If a charger is presently detected when the shorted thermistor fault is registered, the LDO does not shut off. Within 0 to 4 seconds after the short is removed, the FETs re-enable and the device recovers. However, if the charger is disconnected after the short is removed, but before the FETs are re-enabled, the device will shut down with the LDO off and require charger detection for recovery.

(9) If an open-cell fault occurs while a charger is detected, the device does not shut down. However, the device does shut down if the charger is later disconnected while the open-cell condition is still present. If the charger is disconnected after the open-cell condition is removed, the device recovers (i.e., FETs are re-enabled). Following a shutdown caused by an open-cell condition, the FETs initially re-enable when a charger is detected. However, if the open-cell condition is still present, the FETs re-open after the filter time.

CELL-BALANCING FUNCTION

The bq77908 implements an internal cell-balance control circuit and power FET structure. Because no CPU is available to manage a complex algorithm, a simple and robust hardware algorithm is implemented.

Overview

- Uses a separate comparator to check if cells have reached the balancing threshold to start balancing (i.e., does not use the OV trip comparator)
- Balance and charge can run concurrently – no charge-time extension
- Compare cell voltages – cell with highest voltage is bled off for time $t_{CELL\_BAL\_CHECK}$.
- Balancing current set by R_{VCX} – effect of balancing current on cell-to-cell voltage differential depends on cell capacity and $t_{CELL\_BAL\_CHECK}$.
- Cell-balancing options programmable – balancing threshold, when to balance (always, only during charge, or never), and how long to balance

Control Algorithm Description

- **Potential balancing action is updated (latched) every *minimum dwell time* $t_{CELL\_BAL\_CHECK}$**
  1. Action = bleed highest cell above cell-balance start voltage [Note: no hysteresis]
  2. Only one cell is bled at a time
  3. A minimum dwell time of 7.5 minutes equates to <0.5% capacity at 2 Ah and 50 mA balancing current)
  4. Calculation of potential balancing action is reset/inhibited when timer is expired to minimize current draw on the cell stack in case of charger termination
- **Balancing action is suppressed if any of the following are true:**
  1. Highest cell voltage < cell-balance start voltage
  2. Balance time has expired (when configuring balancing time via)
  3. Charger is not detected when configured to balance only in charger
  4. Cell-voltage measurement is active
- **Balancing action inhibited during cell measurement**
  1. Measure for 50 ms, balance for 200 ms per each 250-ms cycle (80% utilization)
  2. Cell measurements are *frozen* when balancing output is asserted
  3. OV, UV protection delay time is constrained to be 500 ms or longer
  4. Cell balancing is suspended when an OV/UV condition is present and is being timed for fault determination (maximum time for OV = 2.25 s; UV = 32 s).
  5. Cell balancing is resumed after the fault checking has been completed, whether faults are cleared or latched
- **Recommended system design – charger continues to *top up* the pack when connected**
  1. This may not be the case with certain chargers which shut down once charge current taper limit is reached.
  2. Timer should be enabled to prevent balancing from discharging the pack (maximum balance time is limited).
  3. Timer value is selectable via EEPROM (1, 2, 4, or 8 hours).
  4. Timer value of 4 hours and 50 mA balancing current is typically sufficient to balance a pack from fully charged to empty.

External Connections for Cell Balancing

Multiple options are supported for different cell-balancing requirements. These are summarized in the following sections. These diagrams do NOT show the other external connections such as BAT, TS, CHGST, or power FET arrangements. See subsequent sections for more complete application diagrams showing all external connections.

Normal Configuration – Balancing With Internal FETs

The basic cell balancing-configuration is shown here. Balance current must be limited using external resistance. Resistive component sizes limit the balance current

Figure 7. Typical Low-Current Balancing Configuration (~2 mA)

High-Current (Approximately 100-mA to 150-mA) Balancing Using External Power FETs

In this example, external PMOS devices are driven from the IC internal NMOS balance FETs. Current limiting is controlled by the external resistors and is on the order of 100 mA to 150 mA, depending on cell voltage. Contact TI for application example.

APPLICATION INFORMATION

Internal Voltage Regulator

The bq77908 has an integrated low-power linear regulator that provides power to both internal and any optional user-defined external circuitry. The input for the regulator is derived from the BAT terminals. VREG nominal output value is 3.3 V and is also internally current-limited. The minimum output capacitance for stable operation is 1 µF.

The regulator is disabled during the SHUTDOWN mode. When the regulator circuit is disabled (including the time during the power-up sequence of the IC) the DSG and CHG FETs are driven OFF.

Charger Detection and Wake-Up

The bq77908 contains a mechanism to detect the presence of an external charger and allow the device to wake up from the low-power shutdown mode when the LDO has been turned off. A low-power wake-up circuit monitors the CHGST pin to determine the charger connection event.

CHGST Pin Detection

Because the bq77908 is designed to use low-side NMOS FETs to control current flow to / from the battery pack, charger presence detection cannot be determined simply by checking the positive terminal voltage. To allow detection of the presence / absence of an external charger under any operating conditions, the bq77908 implements a charger sense pin, designated CHGST. If a voltage of greater than (nominally) 0.5 V is detected at the CHGST pin, the bq77908 logic assumes that a charger has been connected. *The voltage monitoring circuit at the CHGST pin is an always-on subsystem within the chip. When the proper voltage appears at the CHGST pin, the IC wakes up from the SHUTDOWN mode after a charger is connected.* If fault conditions exist, the part

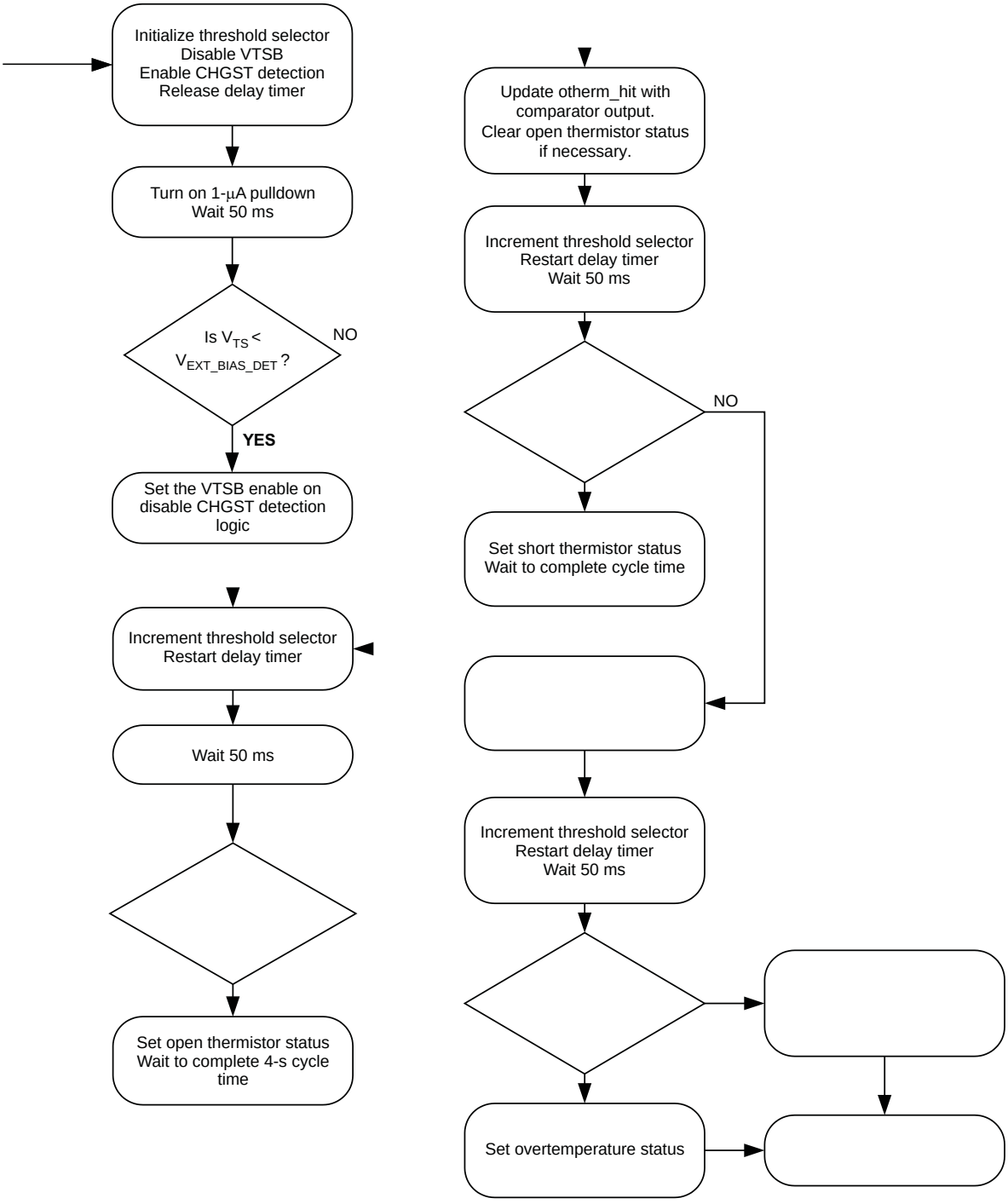
A negative-temperature-coefficient thermistor in the topology shown in Figure 9 is assumed. With this arrangement, the *voltage* at the TS will be lower for high temperature, and higher for low temperature. If the voltage measured at the TS pin is below the V_{HOT} threshold, a pack overtemperature condition is detected.

In the extreme fault cases, an open (disconnected) thermistor indicates a voltage at the TS pin equivalent to the VREG pullup voltage, and a shorted thermistor indicates a voltage close to 0 (VSS). An open-thermistor fault recovers within the fault filter time following removal of the open condition. Shorted-thermistor detection places the device into the low-power SHUTDOWN mode, requiring re-insertion into a charger for wakeup.

External Bias Supply Detection

During the time period in which the bq77908 checks the thermistor status, a weak (nominal 1-µA) current is applied from the TS pin to VSS. If V_TS > V_EXT_PU, then the IC operates as if an external supply is present and does not enable the VTSB internal supply. A sequence of operations is performed to determine the existence of shorted thermistor, open thermistor, or pack overtemperature faults as listed in the following section.

Temperature Measurement / Fault Detection Logic Flow Diagram



Battery Pack / Charger Shared-Thermistor Functionality

The pulsing of the VTSB pin is enabled ONLY when the IC determines that there is no external supply (e.g., from the charger) already driving the thermistor. This allows a single thermistor to be used by both the bq77908 and the external charger to measure pack temperature. This can also be used as a method of charger presence detection in case a dedicated charger-detect pin is not implemented in the end-equipment pack design.

By connecting the CHGST pin to the TS pin on the battery-pack internal circuit board, a three-terminal battery-pack design with (+), (–) and (T) (thermistor) contacts is compatible with the charger-detection mechanism of the bq77908. Because the external charger normally applies a bias voltage to the TS pin from an external source, there is a voltage present on the CHGST pin whenever the pack is inserted into the charger.

NOTE

V_{TH_xxx} (thresholds) are ratiometric

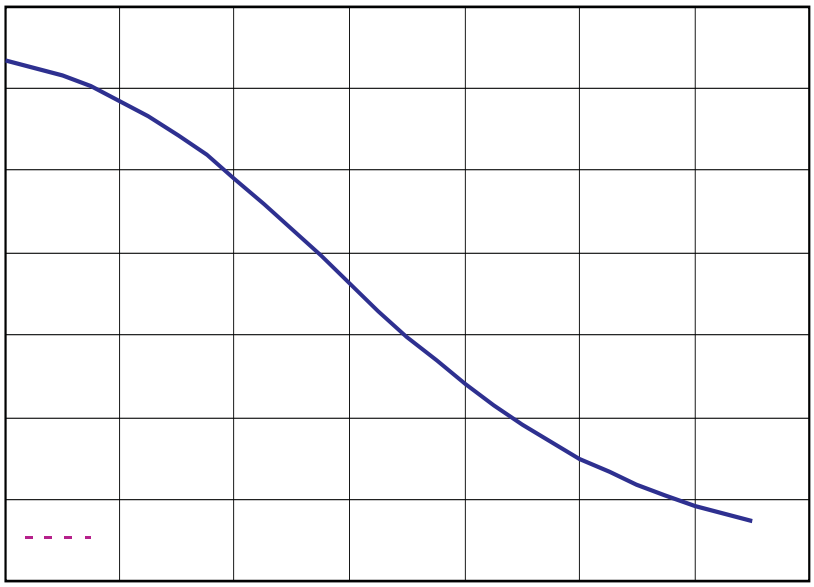


Figure 10. Typical Thermistor Response and Protection Thresholds (VTSB = 3.3 V, Pullup = 10 kΩ)

The bq77908 limits pack operation in the case of an overtemperature, undertemperature, open, or shorted thermistor. An overtemperature fault opens the protection FETs only; a shorted-thermistor fault also puts the device into low-power / fault protection mode. Due to the range of resistance values available with a typical thermistor, an undertemperature fault is indistinguishable from an open-thermistor fault and has the same protection mechanism (enter protection state, but device stays awake). The V_{TH_OPEN}, V_{HOT}, and V_{TH_SHORT} thresholds are ratiometric to the

Additionally, if UV_REC_DLY = 1 and all the cell voltages remain $<V_{UV}$ + hysteresis for more than 8 seconds, then the bq77908 enters the SHUTDOWN mode.

If UV_REC_DLY = 0, the part does not enter SHUTDOWN mode from a UV fault condition.

Once in the SHUTDOWN mode, insertion into a charger is required to exit the SHUTDOWN mode.

When in the SHUTDOWN mode, the LDO turns off.

This recovery criterion is described in the fault summary of Table 2 and the *Cell Undervoltage Detection and Recovery* section.

Pack/System Connection Arrangements

The architecture and fault detection/recovery logic allows the system developer to implement multiple types of battery-pack topologies using the bq77908. A few basic application cases are illustrated here; however, others are also possible as long as the external connections and host-equipment interface are compatible with the fault detection and recovery signaling methods.

Notes regarding the application schematics:

- A five-cell configuration is shown for simplicity. All unused cell inputs (not shown) are tied to the PACK(+) positive terminal.
- For configurations which do not implement a CHG FET, it is assumed that the CHGST pin (in bq77908) is pulled up inside the charger equipment (nominally V_{CHG_DET1}).
- Gate-source pulldown resistances are recommended for the power FETs to prevent parasitic turnon when the bq77908 is in shutdown mode. This may have a slight impact on operating current when FETs are enabled; however, very large resistances (~ 5 MΩ) may be used to minimize this effect.
- Series resistance between the CHG/DSG pins and FET gates should be sized to assure quick turnoff of the FETs used.
- High-current (pack discharge/charge) flow paths are indicated by wide traces; low-current signal paths use narrow traces in the following schematics.

Series CHG and DSG FET Configuration

Use of a separate contact (i.e., CHGST) for charger detection is preferred if the cell-balancing function is used. This is to allow balancing to occur only while charging. Otherwise, if the part cannot detect the presence of a charger, balancing must be enabled to occur at all times or not at all. The CHGST pin should be protected from possible negative voltage inputs which may occur if connected to a charger with the CHG FET open.

Note that in shutdown with the LDO off, the specified shutdown currents require that the voltage at CPCKN with respect to VSS is controlled. In the parallel FET case, CPCKN is clamped through the body diode of the charge FET. In the series FET case, external circuitry is required to keep CPCKN from floating. Contact TI for recommended application circuits.

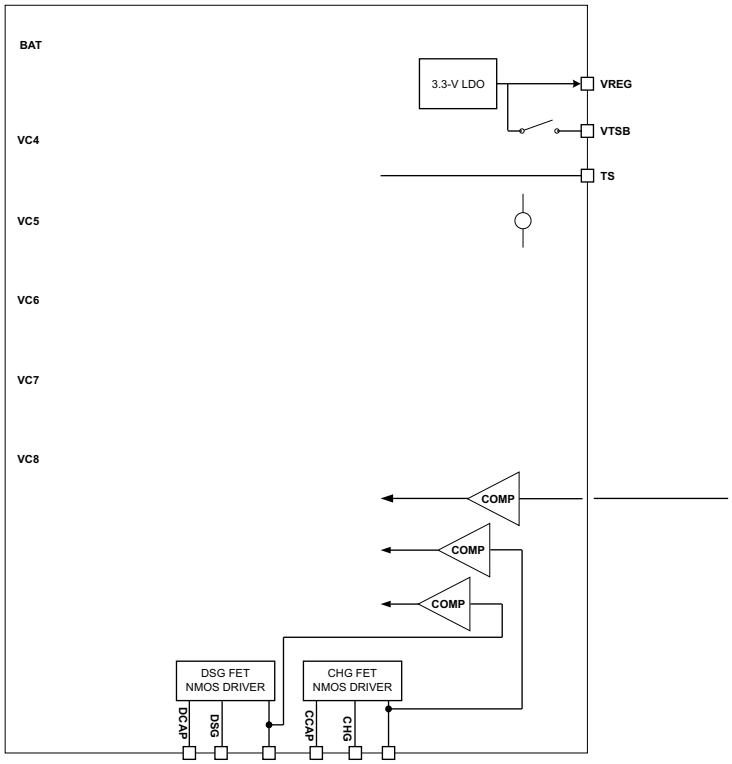
If current is able to flow from CPCKN through the charge FET (e.g., through the body diode), the resistor R_{LDRM_DET} is required to discharge DPCKN for proper detection of load removal. When the FETs are open and a load is present, the PACK– terminal and consequently DPCKN is pulled up to PACK+. When the load is removed, DPCKN is discharged through R_{LDRM_DET}. Detection of load removal occurs when the voltage at DPCKN (referenced to VSS) falls below 2 V (typical).

Figure 11. Example Series FET Configuration Using the CHGST Pin

Separate CHG(–) and DSG(–) Return Paths With Both FETs

In this configuration, if the charge current is typically much lower than the discharge current, a lower-cost component can be used for the charge control FET than in the series configuration previously shown.

Use of a separate contact (CHGST pin) is preferred if the cell balancing function is used. T44.01getoTd (separate)T



DSG(–)

CHG(–)

Separate CHG(–) and DSG(–) Return Paths With DSG FET Only

In this configuration, no charge-control FET is implemented. As a result, the bq77908 is unable to interrupt charge current when an overvoltage condition occurs. The suggested method to stop the charger in an overvoltage event is to use the thermistor signal to indicate a fault condition. The system should configure the OV_TS_CTRL bit high, so that when an overvoltage occurs, the charger detects that an overtemperature condition has occurred, and halts charging. (See the *OV_TS_CTRL (EEPROM Bit) Interface* section.)

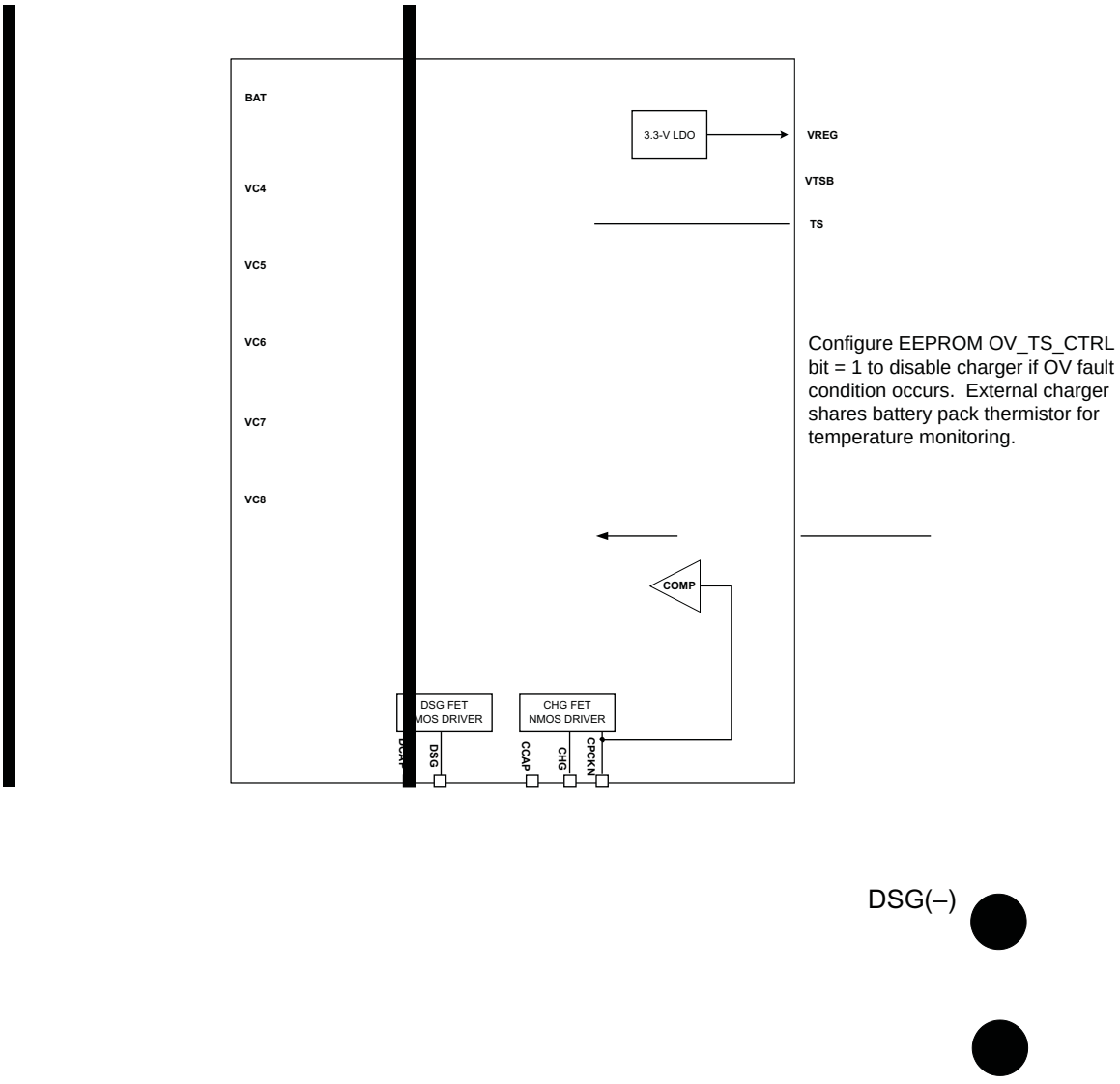


Figure 13. Example Split Power Path With No Charge FET Using the CHGST Pin

4 to 8 Series Cell Configuration

All cell input pins of the device are used for a 8-cell battery pack application. The bq77908 supports pack configurations ranging from 4 to 8 series cells. If fewer than 8 cells are used in an application, all unused VCx cell input pins should be tied together and pulled up to the most-positive cell input. Pullup resistance value is not critical; a 100 Ω–1000-Ω value is suggested. An example for a 5-cell application is shown here. Cell configuration is programmable by EEPROM, using the SYS_CFG register bits CNF[2:0].

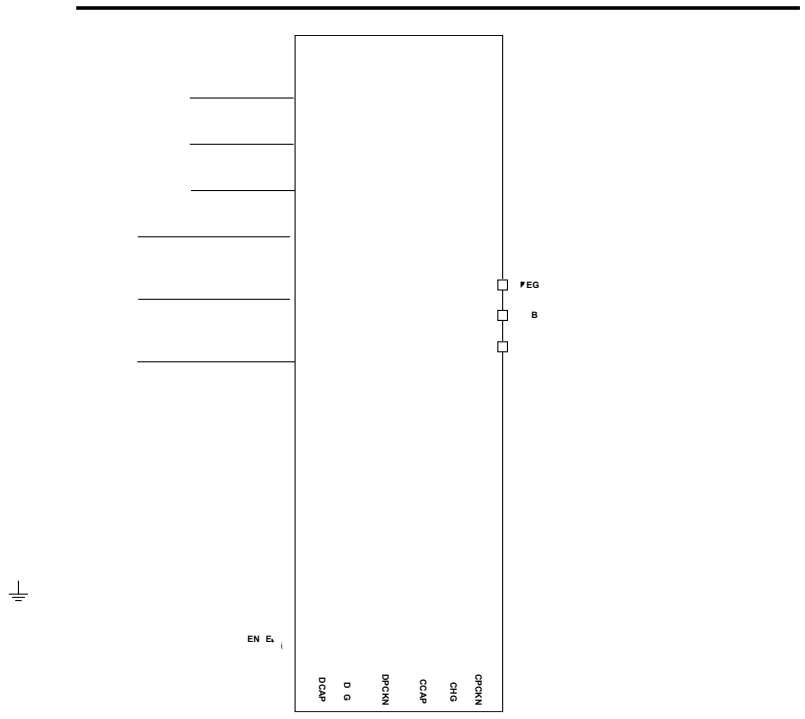


Figure 15. Unused VCELLx Pin Configuration

Delay Time Zero

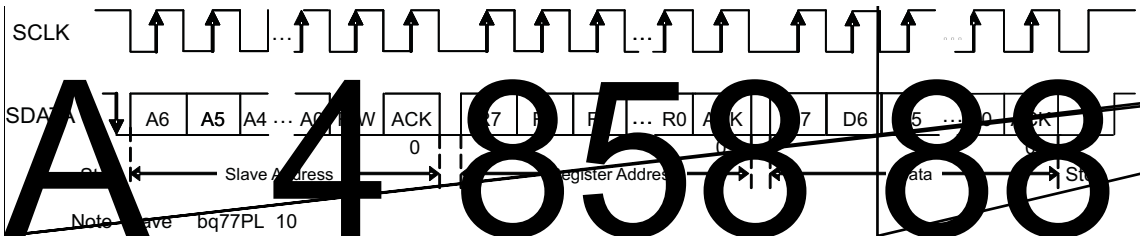
The ZEDE pin enables the EEPROM-programmed detection-delay times when connected to VSS (normal operation). A strong pulldown to VSS is recommended to prevent external circuit noise from causing ZEDE to go high. The detection delay time is set to minimum when this pin is connected to VREG. This is used in battery manufacturing test. When programming the EEPROM, this pin should to be connected to VREG to enable the serial communication interface.

Ship-Mode Equivalent Functionality

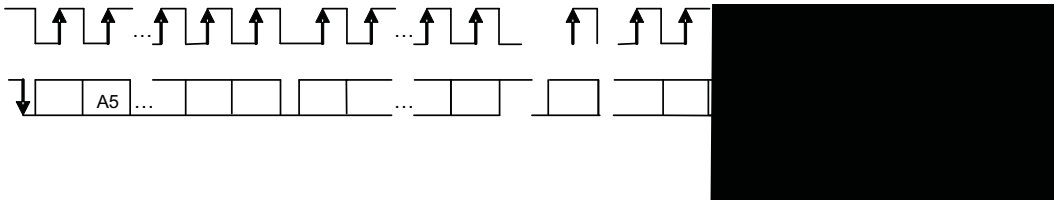
Because the BMU is designed for standalone-mode operation, it does not incorporate a programmable-entry *ship mode*, which is intended for long-term storage of a battery pack after initial assembly.

The ty

Bus Write Command to bq77908



Bus Read Command from bq77908 (Protocol A)



Bus Read Command from bq77908 (Protocol B)

REGISTER SET AND PROGRAMMING

Memory Map

The bq77908 has 10 programmable EEPROM registers and one RAM register used to access / write the EEPROM data. The EEPROM bits are used to program the various threshold, delay, configuration, and recovery control settings. The address, register names, and individual control bit names are shown in the following table. Descriptions of each individual register and available programming options are provided in the subsequent sections. Bits labeled RSVDx (gray) are unused and left for future options.

WARNING

For RSVD1, SERIOUS SAFETY RISK MAY APPLY to battery monitoring features of BQ77910DBT, BQ77910DBTR, BQ77908DBT, and BQ77908DBTR if RSVD1 is not set to 0. Some uses of these components could present serious risk of fire, explosion, battery rupture, serious injury, or death if RSVD1 is not set to 0.

721.52 0 TTj 2,ns.regis0 Td (seeInstrum Td (ris Td (set)Tj Incorpoz 0

Address	Register Name	7	6	5	4	3	2	1	0
0x00	EE_PROG(1)								VGOOD(1)
0x01	SYS_CFG	CNF2	CNF1	CNF0	CHG_TMP_DIS	TMPEN	OT_REC	RSVD1	SOR
0x02	OV_CFG1	RSVD2	RSVD3	OVT5	OVT4	OVT3	OVT2	OVT1	OVT0
0x03	OV_CFG2	OV_TS_CTRL	OVH2	OVH1	OVH0	RSVD4	OVD2	OVD1	OVD0
0x04	UV_CFG1	UV_HYST_INH	RSVD6	RSVD7	RSVD8	UVT3	UVT2	UVT1	UVT0
0x05	UV_CFG2	UV_REC	UV_REC_DLY	UVH1	UVH0	RSVD10	UVD2	UVD1	UVD0
0x06	OCD_DELAY	RSVD11	RSVD12	RSVD13	OCDD4	OCDD3	OCDD2	OCDD1	OCDD0
0x07	SCD_DELAY	RSVD14	RSVD15	ISNS_RNG	SCDD_RNG	SCDD3	SCDD2	SCDD1	SCDD0
0x08	OCD_SCD_TRIP	SCDT3	SCDT2	SCDT1	SCDT0	OCDT3	OCDT2	OCDT1	OCDT0
0x09	SCC_CFG	SCCD3	SCCD2	SCCD1	SCCD0	SCCT3	SCCT2	SCCT1	SCCT0
0x0A	CELL_BAL_CFG	CB_EN1	CB_EN0	CBT1	CBT0	CBV3	CBV2	CBV1	CBV0

(1) Read-only bit.

System Configuration (SYS_CFG, Address 0x01)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	CNF2	CNF1	CNF0	CHG_TMP_DIS(1)(2)	TMPEN	OT_REC	RSVD1(3)	SOR
If 0	8 possible settings to determine pack configuration (4 to 8 cells); see following table			Default value – thermal protection active in all modes	Disable temperature sensing	Recover from OT fault when pack has cooled below limit (incl. hysteresis)	This bit must be set to 0.	Recover from OCD/SCD when load removed
If 1				Thermal protection enabled only when no charger detected; thermal protection DISABLED when CHARGER PRESENT	Enable temperature sensing	Recover from OT fault when pack has cooled below limit (incl. hysteresis) *AND LOAD REMOVED*		Recover from OCD/SCD when load removed and charger attached

(1) If CHG_TMP_DIS = 1, all thermal faults are cleared when a pack is inserted into a charger.
(2) CHG_TMP_DIS takes priority over OT_REC. If both are = 1, then thermal faults are cleared whenever inserted into a charger.
(3) SERIOUS SAFETY RISK MAY APPLY to battery monitoring features of BQ77910DBT, BQ77910DBTR, BQ77908DBT, and BQ77908DBTR if RSVD1 is not set to 0. Some uses of these components could present serious risk of fire, explosion, battery rupture, serious injury, or ion, injury, ion nitsering0.07 0 Td (all)Tj 10.4 0 Td (therma 100 Tz 0 0 0 rg6rg 59.6 5110 0 0 rg 144 Td (to)Tj,)Tj 52.4bled

or bit.

OV Detection Configuration #1 (OV_CFG1, Address 0x02)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	RSVD2	RSVD3	OVT5	OVT4	OVT3	OVT2	OVT1	OVT0
If 0	NOT USED	NOT USED	Overvoltage trip threshold (64 possible values); see following table.					
If 1	NOT USED	NOT USED						

Programmable Overvoltage Threshold Settings

Using the 5 bits OVT[5:0], up to 64 possible set points for overvoltage trip are possible, as shown. OVT setting is chosen to match the cell type and application requirements.

OVT[5:0]	OV Trip (Volts)		OVT[5:0]	OV Trip (Volts)
0x00	2.800		0x20	3.600
0x01	2.825		0x21	3.625
0x02	2.850		0x22	3.650
0x03	2.875		0x23	3.675
0x04	2.900		0x24	3.700
0x05	2.925		0x25	3.725
0x06	2.950		0x26	3.750
0x07	2.975		0x27	3.775
0x08	3.000		0x28	3.800
0x09	3.025		0x29	3.825
0x0A	3.050		0x2A	3.850
0x0B	3.075		0x2B	3.875
0x0C	3.100		0x2C	3.900
0x0D	3.125		0x2D	3.925
0x0E	3.150		0x2E	3.950
0x0F	3.175		0x2F	3.975
0x10	3.200		0x30	4.000
0x11	3.225		0x31	4.025
0x12	3.250		0x32	4.050
0x13	3.275		0x33	4.075
0x14	3.300		0x34	4.100
0x15	3.325		0x35	4.125
0x16	3.350		0x36	4.150
0x17	3.375		0x37	4.175
0x18	3.400		0x38	4.200
0x19	3.425		0x39	4.225
0x1A	3.450		0x3A	4.250
0x1B	3.475		0x3B	4.275
0x1C	3.500		0x3C	4.300
0x1D	3.525		0x3D	4.325
0x1E	3.550		0x3E	4.350
0x1F	3.575		0x3F	4.375

OV Detection Configuration #2 (OV_CFG2, Address 0x03)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	OV_TS_CTRL	OVH2	OVH1	OVH0	RSVD4	OVD2	OVD1	OVD0
If 0	Do not use TS line for external charger control	8 possible settings to control OV hysteresis (see following table)			NOT USED	8 possible settings to control OV sense delay (see following table)		
If 1	Use TS line for external charger control (if OV event, pull TS = low)				NOT USED			

OV Hysteresis Settings

Eight possible hysteresis settings are selectable using the bits OVH[2:0] as shown in the following table.

OVH[2:0]	OV Hysteresis (mV)
000	300
001	250
010	200
011	150
100	100
101	50
110	25
111	0

OV Delay Settings

Eight possible OV trip time delay settings are selectable using the bits OVD[2:0]

OVH[2:0]	OV Delay (Seconds)
000	0.50
001	0.75
010	1.00
011	1.25
100	1.50
101	1.75
110	2.00
111	2.25

UV Detection Configuration #1 (UV_CFG1, Address 0x04)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	UV_HYST_INH	RSVD6	RSVD7	RSVD8	UVT3	UVT2	UVT1	UVT0
If 0	Use hysteresis threshold to allow recovery after UV condition (DEFAULT)	NOT USED	NOT USED	NOT USED	Set one of 16 possible values; see following table.			
If 1	Do not use (inhibit) hysteresis threshold to allow recovery from UV threshold	NOT USED	NOT USED	NOT USED				

Undervoltage Trip Threshold Settings

The specific undervoltage trip point required by the cell type and application can be set using the UVT[3:0] bits as shown here:

UVT[3:0]	UV Trip Level (Volts)		UVT[3:0]	UV Trip Level (Volts)
0000	1.4		1000	2.2
0001	1.5		1001	2.3
0010	1.6		1010	2.4
0011	1.7		1011	2.5
0100	1.8		1100	2.6
0101	1.9		1101	2.7
0110	2.0		1110	2.8
0111	2.1		1111	2.9

UV Detection Configuration #2 (UV_CFG2, Address 0x05)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	UV_REC	UV_REC_DLY	UVH1	UVH0	RSVD10	UVD2	UVD1	UVD0
If 0	Recover from UV fault when all cell voltages increase above V_{UV} threshold+hyst. CHG FET enabled immediately if charger detected	Part does NOT enter SHUTDOWN mode from the UV fault state	1 of 4 possible values, see		NOT USED	1 of 8 possible values, binary spacing, see		
If 1	Do not recover from UV fault when all cell voltages increase above V_{UV} threshold+hyst. CHG FET enabled immediately if charger detected	Part enters SHUTDOWN mode from the UV fault state						

Discharge Overcurrent/Short-Circuit Trip Levels (OCD_SCD_TRIP, Address 0x08)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	SCDT3	SCDT2	SCDT1	SCDT0	OCDT3	OCDT2	OCDT1	OCDT0
If 0	One of 16 possible SC trip settings (sense resistor voltage), see following table.				One of 16 possible OC trip settings (sense resistor voltage), see following table.			
If 1								

NOTE: SCD and OCD trip levels are controlled by current-sense gain-control bit ISNS_RNG located in register 0x07. Trip levels measured at SENSE– are referenced to SENSE+.

Discharge Short-Circuit Trip-Level Settings (Sense-Resistor Voltage)

SCDT[3:0]	Discharge Short-Circuit Trip Level, mV at SENSE (–), With ISNS_RNG = 0	Discharge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	40	200
0001	50	250
0010	60	300
0011	70	350
0100	80	400
0101	90	450
0110	100	500
0111	110	550
1000	120	600
1001	130	650
1010	140	700
1011	150	750
1100	160	800
1101	170	850
1110	180	900
1111	190	950

Discharge Overcurrent Trip-Level Settings (Sense-Resistor Voltage)

OCDT[3:0]	Discharge Overcurrent Trip Level, mV at SENSE(–), With ISNS_RNG = 0	Discharge Overcurrent Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	25	125
0001	30	150
0010	35	175
0011	40	200
0100	45	225
0101	50	250
0110	55	275
0111	60	300
1000	65	325
1001	70	350
1010	75	375
1011	80	400
1100	85	425
1101	90	450
1110	95	475
1111	100	500

Charge Short-Circuit Threshold and Delay Settings (SCC_CFG, Address 0x09)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	SCCD3	SCCD2	SCCD1	SCCD0	SCCT3	SCCT2	SCCT1	SCCT0
If 0	One of 16 possible charger short-circuit sensing delay settings, see following table.				One of 16 possible charger short-circuit sensing threshold settings (sense resistor voltage), see following table.			
If 1								

NOTE: SCC trip-level range is controlled by current-sense gain-control bit ISNS_RNG, located in register 0x07. Trip levels measured at SENSE– are referenced to SENSE+.

Charge Short-Circuit Delay-Time Settings

SCCD[3:0]	Charge Short-Circuit Delay (µs)		SCCD[3:0]	Charge Short-Circuit Delay (µs)
0000	60		1000	540
0001	120		1001	600
0010	180		1010	660
0011	240		1011	720
0100	300		1100	780
0101	360		1101	840
0110	420		1110	900
0111	480		1111	960

Charge Short-Circuit Trip-Level Settings

SCCT[3:0]	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 0	Charge Short-Circuit Trip Level, mV at SENSE(–), With ISNS_RNG = 1
0000	–10	–50
0001	–15	–75
0010	–20	–100
0011	–25	–125
0100	–30	–150
0101	–35	–175
0110	–40	–200
0111	–45	–225
1000	–50	–250
1001	–55	–275
1010	–60	–300
1011	–65	–325
1100	–70	–350
1101	–75	–375
1110	–80	–400
1111	–85	–425

CBV[3:0]	Cell Voltage
1110	2.5
1111	2.4

EEPROM Control Register (EEPROM, Address 0x0B)

Bit Number	7	6	5	4	3	2	1	0
Bit Name	EEPROM7	EEPROM6	EEPROM5	EEPROM4	EEPROM3	EEPROM2	EEPROM1	EEPROM0

These bits enable data write to EEPROM locations (0x01–0x0A) when written with data 0100 0001 (0x41). Pre-read of EEPROM data is available by setting these bits with 0110-0010 (0x62). Default is 0000-0000 (0x00).

EEPROM Write Sequence

EEPROM is written by I^2C command. When ZEDE = H, the SCLK and SDATA lines are enabled to allow I^2C communication.

	(MSB)			I^2C Address +R/W bit				(LSB)
	(MSB)			I^2C Address			(LSB)	
Write	0	0	1	0	0	0	0	0
Read								1

The bq77908 has integrated configuration EEPROM for OV, UV, OCD, SCD, and SCC thresholds and delays. The appropriate configuration data is programmed to the configuration registers and then 0x41 is sent to the EEPROM register to enable programming. By driving the EEPROM pin (set high and then low), the data is written to the EEPROM. The recommended voltage at BAT for EEPROM writing is >7 V. A flowchart showing the EEPROM write / check sequence is shown in Figure 16.

Parity Check

The bq77908 uses EEPROM for storage of protection thresholds and delay times as previously described. Additional EEPROM is also used to store internal trimming data. For safety reasons, the bq77908 uses a column-parity error-checking scheme. If the column-parity bit is changed from the written data, both DSG and CHG FETs are forced OFF as a fail-safe mechanism.

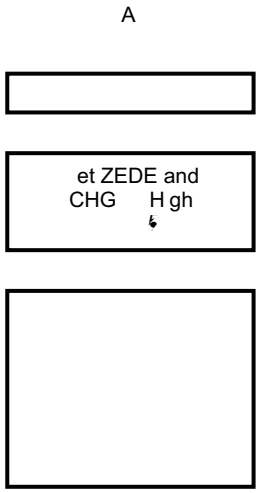


Figure 16. EEPROM Programming Flow Diagram

REVISION HISTORY

Changes from Revision B (May 2011) to Revision C **Page**

- Deleted $I_{SHUTDOWN\_1}$ row from Electrical Characteristics table 7
- Changed text and table of *Power Modes* section 10
- Deleted text from next-to-last paragraph of *Cell Undervoltage Detection and Recovery* section 12
- Changed bulleted list items in the *Open Cell Connection* section 14
- Changed text in Figure 5 20
- Changed last two rows in Table 2 21
- Deleted text from last paragraph of *Internal Voltage Regulator* section 25
- Changed text in Figure 8 26
- Changed text in next-to-last paragraph of UV Fault – Secondary Delay Function section 31
- Changed numbered list in *Ship-Mode Equivalent Functionality*section 37
- Changed memory map and system configuration tables 39
- 39

Changes from Revision C (November 2011) to Revision D **Page**

- Added RSVD1 WARNING 39

Changes from Revision A (April 2011) to Revision B **Page**

- Changed I_{CC} test condition BAT from 36 V to 28.8 V 7
- Changed values in Electrical Characteristics for t_f with test condition BAT = 6.4 7

Changes from Revision Original (April 2011) to Revision A **Page**

- Deleted a Features bullet under Low Supply Current 1
- Changed maximum ΔV_{OV} threshold accuracies from 40 mV to 50 mV and from 65 mV to 75 mV 8
- Corrected second paragraph in FET Gate Drive Control section 17

PACKAGING INFORMATION

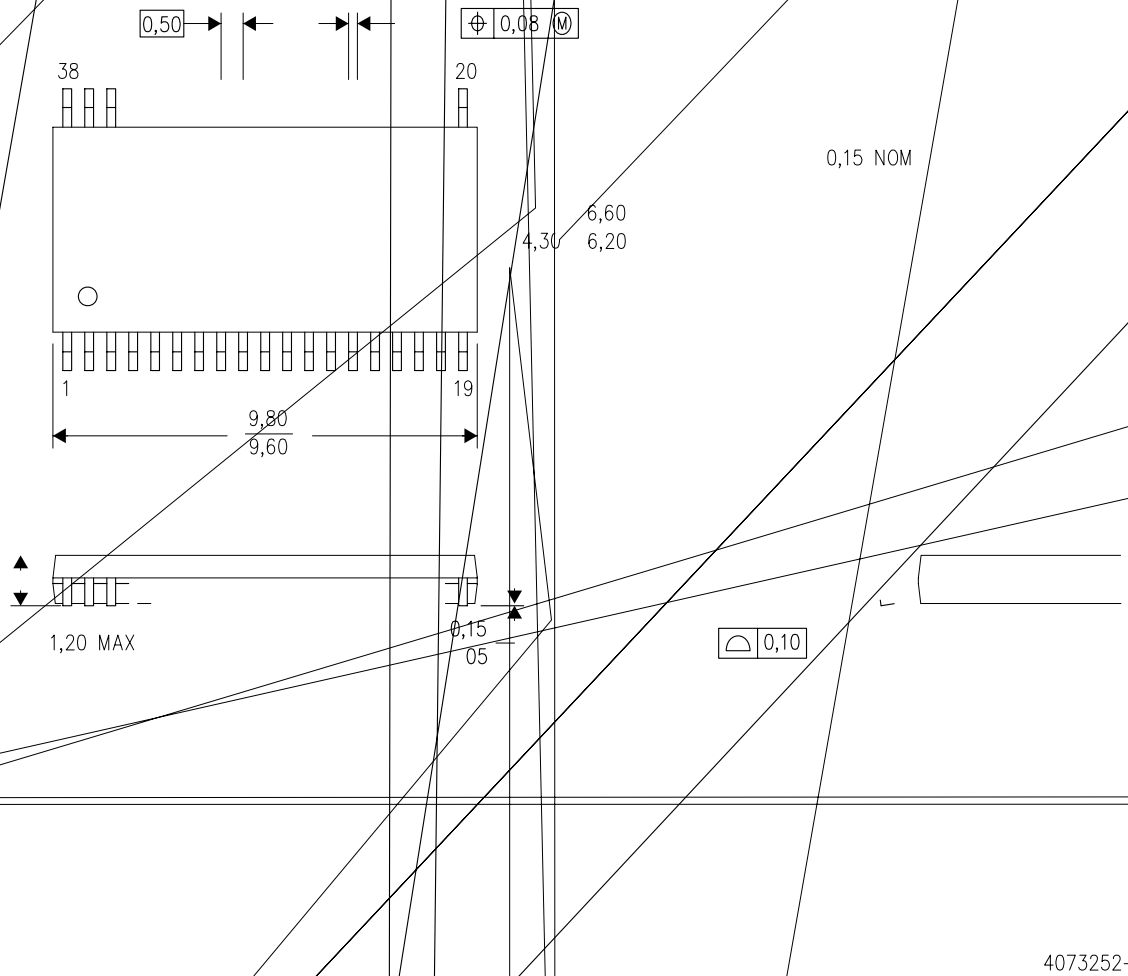
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ77908DBT	OBSOLETE	TSSOP	DBT	38		TBD	Call TI	Call TI	
BQ77908DBTR	OBSOLETE	TSSOP	DBT	38		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



cr ASME Y14.5M–1994.

B. This drawing is subject to change without notice.
C. Body dimensions do not include mo
D. Falls within JEDEC MO–153.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265