THREE AND FOUR CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION AFE

FEATURES

- **2-, 3-, or 4-Cell Series Protection Control**
- **Can Directly Interface With the bq2084 Gas Gauges**
- **Provides Individual Cell Voltages and Battery Voltage to Battery Management Host**
- **Integrated Cell Balancing Drive**
- **I^2C Compatible User Interface Allows Access to Battery Information**
- **Programmable Threshold and Delay for Over Load and Short Circuit During Charge and Discharge**
- **System Alert Interrupt Output**
- **Host Control Can Initiate Sleep Power Mode and Ship Mode**
- **Integrated 3.3-V, 25-mA LDO**
- **Supply Voltage Range From 4.5 V to 25 V**
- **Low Supply Current of 60-µA Typical**

APPLICATIONS

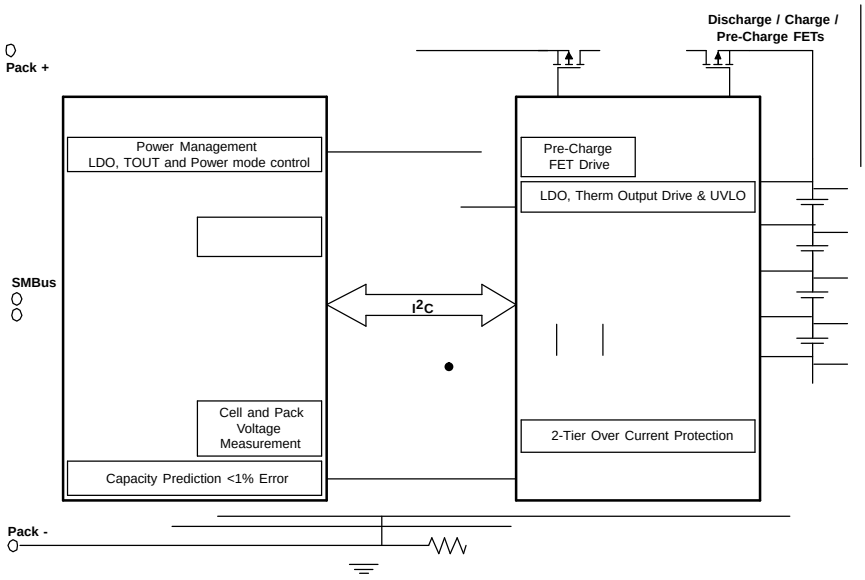
- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq29312 is a 2-, 3-, or 4-cell lithium-ion battery pack protection analog front end (AFE) IC that incorporates a 3.3-V, 25-mA low-dropout regulator (LDO). The bq29312 also integrates an I^2C compatible interface to extract battery parameters such as cell voltages and control output status. Other parameters such as current protection thresholds and delays can be programmed into the bq29312 to increase the flexibility of the battery management system.

The bq29312 provides safety protection for overcharge, overload, short-circuit, overvoltage, and undervoltage conditions in conjunction with the battery management host. In overload and short-circuit conditions, the bq29312 turns the FET drive off autonomously dependant on the internal configuration setting.

SYSTEM PARTITIONING DIAGRAM



DESCRIPTION (Continued)

EL

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, $C_{(REG)}$ = 4.7 µF, BAT = 14 V (unless otherwise noted)

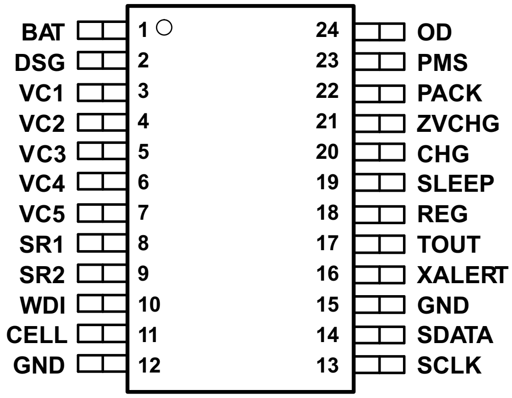
PARAMETER		TEST CONDITION		MIN	NOM	MAX	UNIT
OVER LOAD (OL) AND SHORT CIRCUIT (SC) DETECTION							
V_{OL}	OL detection threshold range, typical(1)			–50		–205	mV
ΔV_{OL}	OL detection threshold program step				5		mV
$V_{HYS(OL)}$	OL detection threshold hysteresis			7	10	13	mV
$V_{(SC)}$	SC detection threshold range, typical(2)	Charge		100		475	mV
		Discharge		–100		–475	
$\Delta V_{(SC)}$	SC detection threshold program step	Charge			25		mV
		Discharge			–25		
$V_{HYS(SC)}$	SC detection threshold hysteresis	Charge and Discharge		40	50	60	mV
$V_{(OL\_acr)}$	OL detection threshold accuracy(1)	Discharge	V_{OL} = 50 mV (min)	40	50	60	mV
			V_{OL} = 100 mV	90	100	110	
			V_{OL} = 205 mV (max)	184	205	226	
$V_{(SC\_acr)}$	SC detection threshold accuracy(2)	Charge and Discharge	V_{SC} = 100 mV (min)	80	100	120	mV
			V_{SC} = 200 mV	180	200	220	
			V_{SC} = 475 mV (max)	426	475	523	
FET DRIVE CIRCUIT							
$V_{(FETON)}$	Output voltage, charge and discharge FETs on	$V_{(FETOND)}$= $V_{(BAT)}$– $V_{(DSG)}$ VGS connect 1 MΩ	BAT= 20 V	12	15	18	V
		$V_{(FETONC)}$=$V_{(PACK)}$– $V_{(CHG)}$ VGS connect 1 MΩ	PACK = 20 V	12	15	18	
$V_{(ZCHG)}$	ZVCHG clamp voltage		PACK= 4.5 V	3.3	3.5	3.7	V
$V_{(FETOFF)}$	Output voltage, charge and discharge FETs off	$V_{(FETOFF)}$= $V_{(PACK)}$– $V_{(DSG)}$	PACK= 16 V			0.2	V
		$V_{(FETOFF)}$=$V_{(BAT)}$– $V_{(CHG)}$	BAT = 16 V			0.2	
t_r	Rise time	C_L = 4700 pF	V_{DSG} :10%–90%		40	200	µs
			V_{CHG} :10%–90%		40	200	
t_f	Fall time	C_L = 4700 pF	V_{DSG} :90%–10%		40	200	µs
			V_{CHG} :90%–10%		40	200	
THERMISTOR DRIVE							
$r_{DS(on)}$	TOUT pass-element series resistance	I_O = –1 mA at TOUT pin, $rds_{(ON)}$ = (V_{REG}– V_O (TOUT))/1 mA, T_A = –25°C to 85°C			50	100	Ω
LOGIC							
$R_{(PUP)}$	Internal pullup resistance	XALERT	T_A = –25°C to 85°C	60	100	200	kΩ
		SDATA, SCLK,	T_A = –25°C to 85°C	6	10	20	
V_{OL}	Logic level output voltage	XALERT, I_O = 200 µA,	T_A = –25°C to 85°C			0.2	V
		SDATA, I_O = 50 µA,	T_A = –25°C to 85°C			0.4	
		OD I_O = 1 mA,	T_A = –25°C to 85°C			0.6	

(1) See OL register for setting detection threshold
(2) See SC register for setting detection threshold

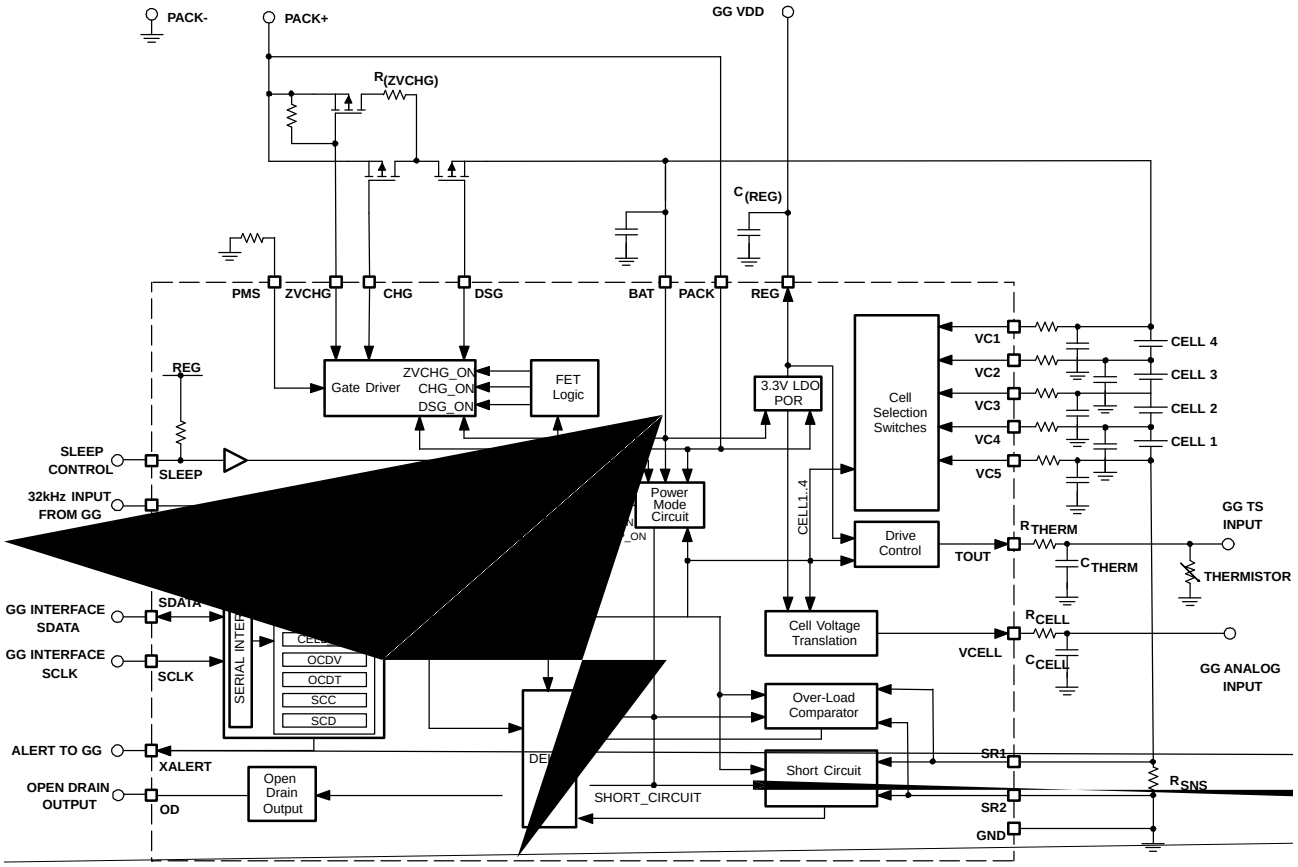
AC ELECTRICAL CHARACTERISTICS

AC

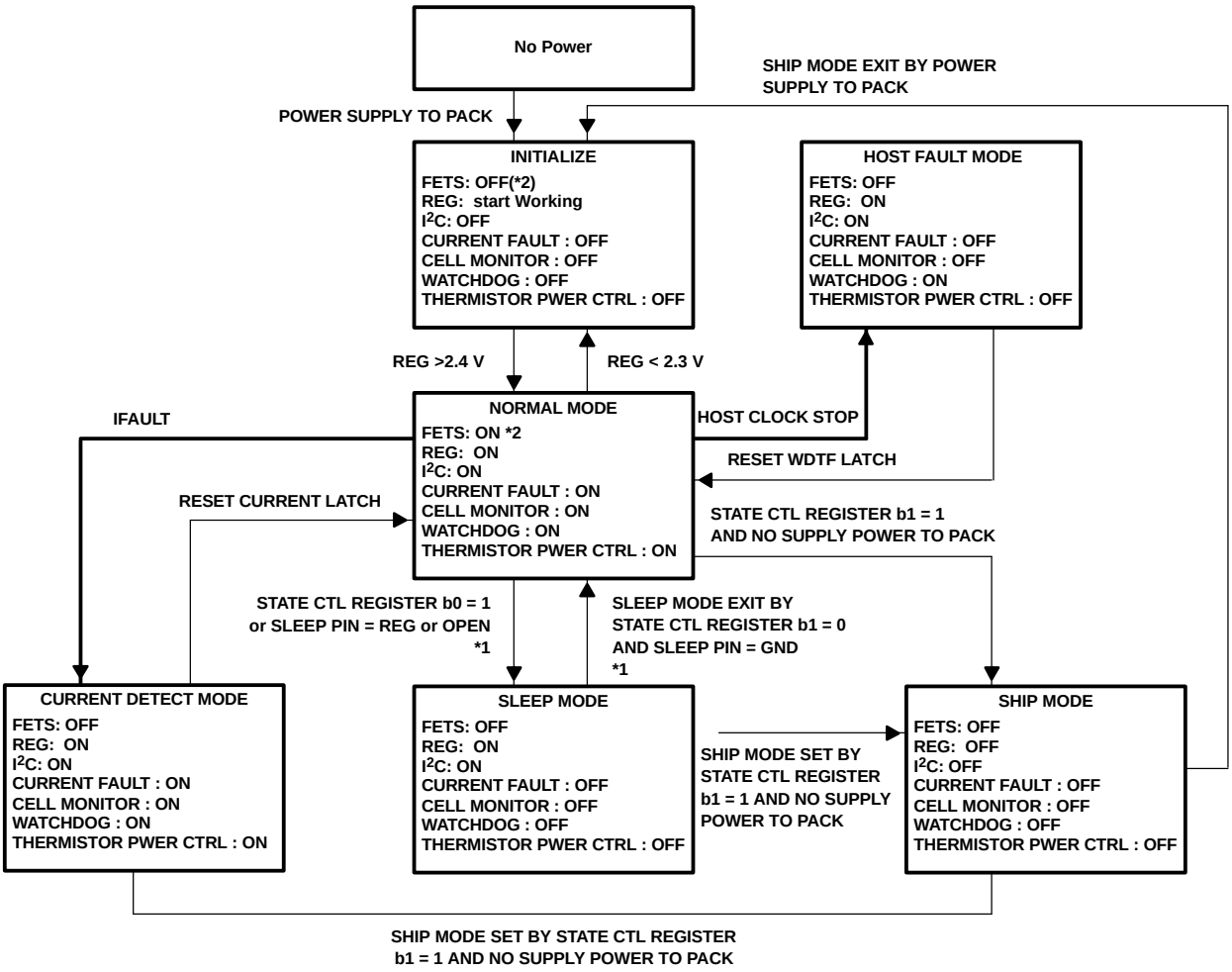
PIN ASSIGNMENTS



FUNCTIONAL BLOCK DIAGRAM



STATE DIAGRAM



Interrupt Request When Enrering These States

*1: Interrupt Request is Granted When Only External Sleep Pin Changes

*2: When PMS connect to Pack, Default State of CHG FET is ON.

FUNCTIONAL DESCRIPTION

Low-Dropout Regulator (REG)

The inputs for this regulator can be derived from the battery cell stack (BAT) or the pack positive terminal (PACK). The output is typically 3.3 V with the minimum output capacitance for stable operation is 4.7 µF and is also internally current limited. During normal operation, the regulator limits output current to typically 50 mA.

Initialization

The bq29312 internal control circuit is powered by the REG voltage, which it also monitors. When the voltage at REG falls below 2.3 V, the internal circuit turns off the FETs and disables all controllable functions, including the REG and TOUT outputs. REG does not start up unless a voltage above $V_{(STARTUP)}$ is supplied to the PACK terminal. After the regulator has started, based on PACK voltage, it keeps operating through the BAT input, even if the PACK voltage is removed. If the BAT input is below the minimum operating range, then the bq29312 does not operate if the supply to the PACK input is removed. After start up, when the REG voltage is above 2.4 V, the bq29312 is in Normal mode.

The initial state of the CHG output depends on the PMS input. If PMS = PACK then CHG = ON however, if PMS = GND then CHG = OFF.

Overload Detection

The overload detection is used to detect abnormal currents in the discharge direction. This feature is used to protect the pass FETs, cells and any other inline components from excessive current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The overload sense voltage is set in the OLV register, and delay time is set in the OLT register. The overload threshold can be programmed from 50 mV to 205 mV in 5-mV steps with the default being 50 mV and hysteresis of 10 mV.

Short-Circuit Detection

The short current circuit detection is used to detect abnormal current in either the chargeusedused

Overload and Short-Circuit Delay

Overload and Short-Circuit Response

FUNCTIONAL DESCRIPTION (continued)

Cell Voltage

The cell voltage is translated to allow a system host to measure individual series elements of the battery. The series element voltage is translated to a GND-based voltage equal to 0.15 ±0.002 of the series element voltage. This provides a range from 0 V to 4.5 V. The translation output is inversely proportional to the input using the following equation.

Where, $V_{(CELL\ OUT)} = -K \times V_{(CELL\ IN)} + 0.975$ (V)

Programming CELL_SEL (b1, b0) selects the individual series element. The CELL_SEL (b3, b2) selects the voltage monitor mode, cell monitor, offset etc.

Calibration of Cell Voltage Monitor Amplifier Gain

The cell voltage monitor amplifier has an offset and to increase accuracy this can be calibrated.

There are a couple of method by calibration circumstance.

The following procedure shows how to measure and calculate the offset and gain as one of example.

- **Step 1**
  - Set CAL1=1, CAL0=1, CELL1=0, CELL0=0, VMEN=1
  - V_{REF} is trimmed to 0.975 V within ±

FUNCTIONAL DESCRIPTION (continued)

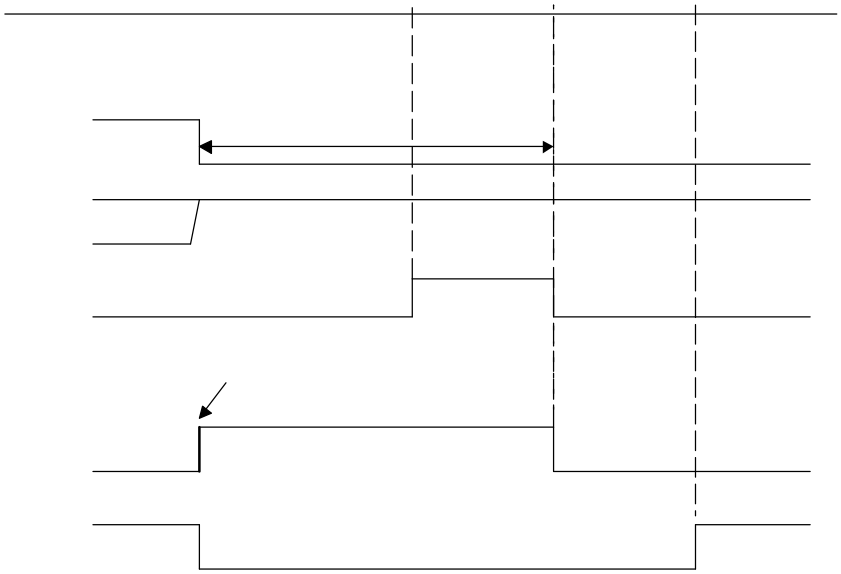


Figure 1. LTCLR and XALERT Clear Example After Sensing Short LTCLR and XALER Clear Example

2-, 3-, or 4-Cell Configuration

In a 3-cell configuration, VC1 is shorted to VC2. In a 2-cell configuration, VC1 and VC2 are shorted to VC3.

FUNCTIONAL DESCRIPTION (continued)

Watchdog Input (WDI)

The WDI input is required as a time base for delay timing when determining overload and short-circuit delay periods and is used as part of the system watchdog.

Initially the watchdog monitors the hosts oscillator start up, if there is no response from the host within 700 ms of the bq29312 reaching its minimum operating voltage, then the bq29312 turns both CHG, DSG and ZVCHG FETs OFF.

Once the watchdog has been started during this wake up period, it monitors the host for an oscillation stop condition, which is defined as a period of 100 µs (typ) where no clock input is received. If an oscillator stop condition is identified, then the watchdog turns the CHG, DSG and ZVCHG FETs OFF. When the host clock oscillation is started, WDF is released, but the flag is latched until LTCLR is toggled.

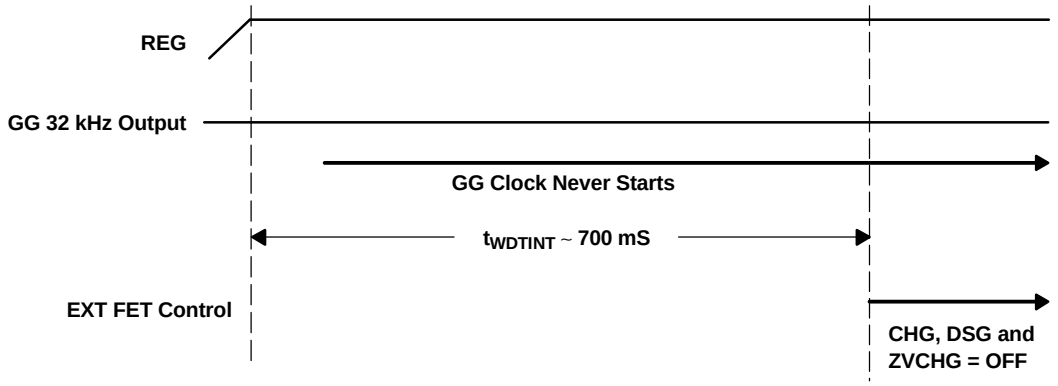


Figure 2. Watchdog Timing Chart—WDI Fault at Startup

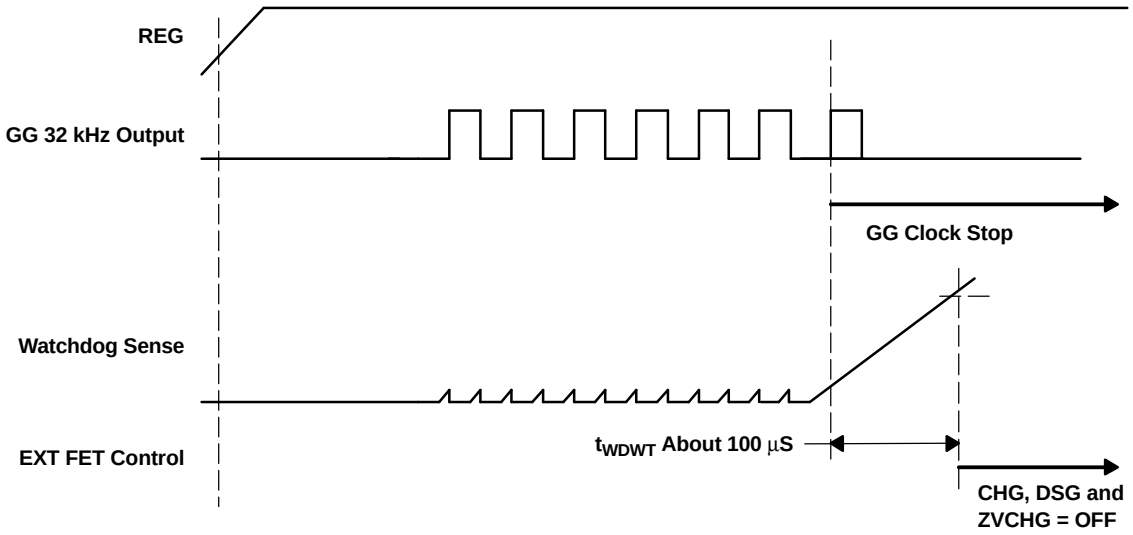


Figure 3. Watchdog Timing Chart—WDI Fault After Startup

DSG and CHG FET Driver Control

The bq29312 drives the DSG, CHG, and ZVCHG FET off if an OL or SC safety threshold is breached depending on the current direction. The host can force any FET on or off only if the bq29312 integrated protection control allows. The DSG and CHG FET drive gate-to-drain voltage is clamped to 15 V (typ).

FUNCTIONAL DESCRIPTION (continued)

The default-state of the CHG and DSG FET drive is off, when PMS = GND. A host can control the FET drive by programming OUTPUT CTL (b3...b1) where b1 is used to control the discharge FET, b2 is used to control the charge FET and b3 is used to control the ZVCHG FET. These controls are only valid when not in the initialized state. The CHG drive FET can be powered by PACK and the DSG FET can be powered by BAT.

Precharge and 0 V Charging—Theory of Operation

The bq29312 supports both a charger that has a precharge mode and one that does not. The bq29312 also supports charging even when the battery falls to 0 V. Detail is described in the application section.

SLEEP Control Input (SLEEP)

The SLEEP input is pulled-up internally to REG. When SLEEP is pulled to REG, the bq29312 enters the SLEEP mode. The SLEEP mode disables all the FET outputs and the OL, SC and watchdog faults are also disabled. The RAM configuration is still valid on exit of the SLEEP mode. The host can force the bq29312 into SLEEP mode via register control also.

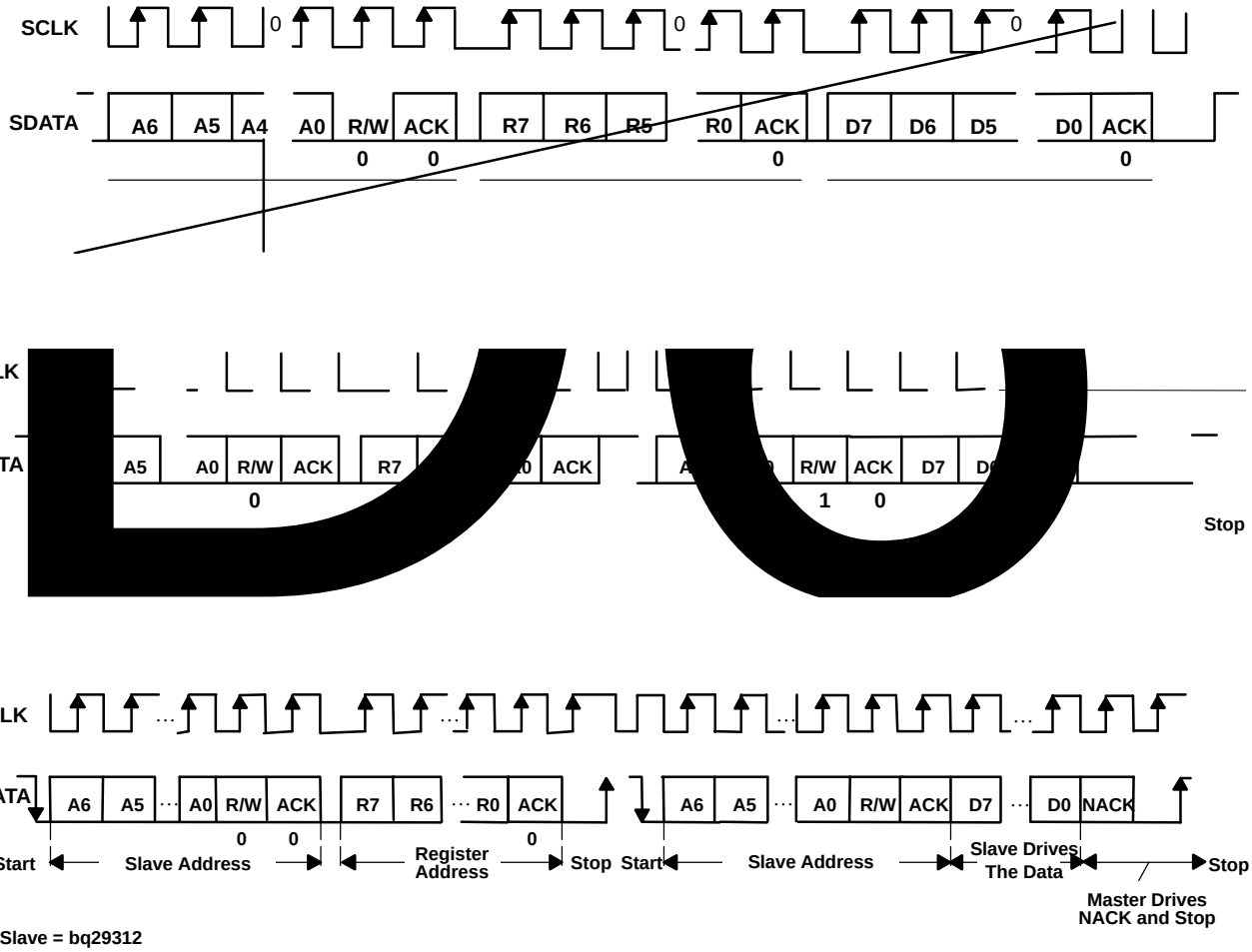
Table 1. SLEEP Control Input

ITEM	SLEEP		EXIT SLEEP
	FUNCTION	I²C READ/WRITE	
I²C Read/Write	Active		
REG Output	Active		
External pin control: CHG, DSG, ZVCHG			

Power Modes

Communications

The I^2C compatible serial communications provides read and write access to the bq29312



Note: Slave = bq29312

Register Map

The bq29312 has 9 addressable registers. These registers provide status, control, and configuration information for the battery protection system.

Table 3. Addressable Registers

NAME	ADDR	TYPE	DESCRIPTION
STATUS	0x00	R	Status register
OUTPUT CTL	0x01	R/W	Output pin control from system host
STATE CTL	0x02	R/W	State control
FUNCTION CTL	0x03	R/W	Function control
CELL _SEL	0x04	R/W	Battery cell select for cell translation and balance bypass and select mode for calibration
OLV	0x05	R/W	Overload threshold voltage
OLT	0x06	R/W	Overload delay time
SCC	0x07	R/W	Short-circuit current threshold voltage and delay for charge
SCD	0x08	R/W	Short-circuit current threshold voltage and delay for discharge

STATUS : Status register

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
0	0	ZVCLMP	SLEEPDET	WDF	OL	SCCHG	SCDSG

The STATUS register provides information about the current state of the bq29312. Reading the STATUS register clears the XALERT pin.

STATUS b0 (SCDSG): This bit indicates a short-circuit in the discharge direction.

0 = Current below the short-circuit threshold in the discharge direction (default).

1 = Current greater than or equal to the short-circuit threshold in the discharge direction.

STATUS b1 (SCCHG): This bit indicates a short-circuit in the charge direction.

0 = Current below the short-circuit threshold in the charge direction (default).

1 = Current greater than or equal to the short-circuit threshold in the charge direction.

STATUS b2 (OL): This bit indicates an overload condition.

0 = Current less than or equal to the overload threshold (default).

1 = Current greater than overload threshold.

STATUS b3 (WDF): This bit indicates a watchdog fault condition has occurred.

0 = 32 kHz oscillation is normal (default).

1 = 32 kHz oscillation stopped or not started and the watchdog has timed out.

STATUS b4 (SLEEPDET): This bit indicates the bq29312 is SLEEP mode.

0 = bq29312 is not SLEEP mode (default).

1 = bq29312 is SLEEP mode.

STATUS b5 (ZVCLMP): This bit indicates ZVCHG output is clamped.

0 = ZVCHG pin is not clamped (default).

1 = ZVCHG pin is clamped.

OUTPUT CTL: Output Control Register

OUTPUT CTL REGISTER (0x01)							
7	6	5	4	3	2	1	0
0	0	0	OD	XZVCHG	CHG	DSG	LTCLR

The OUTPUT CTL register controls the outputs of the bq29312 and can be used to clear certain states.

OUTPUT CTL b0 (LTCLR): When a current limit fault or watchdog timer fault is latched, this bit releases the fault latch when toggled from 0 to 1 and back to 0 (default =0).

0 = (default)

0->1 ->0 clears the fault latches

OUTPUT CTL b1 (DSG): This bit controls the external discharge FET.

0 = discharge FET is off and is controlled by the system host (default).

1 = discharge FET is on and the bq29312 is in normal operating mode.

OUTPUT CTL b2 (CHG): This bit controls the external charge FET.

PMS=GND

0 = chargeoperF4 -10 T3 Tf (0-)Tj /F4 -10 Tf3 Tf (>1)Tj 1 0 0 1 95 0 1 Tm 1 129.8 m 54 1l

STATE CTL: State Control Register

FUNCTION CTL: Function Control Register

FUNCTION CTL REGISTER (0x03)							
7	6	5	4	3	2	1	0
0	0	TOUT	XSCD	SSCC	XOL	PACKOUT	VMEN

The FUNCTION CTL register enables and disables functons of the bq29312.

FUNCTION CTL b0 (VMEN): This bit enables or disables the cell and battery voltage monitoring function.

0 = disable voltage monitoring (default). CELL output is pulled down to GND level.

1 = enable voltage monitoring.

FUNCTION CTL b1 (PACKOUT): This bit is used to translate the PACK input to the CELL pin when VMEN=1 The pack voltage is divided by 25 and is presented on CELL regardless of the CELL_R

CELL SEL: Cell Select Register

CELL_SEL REGISTER (0x04)							
7	6	5	4	3	2	1	0
CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0

This register determines cell selection for voltage measurement and translation, cell balancing and the operational mode of the cell voltage monitoring.

CELL_SEL b0–b1 (CELL0–CELL1): These two bits select the series cell for voltage measurement translation.

CELL1	CELL0	SELECTED CELL
0	0	VC4–VC5, Bottom series element (Default)
0	1	VC4–VC3, Second lowest series element
1	0	VC3–VC2, Second highest series element
1	1	VC1–VC2, Top series element

CELL_SEL b2–b3 (CAL1, CAL0): These bits determine the mode of the voltage monitor block.

CAL1	CAL0	SELECTED MODE
0	0	Cell translation for selected cell (default)
0	1	Offset measurement for selected cell
1	0	Monitor the V_{REF} value for gain calibration
1	1	Monitor the V_{REF} directly value for gain calibration, bypassing the translation circuit

CELL_SEL b4–b7 (CB0–CB3): These 4 bits select the series cell for cell balance bypass path.

CELL SEL b4 (CB0): This bit enables or disables the bottom series cell balance charge bypass path

0 = disable bottom series cell balance charge bypass path (default).

1 = enable bottom series cell balance charge bypass path.

CELL SEL b5 (CB1): This bit enables or disables the second lowest series cell balance charge bypass path.

0 = disable series cell balance charge bypass path (default).

1 = enable series cell balance charge bypass path.

CELL SEL b6 (CB2): This bit enables or disables the second highest cell balance charge bypass path.

0 = disable series cell balance charge bypass path (default).

1 = enable series cell balance charge bypass path.

CELL SEL b7 (CB3): This bit enables or disables the highest series cell balance charge bypass path.

0 = disable series cell balance charge bypass path (default).

1 = enable series cell balance charge bypass path.

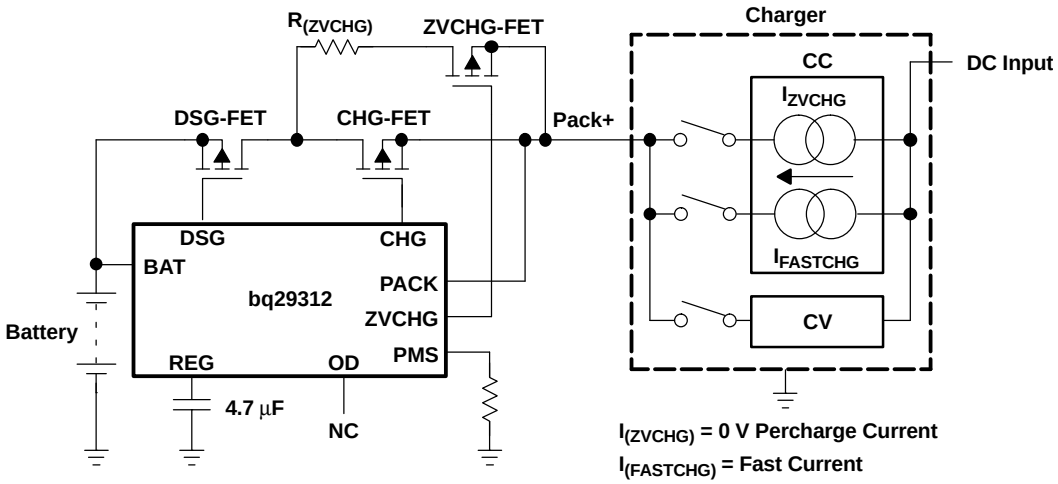
OLV: Overload Voltage Threshold Register

APPLICATION INFORMATION

Precharge and 0-V Charging—Theory of Operation

In order to charge, the charge FET (CHG-FET) must be turned on to create a current path. When the $V_{(BAT)}$ is 0 V and CHG-FET = ON, the $V_{(PACK)}$ is as low as the battery voltage. In this case, the supply voltage for the device is too low to operate. There are 3 possible configurations for this con88 1chaions82.98 1chaions

0-V Charge FET Mode



APPLICATION INFORMATION (continued)

In order to pass 0 V or precharge current an appropriate gate-source voltage $V_{(GS)}$, for ZVCHG-FET must be applied. Here, $V_{(PACK)}$ can be expressed in terms of $V_{(GS)}$ as follows:

$V_{(PACK)} = V_{(ZVCHG)} + V_{(GS)}$(ZVCHG-FET gate - source voltage)

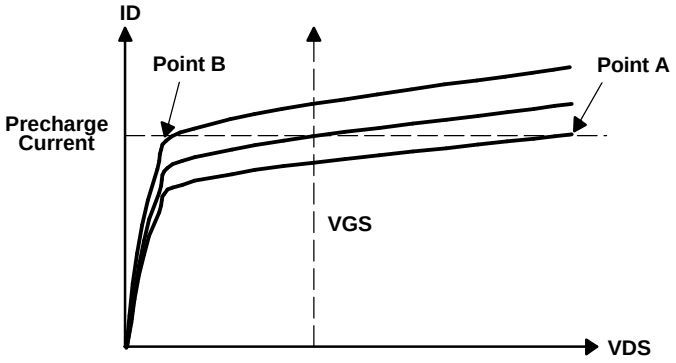


Figure 8. Drain Current vs Drain-Source Voltage Characteristics

In the bq29312, the initial state is for CHG-FET = OFF and ZVCHG-FET = ON with the $V_{(ZVCHG)}$ clamped at 3.5 V initially. Then the charger applies a constant current and raises $V_{(PACK)}$ high enough to pass the precharge current, point A. For example, if the $V_{(GS)}$ is 2 V at this point, $V_{(PACK)}$ is 3.5 V + 2 V = 5.5 V. Also, the ZVCHG-FET is used in its MOS saturation region at this point so that $V_{(DS)}$ is expressed as follows:

APPLICATION INFORMATION (continued)

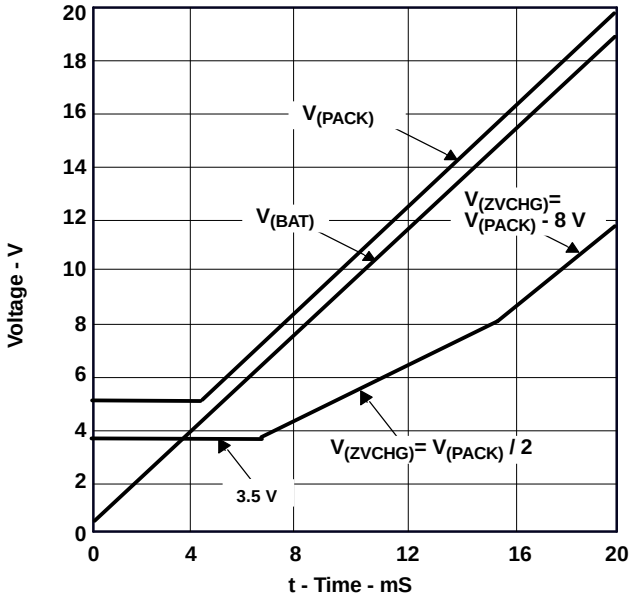


Figure 9. Voltage Transition at ZVCHG, PACK and BAT

As $V_{(PACK)}$ exceeds 7 V, $V_{(ZVCHG)} = V_{(PACK)}/2$. However, $V_{(ZVCHG)}$ is maintained to limit the voltage

APPLICATION INFORMATION (continued)

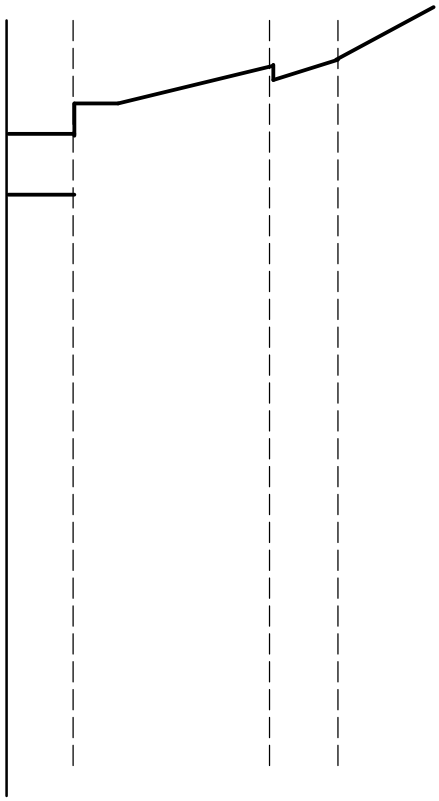


Figure 10. Signal Timing of Pins During 0 V Charging and Precharging (0 V Charge FET)

Common FET

This mode does not require a dedicated precharge FET (ZVCHG-FET). The charge FET (CHG-FET) is ON at initialization of the bq29312 when PMS = $V_{(PACK)}$ allowing for 0 V or precharge current to flow. The application circuit is shown in Figure 11. The charger is expected to provide the precharge function in this mode, where the charger provides a precharge current level suitable to charge cells below a set level, typically below 3.0 V per cell. When the lowest cell voltage rises above this level then a fast charging current is applied.

When the charger is connected the voltage at PMS rises. Once it is above 0.7 V, the CHG output is driven to GND which turns ON the CHG-FET. The charging current flows through the CHG-FET and a back diode of DSG-FET. The pack voltage is represented by the following equation.

$$V_{(PACK)} = V_{(BAT)} + V_F + V_{DS(CHG\text{-}FET)}$$

Where V_F = 0.7 V is the forward voltage of a DSG-FET back diode and is typically 0.7 V.

While $V_{(PACK)}$ is maintained above 0.7 V the precharging current is maintained. While $V_{(PACK)}$ and $V_{(BAT)}$ are under the bq29312 supply voltage then the bq29312 regulator is inactive and the host controller is not functional. Thus, any protection features of this chipset do not function during this period. This state continues until $V_{(PACK)}$ goes higher than the bq29312 minimum supply voltage.

When $V_{(BAT)}$ rises and $V_{(PACK)}$ reaches bq29312 minimum supply voltage, the REG output is active providing a 3.3 V (typ) supply to the host. When this level is reached the CHG pin changes its state from GND to the level controlled with CHG bit in bq29312 registers. In this state, the CHG output level is driven by a clamp circuit so that its voltage level changes from 0 V to 1 V. Also, the host controller is active and can turn ON the DSG-FET.

APPLICATION INFORMATION (continued)

The disadvantages is that during 0 V charging, bq29312 is inactive. The device does not protect the battery and does not update battery information (now is 0 V charging) to the PC.

There are two advantage of this configuration:

1. The voltage between BAT and PACK is lower. Higher precharge current is allowed due to less heat loss is the FET and no external resistor required.
2. The charge FET is turned on during precharging. The precharge current can be fully controlled by the charger.

Figure 11. Common FET Mode Circuit Diagram

The signal timing during the common FET mode is shown in Figure 12. The CHG-FET is turned on when the charger is connected. As $V_{(BAT)}$ rises and $V_{(PACK)}$ reaches the bq29312 minimum supply voltage, the REG output becomes active and the host controller starts to work.

When $V_{(PACK)}$ becomes high enough, the host controller turns ON the DSG-FET. The charger enters the fast charging mode when $V_{(BAT)}$ reaches the fast charge level.

APPLICATION INFORMATION (continued)

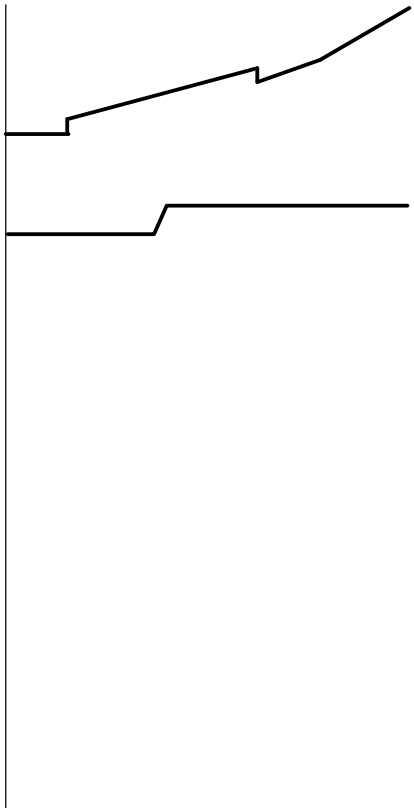
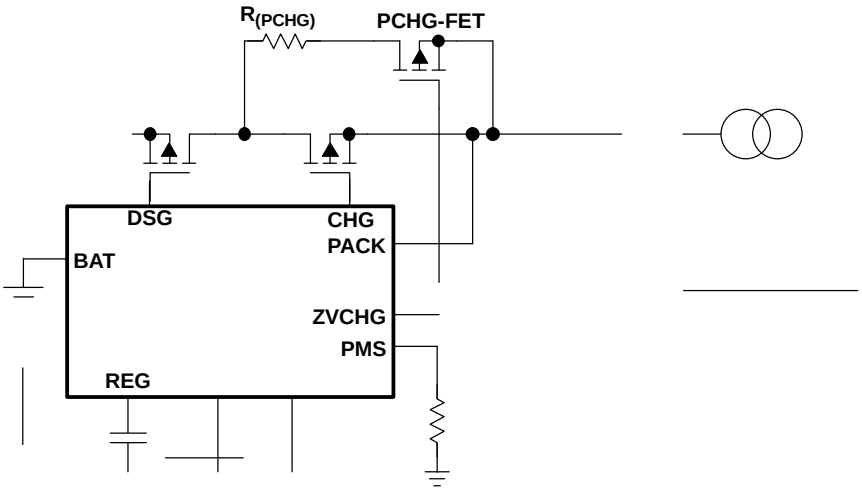


Figure 12. Signal Timing of Pins During 0 V Charging and Precharging (Common FET)

Precharge FET

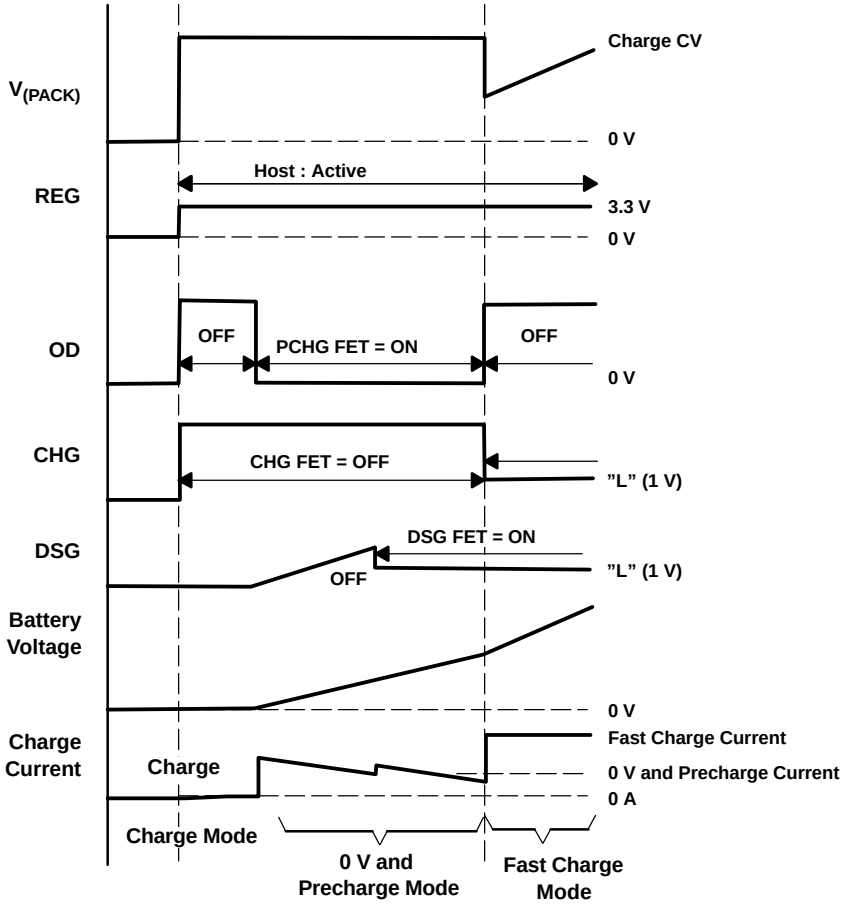
This mode has a dedicated precharge current path using an additional open drain driven FET (PCHG-FET) and sustains the $V_{(PACK)}$ level. In this mode, where the PMS input is connected to GND, the bq29312 and host combine to provide the precharge function by limiting the fast charge current which is provided by the system side charger.

Figure 13 shows the bq29312 application circuit in this mode.


R(PCHG)
PCHG-FET
DSG
CHG
PACK
BAT
ZVCHG
PMS
REG

APPLICATION INFORMATION (continued)

In this configuration, attention must be paid to high power consumption in the PCHG-FET and the series resistor $R_{(PCHG)}$. The highest power is consumed when V_{BAT} = 0 V, where it is the highest differential between the PACK and BAT pins. For example, the power consumption in 4 series cells with 17.4 V fast charge voltage and $R_{(PCHG)}$ = 188 Ω is



APPLICATION INFORMATION (continued)

Summary

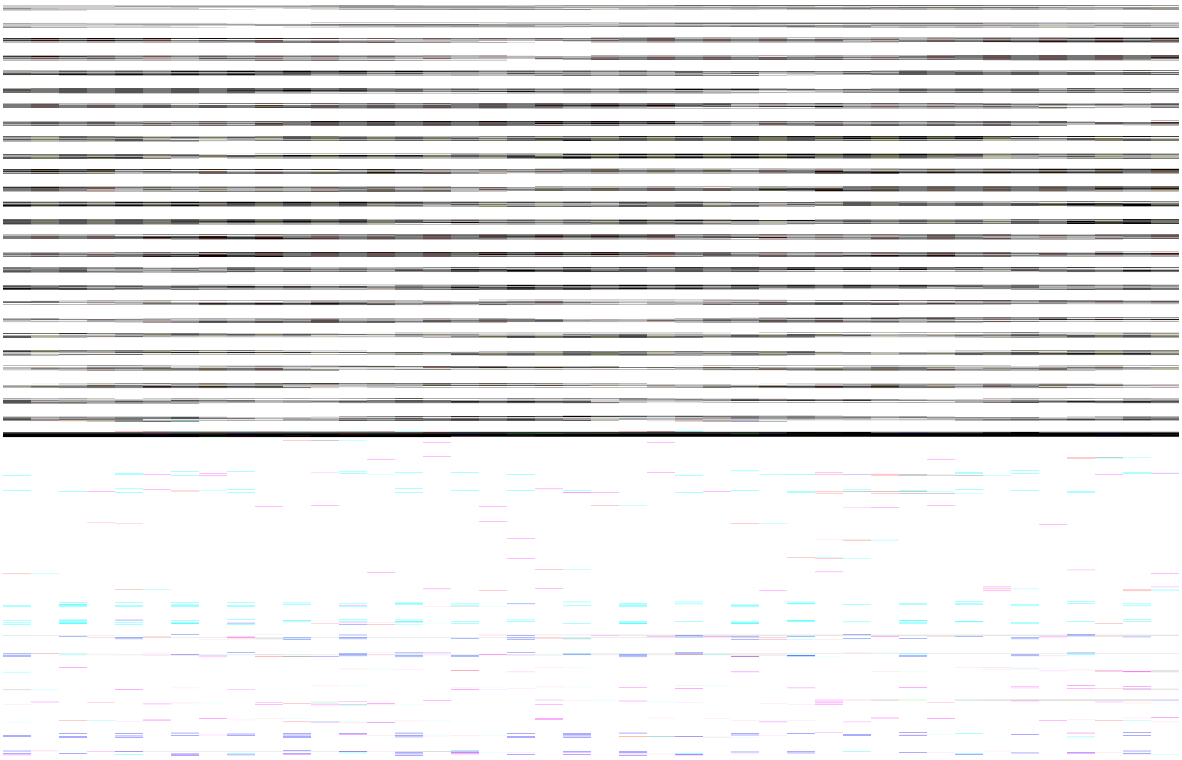
The three types of 0-V charge options available with the bq29312 are summarized in Table 4.

Table 4. Charge Options

CHARGE MODE TYPE	HOST CHARGE CAPABILITIES	KEY APPLICATION CIRCUIT NOTES
1) 0-V Charge FET	Fast charge and precharge	PMS = GND ZVCHG:

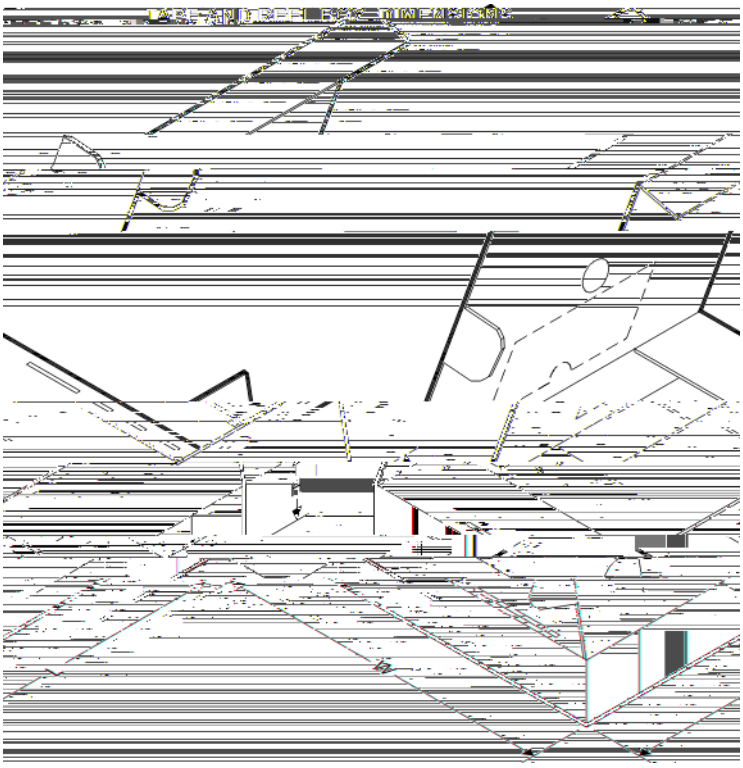
PACKAGE OPTION ADDENDUM

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29312PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1



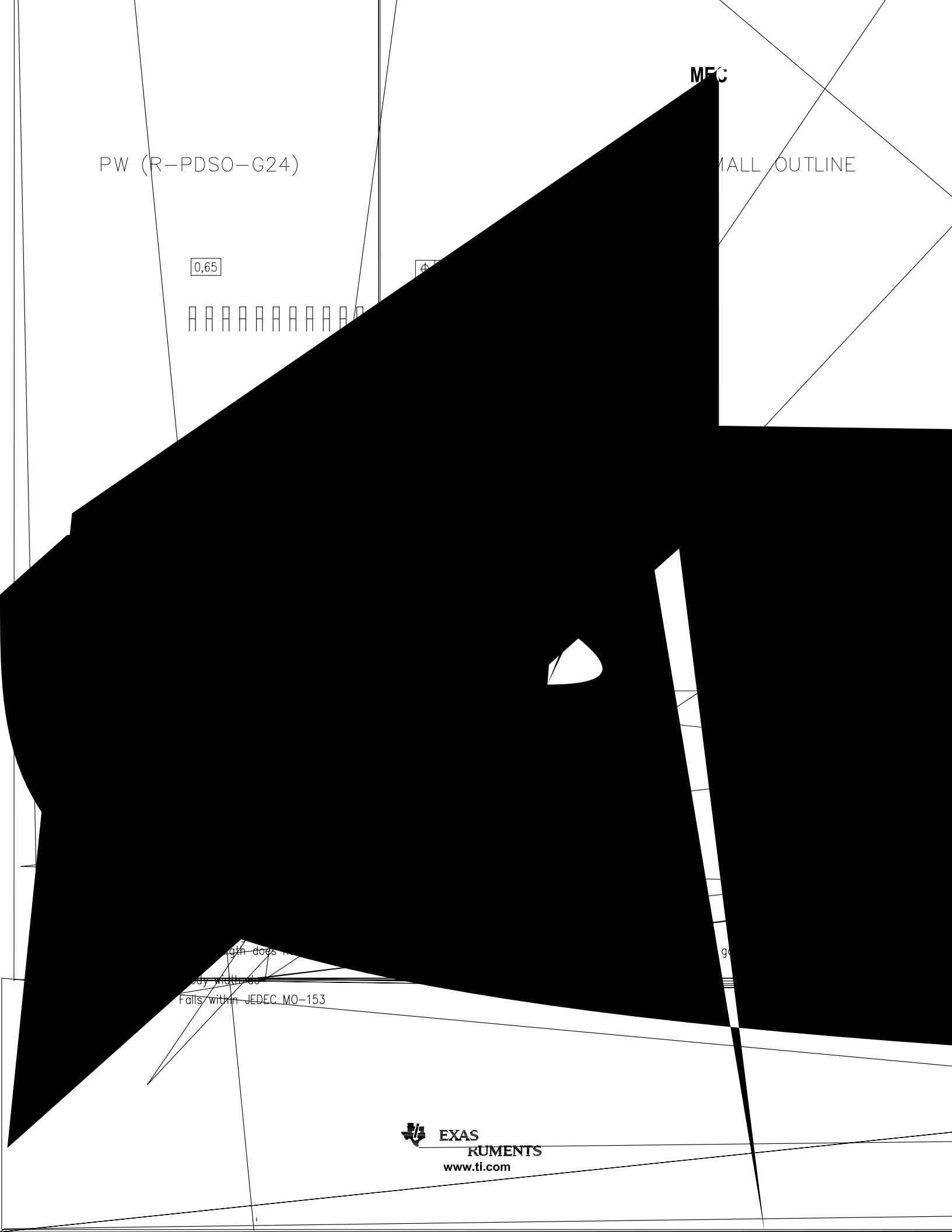
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29312PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

MEC

PW (R–PDSO–G24)

MALL OUTLINE



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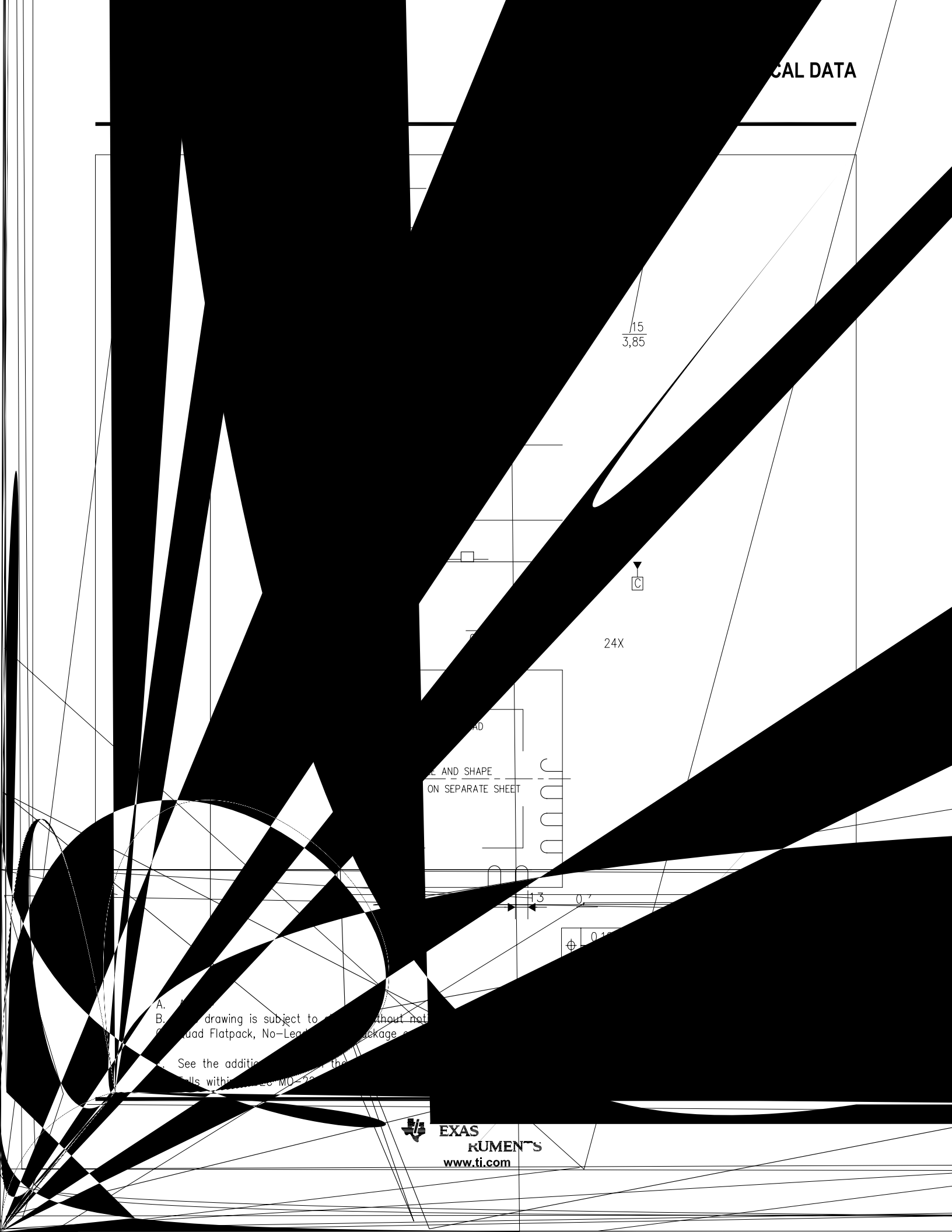
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