# Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

**Check for Samples: bq294700, bq294701, bq294702, bq294703, bq294704, bq294705**

## FEATURES

- **2-, 3-, and 4-Series Cell Overvoltage Protection**
- **External Capacitor-Programmed Delay Timer**
- **Factory Programmed OVP Threshold (Threshold Range 3.85 V to 4.6 V)**
- **Output Options: Active High or Open Drain Active Low**
- **High-Accuracy Overvoltage Protection: ±10 mV**
- **Low Power Consumption $I_{CC}$ 1 µA ($V_{CELL(ALL)} < V_{PROTECT}$)**
- **Low Leakage Current Per Cell Input < 100 nA**
- **Small Package Footprint**
  - **8-Pin SON (2 mm x 2 mm)**

## APPLICATIONS

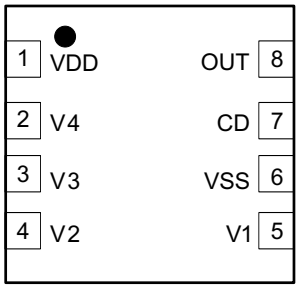
- **Notebook**
- **UPS Battery Backup**

## DESCRIPTION

The bq2947xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq2947xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

For quicker production-line testing, the bq2947xy device provides a Customer Test Mode with reduced delay time.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| $T_A$ | Part Number | Package | Package Designator | OVP (V) | OV Hysteresis (V) | Output Drive | Tape and Reel (Large) |
|---|---|---|---|---|---|---|---|
| –40°C to 110°C | bq294700 | 8-pin SON | DSG | 4.350 | 0.300 | CMOS Active High | bq294700DSGR |
| | bq294701 | | | 4.250 | 0.300 | CMOS Active High | bq294701DSGR |
| | bq294702 | | | 4.300 | 0.300 | CMOS Active High | bq294702DSGR |
| | bq294703 | | | 4.325 | 0.300 | CMOS Active High | bq294703DSGR |
| | bq294704 | | | 4.400 | 0.300 | CMOS Active High | bq294704DSGR |
| | bq294705 | | | 4.450 | 0.300 | CMOS Active High | bq294705DSGR |
| | bq2947xy(1) | | | 3.850–4.600 | 0–0.300 | CMOS Active High | |

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## PIN FUNCTIONS

| bq2947xy | Pin Name | Type I/O | Description |
|---|---|---|---|
| 1 | VDD | P | Power supply input |
| 2 | V4 | IA | Sense input for positive voltage of the fourth cell from the bottom of the stack |
| 3 | V3 | IA | Sense input for positive voltage of the third cell from the bottom of the stack |
| 4 | V2 | IA | Sense input for positive voltage of the second cell from the bottom of the stack |
| 5 | V1 | IA | Sense input for positive voltage of the lowest cell in the stack |
| 6 | VSS | P | Electrically connected to IC ground and negative terminal of the lowest cell in the stack |
| 7 | CD | OA | External capacitor connection for delay timer |
| 8 | OUT | OA | Analog Output drive for overvoltage fault signal. Active High or Open Drain Active Low |
| 9 | PWPD | P | TI recommends connecting the exposed pad to VSS on PCB. |

## PIN DETAILS

In the bq2947xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, $V_{OV}$. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See Figure 2 for details on CD and OUT pin behavior.

Figure 2 shows the behavior of CD pin during an OV sequence.

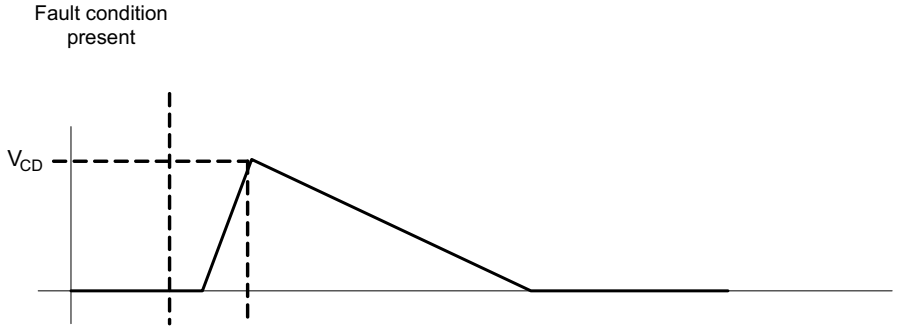



**Figure 2. CD Pin Mechanism**

**NOTE**

In the case of an Open Drain Active Low version, the $V_{OUT}$ signal will be high and transition to low state when the voltage on the $V_{CD}$ capacitor discharges to the set level based on the $t_{CD}$ timer.

### Input Sense Voltage, Vx

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

### Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either Active High or Open Drain Active Low options.

### Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and

To calculate the delay, use the following equation:

$t_{CD}$ (sec) = K * $C_{CD}$ (µF), where K = 10 to 20 range. (1)

Example: If $C_{CD}$= 0.1 µF (typical), then the delay timer range is

$t_{CD}$ (sec) = 10 * 0.1 = 1 s (Minimum)

$t_{CD}$ (sec) = 20 * 0.1 = 2 s (Maximum)

**NOTE**

The tolerance on the capacitor used for $C_{CD}$ increases the range of the $t_{CD}$ timer.

## FUNCTIONAL BLOCK DIAGRAM

Figure 3 shows a CMOS Active High configuration.

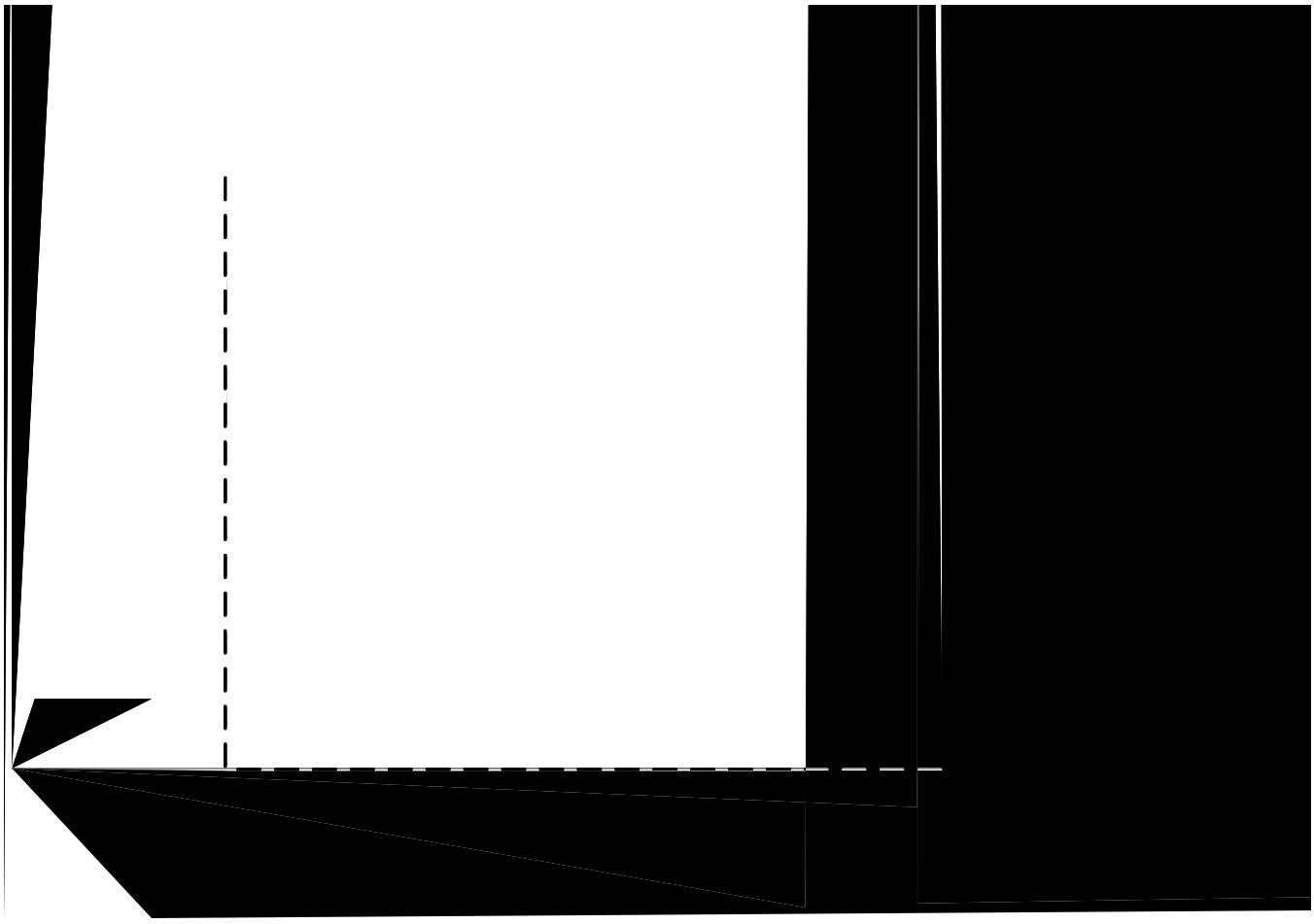


**Figure 3. Block 3CD**Figu

FiguIn13.7 0 2Td (the)Ti 16.9 8 Td (F)Ticai 19.1 0 02d (of)Ti 11.340 2Td (the)an16.9 0 02d (of)TOpi 22.469.3Td (3.)TDrain28.57 0 Td (BLC

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | CONDITION | VALUE/UNIT |
|---|---|---|
| Supply voltage range | VDD–VSS | –0.3 to 30 V |
| Input voltage range | V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS | –0.3 to 30 V |
| Output voltage range | OUT–VSS | –0.3 to 30 V |
| Continuous total power dissipation, $P_{TOT}$ | | See package dissipation rating. |
| Storage temperature range, $T_{STG}$ | | –65 to 150°C |
| Lead temperature (soldering, 10 s), $T_{SOLDER}$ | | 300°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{DD}$(1) | | 3 | | 20 | V |
| Input voltage range | V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS | 0 | | 5 | V |
| Operating ambient temperature range, $T_A$ | | –40 | | 110 | °C |

(1) See APPLICATION SCHEMATIC.

## DC CHARACTERISTICS

Typical values stated where $T_A$ = 25°C and VDD = 14.4 V, MIN/MAX values stated where $T_A$ = –40°C to 110°C and $V_{DD}$ = 3 V to 20 V (unless otherwise noted).

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Voltage Protection Thresholds | | | | | | |
| $V_{OV}$ | $V_{(PROTECT)}$ Overvoltage Detection | bq294700, $R_{IN}$ = 1 kΩ | | 4.350 | | V |
| | | bq294701, $R_{IN}$ = 1 kΩ | | 4.250 | | V |
| | | bq294702, $R_{IN}$ = 1 kΩ | | 4.300 | | V |
| | | bq294703, $R_{IN}$ = 1 kΩ | | 4.325 | | V |
| | | bq294704, $R_{IN}$ = 1 kΩ | | 4.400 | | V |
| | | bq294705, $R_{IN}$ = 1 kΩ | | 4.450 | | V |
| $V_{HYS}$ | OV Detection Hysteresis | bq2947xy(1) | 250 | 300 | 400 | mV |
| $V_{OA}$ | OV Detection Accuracy | $T_A$ = 25°C | –10 | | 10 | mV |
| $V_{OADRIFT}$ | OV Detection Accuracy Across Temperature | $T_A$ = –40°C | –40 | | 40 | mV |
| | | $T_A$ = 0°C | –20 | | 20 | mV |
| | | $T_A$ = 60°C | –24 | | 24 | mV |
| | | $T_A$ = 110°C | –54 | | 54 | mV |
| Supply and Leakage Current | | | | | | |
| $I_{DD}$ | Supply Current | (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V at $T_A$ = 25°C (See Figure 14.) | | 1 | 2 | µA |
| $I_{IN}$ | Input Current at Vx Pins | (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V at $T_A$ = 25°C (See Figure 14.) | –0.1 | | 0.1 | µA |
| $I_{CELL}$ | Input Current (ALL Vx and VDD Input Pins) | Current Consumption at Power down, (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 2.30 V at $T_A$ = 25°C | | 1.1 | | µA |
| Output Drive OUT, CMOS Active High Versions Only | | | | | | |

(1) Future option, contact TI.

## DC CHARACTERISTICS (continued)

Typical values stated where $T_A$ = 25°C and VDD = 14.4 V, MIN/MAX values stated where $T_A$ = –40°C to 110°C and $V_{DD}$ = 3 V to 20 V (unless otherwise noted).

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Drive Voltage, Active High | (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > $V_{OV}$, VDD = 14.4 V, $I_{OH}$ = 100 µA | 6 | | | V |
| | | If three of four cells are short circuited, only one cell remains powered and > $V_{OV}$, VDD = Vx (cell voltage), $I_{OH}$ = 100 µA | | VDD – 0.3 | | V |
| | | (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < $V_{OV}$, VDD = 14.4 V, $I_{OL}$ = 100 µA measured into OUT pin. | | 250 | 400 | mV |
| $I_{OUTH}$ | OUT Source Current (during OV) | (V4–V3), (V3–V2), (V2–V1), or (V1–VSS) > $V_{OV}$, VDD = 14.4 V, OUT = 0 V, measured out of OUT pin. | | | 4.5 | mA |
| $I_{OUTL}$ | OUT Sink Current (no OV) | (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < $V_{OV}$, VDD = 14.4 V, OUT = VDD, measured into OUT pin .Pull resistor $R_{PU}$ = 5 kΩ to VDD = 14.4 V | 0.5 | | 14 | mA |
| Output Drive OUT, CMOS Open Drain Active Low Versions Only | | | | | | |
| $V_{OUT}$ | Output Drive Voltage, Active High | (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < $V_{OV}$, VDD = 14.4 V, $I_{OL}$ = 100 µA measured into OUT pin. | | 250 | 400 | mV |
| $I_{OUTL}$ | OUT Sink Current (no OV) | (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < $V_{OV}$, VDD = 14.4 V, OUT = VDD, measured into OUT pin. Pull resistor $R_{PU}$ = 5 kΩ to VDD = 14.4 V | 0.5 | | 14 | mA |
| $I_{OUTLK}$ | OUT pin leakage | (V4–V3), (V3–V2), (V2–V1), and (V1–VSS) < $V_{OV}$, VDD = 14.4 V, OUT = VDD, measured into OUT pin. | | | 100 | nA |
| Delay Timer | | | | | | |
| $t_{CD}$ | OV Delay Time | $C_{CD}$ = 0.1 µF (see Equation 1) | 1 | 1.5 | 2 | s |
| $t_{CD\_GND}$ | OV Delay Time with CD pin = 0 V | Delay due to $C_{CD}$ capacitor shorted to ground for Customer Test Mode | 20 | | 170 | ms |

## TYPICAL CHARACTERISTICS

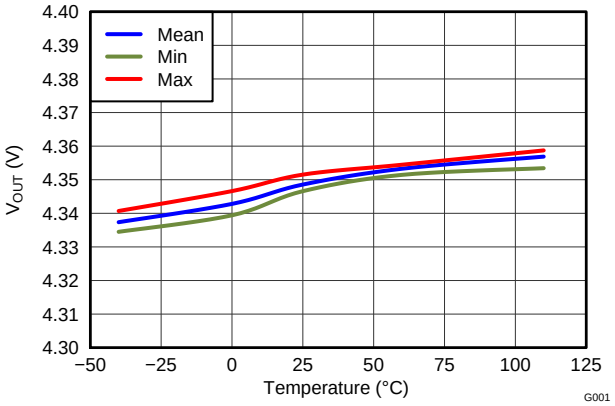



**Figure 4. Overvoltage Threshold (OVT) vs. Temperature**

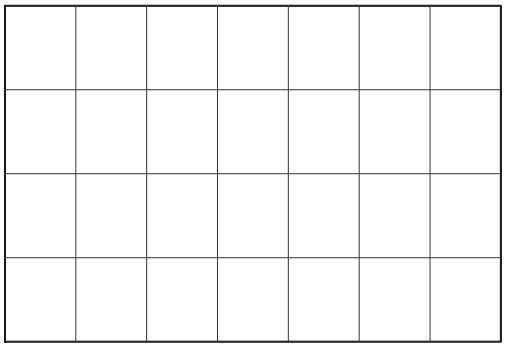


**Figure 5. Hysteresis $V_{HYS}$ vs. Temperature**

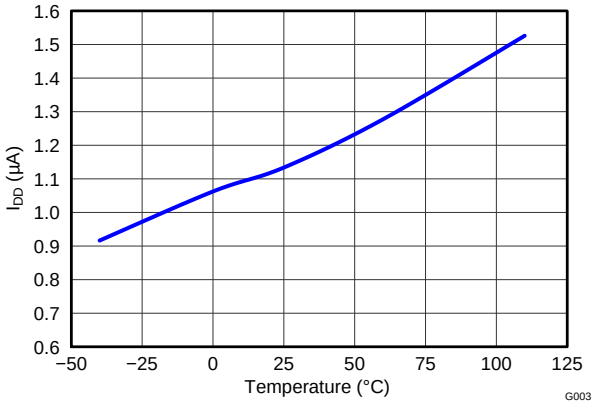



**Figure 6. $I_{DD}$ Current Consumption vs. Temperature at VDD = 16 V**

**Figure 7. $I_{CELL}$ vs. Temperature at $V_{CELL}$= 9.2 V**

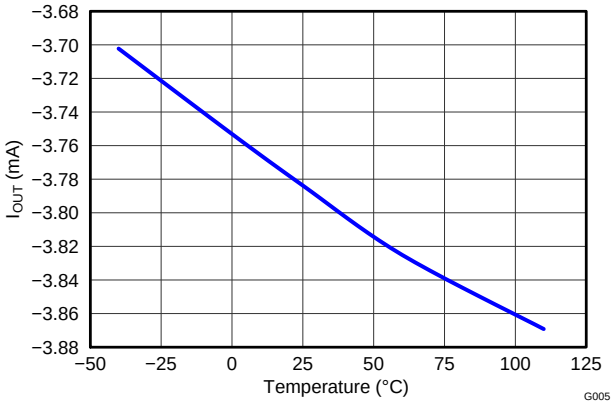



**Figure 8. Output Current $I_{OUT}$ vs. Temperature**

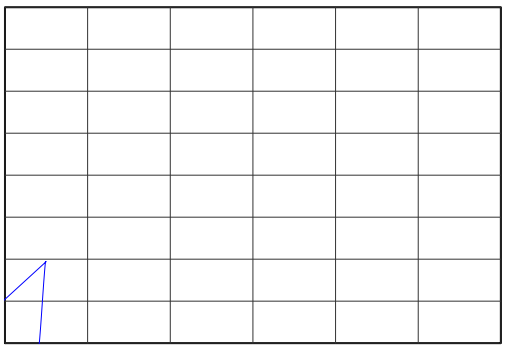


**Figure 9. $V_{OUT}$ vs. $V_{DD}$**

## APPLICATION INFORMATION

Figure 10 shows the recommended reference design components.

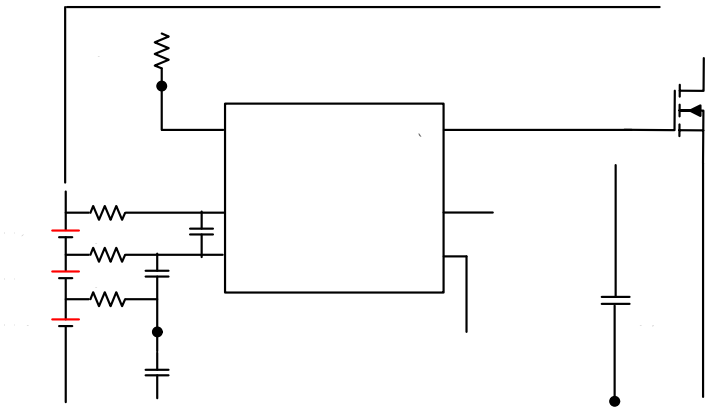


**Figure 10. Application Configuration for Active High**

**NOTE**

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

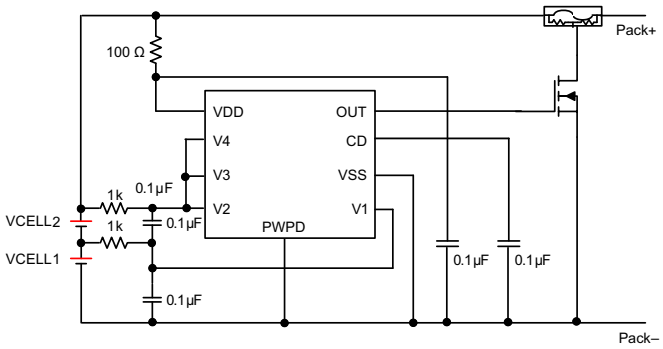
Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

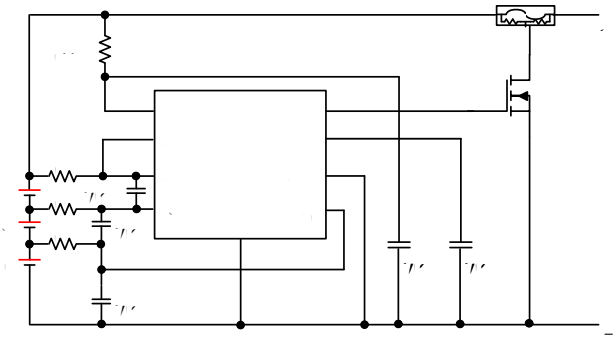
**Table 1. Parameters**

| PARAMETER | EXTERNAL COMPONENT | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage monitor filter resistance | $R_{IN}$ | 900 | 1000 | 4700 | Ω |
| Voltage monitor filter capacitance | $C_{IN}$ | 0.01 | 0.1 | 1.0 | µF |
| Supply voltage filter resistance | $R_{VD}$ | 100 | | 1 | KΩ |
| Supply voltage filter capacitance | $C_{VD}$ | | 0.1 | 1.0 | µF |
| CD external delay capacitance | $C_{CD}$ | | 0.1 | 1.0 | µF |

**NOTE**

The device is calibrated using an $R_{IN}$ value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and $V_{OV}$ trigger level.


Pack+
100 Ω
VDD
OUT
V4
CD
V3
VSS
V2
V1
PWPD
1k
0.1µF
VCELL2
1k
0.1µF
VCELL1
0.1µF
0.1µF
0.1µF
Pack–



## CUSTOMER TEST MODE

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CD\_GND)}$ value, which has a maximum of 170 ms.

Figure 13 shows the timing for the Customer Test Mode.

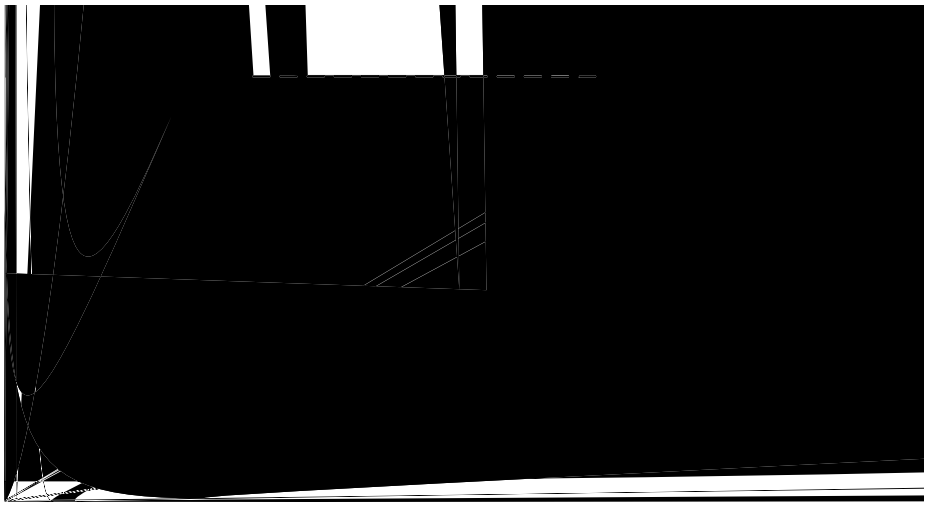


**Figure 13. Timing for Customer Test Mode**

Figure 14 shows the measurement for current consumption of the product for both VDD and Vx.

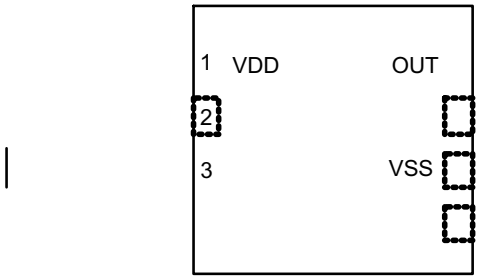



**Figure 14. Configuration for IC Current Consumption Test**

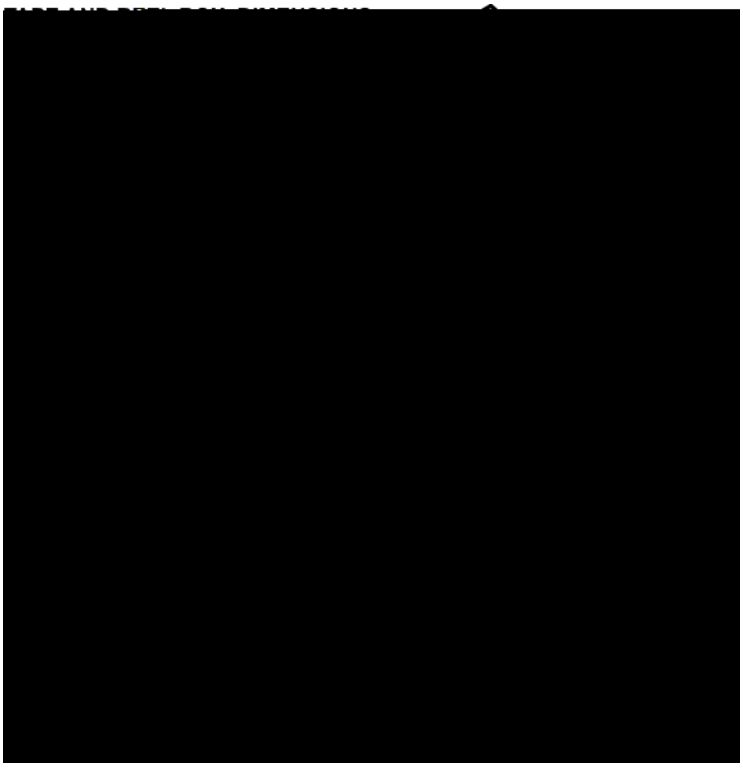
## PACKAGING INFORMATION

| Orderable Device |
| --- |

## TAPE AND REEL INFORMATION

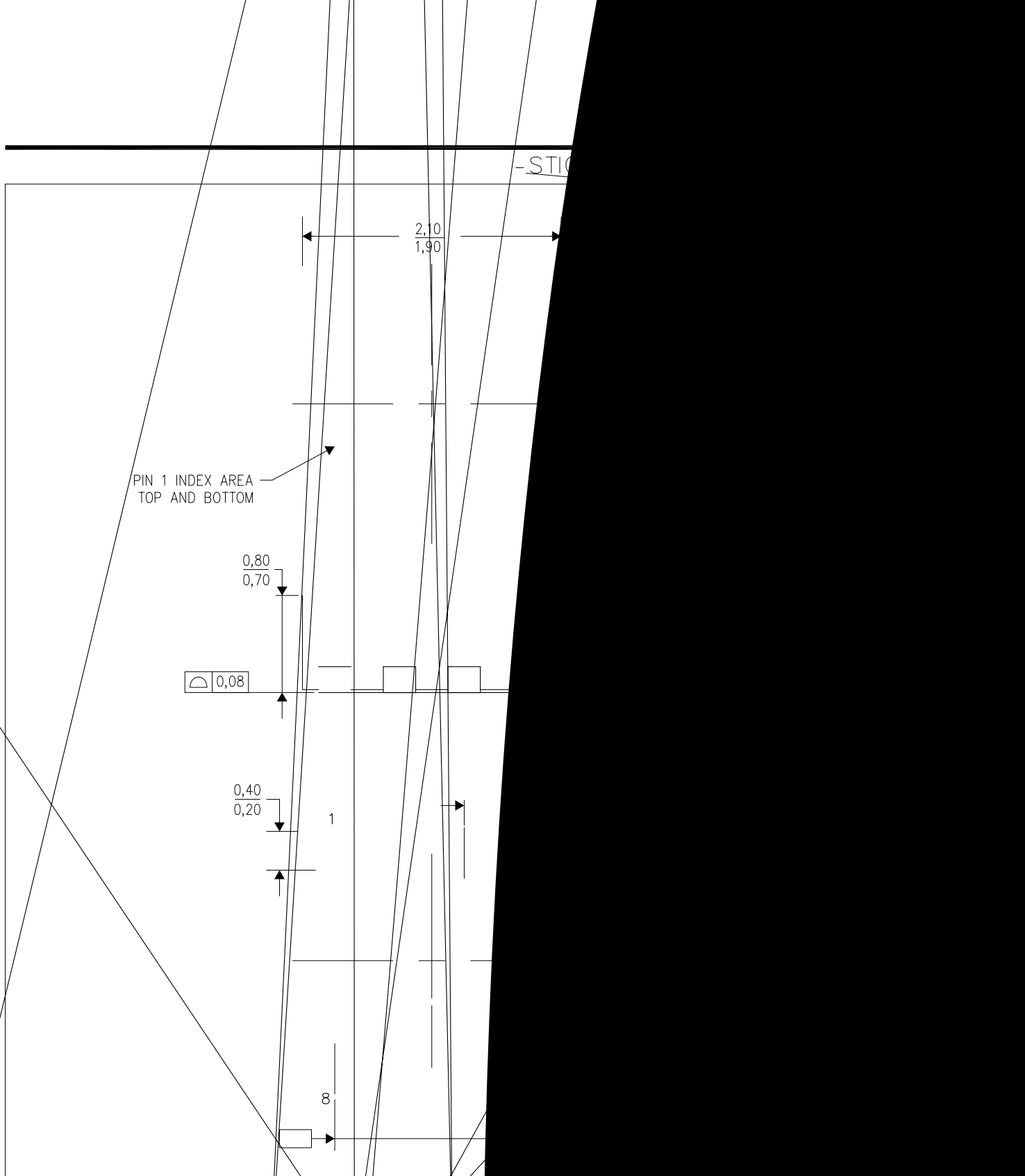

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ294700DSGR | WSON | DSG | 8 | 3000 | 330.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294700DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294701DSGR | WSON | DSG | 8 | 3000 | 330.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294701DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294702DSGR | WSON | DSG | 8 | 3000 | 330.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294702DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294703DSGR | WSON | DSG | 8 | 3000 | 330.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294703DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294704DSGR | WSON | DSG | 8 | 3000 | 330.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294704DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294705DSGR | WSON | DSG | 8 | 3000 | 330.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| BQ294705DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ294700DSGR | WSON | DSG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ294700DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| BQ294701DSGR | WSON | DSG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ294701DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| BQ294702DSGR | WSON | DSG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ294702DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| BQ294703DSGR | WSON | DSG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ294703DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| BQ294704DSGR | WSON | DSG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ294704DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| BQ294705DSGR | WSON | DSG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| BQ294705DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the
See the Product Data Sheet for details regarding the ex
E. Falls within JEDEC MO–229.

TEXAS
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ct is desi

rmal pad must be sold d the

d as a heatsink. In add use of the

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special heatsink structure d into the PCB

QFN/SON PCB Attachment, Texas Instruments Literature

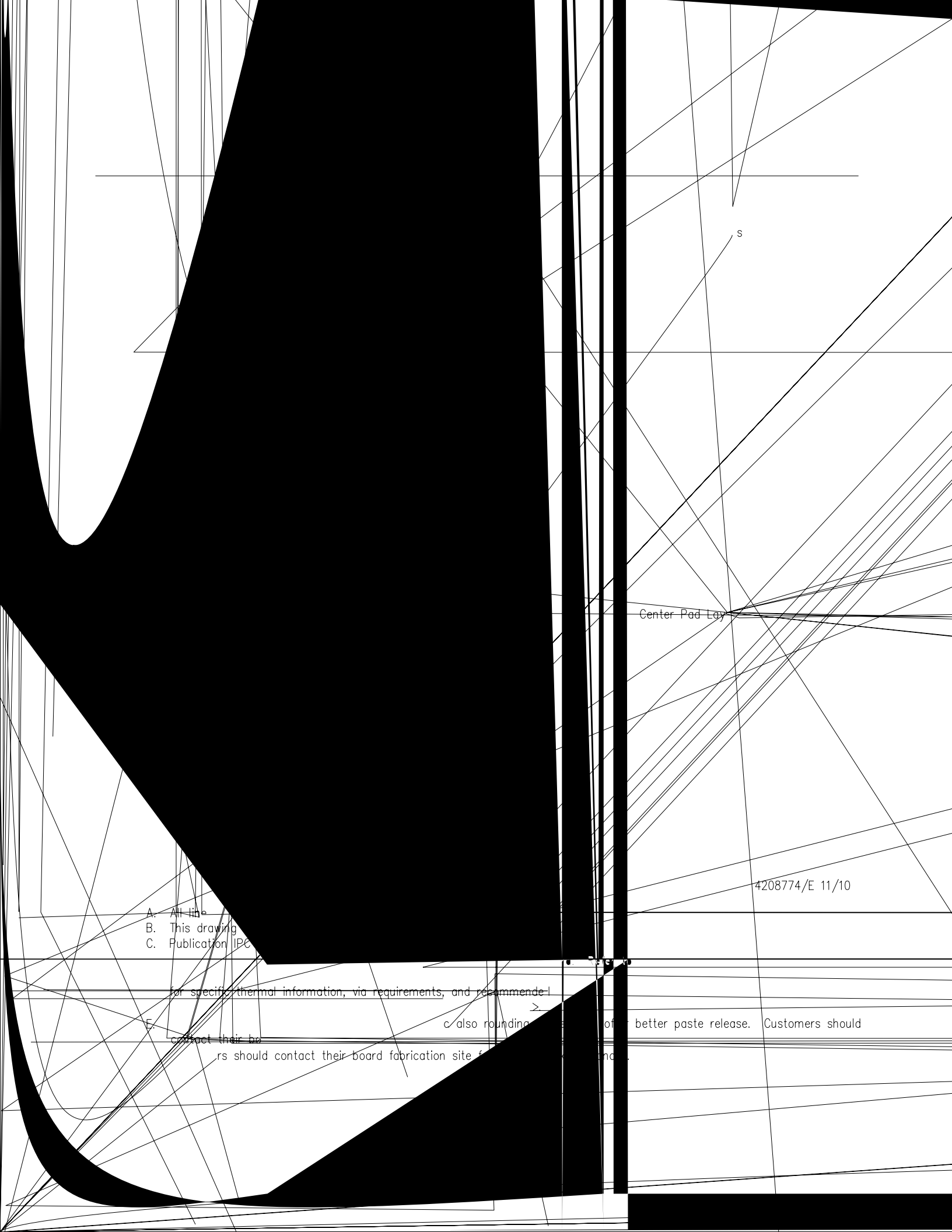
own in the following illustration.

Bottom View

osed Thermal Pad Dimensions

4208347/E 11/10

N in millimeters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Center Pad Lay
4208774/E 11/10

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