

## Voltage Protection for 2-Series, 3-Series, or 4-Series Cell Li-Ion Batteries (Second-Level Protection)

Check for Samples: [bq29440](#), [bq2944L0](#), [bq29441](#), [bq29442](#), [bq29443](#), [bq29449](#), [bq2944L9](#)

### FEATURES

- 2-Series, 3-Series, or 4-Series Cell Secondary Protection
- External Capacitor-Controlled Delay Timer
- Low Power Consumption  $I_{CC} < 2 \mu\text{A}$  Typical [ $V_{\text{CELL(ALL)}} < V_{\text{PROTECT}}$ ]
- High-Accuracy Overvoltage Protection:  $\pm 25$  mV with  $T_A = 0^\circ\text{C}$  to  $60^\circ\text{C}$
- Fixed Overvoltage Protection Thresholds: 4.30 V, 4.35 V, 4.40 V, 4.45 V, 4.50 V
- Small 8L QFN Package

### APPLICATIONS

- Second-Level Protection in Li-Ion Battery Packs
  - Notebook Computers
  - Power Tools
  - Portable Equipment and Instrumentation

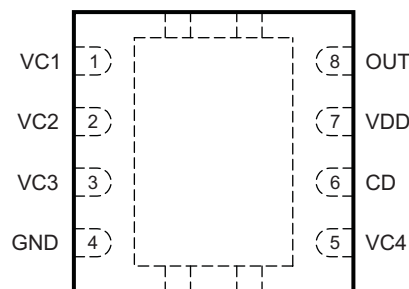
### DESCRIPTION

The bq2944x is a secondary overvoltage protection IC for 2-series, 3-series, or 4-series cell Li-Ion battery packs that incorporates a high-accuracy precision overvoltage detection circuit.

### FUNCTION

The voltage of each cell in a battery pack is compared to an internal reference voltage. If any cells reach an overvoltage condition, the bq2944x device starts a timer that provides a delay proportional to the capacitance on the CD pin. Upon expiration of the internal timer, the OUT pin changes from a low state to a high state. An optional latch configuration is available that holds the OUT pin in a high state indefinitely after an overvoltage condition has satisfied the specified delay timer period. The latch is released when the CD pin is shorted to GND.

DRB Package  
(Top View)



P0012-02



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PART NUMBER	OUT PIN LATCH OPTION	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING	OVP	ORDERING INFORMATION <sup>(2)</sup>	
							TAPE AND REEL (LARGE) <sup>(3)</sup>	TAPE AND REEL (SMALL) <sup>(4)</sup>
-40°C to +110°C	BQ29440	No	QFN-8	DRB	440	4.35 V	BQ29440DRBR	BQ29440DRBT
	BQ2944L0	Yes			44L0	4.35 V	BQ2944L0DRBR	BQ2944L0DRBT
	BQ29441	No			441	4.40 V	BQ29441DRBR	BQ29441DRBT
	BQ29442	No			442	4.45 V	BQ29442DRBR	BQ29442DRBT
	BQ29443	No			443	4.50 V	BQ29443DRBR	BQ29443DRBT
	BQ29449	No			449	4.30 V	BQ29449DRBR	BQ29449DRBT
	BQ2944L9	Yes			44L9	4.30 V	BQ2944L9DRBR	BQ2944L9DRBT

(1) Example: bq2944L0DRBR is a device with the OUT latch option with a V<sub>OV</sub> threshold of 4.35 V.

Contact Texas Instruments for other V<sub>OV</sub> threshold options.

(2) For the most current package and ordering information, see the Package Addendum at the end of this document, or the TI website at www.ti.com.

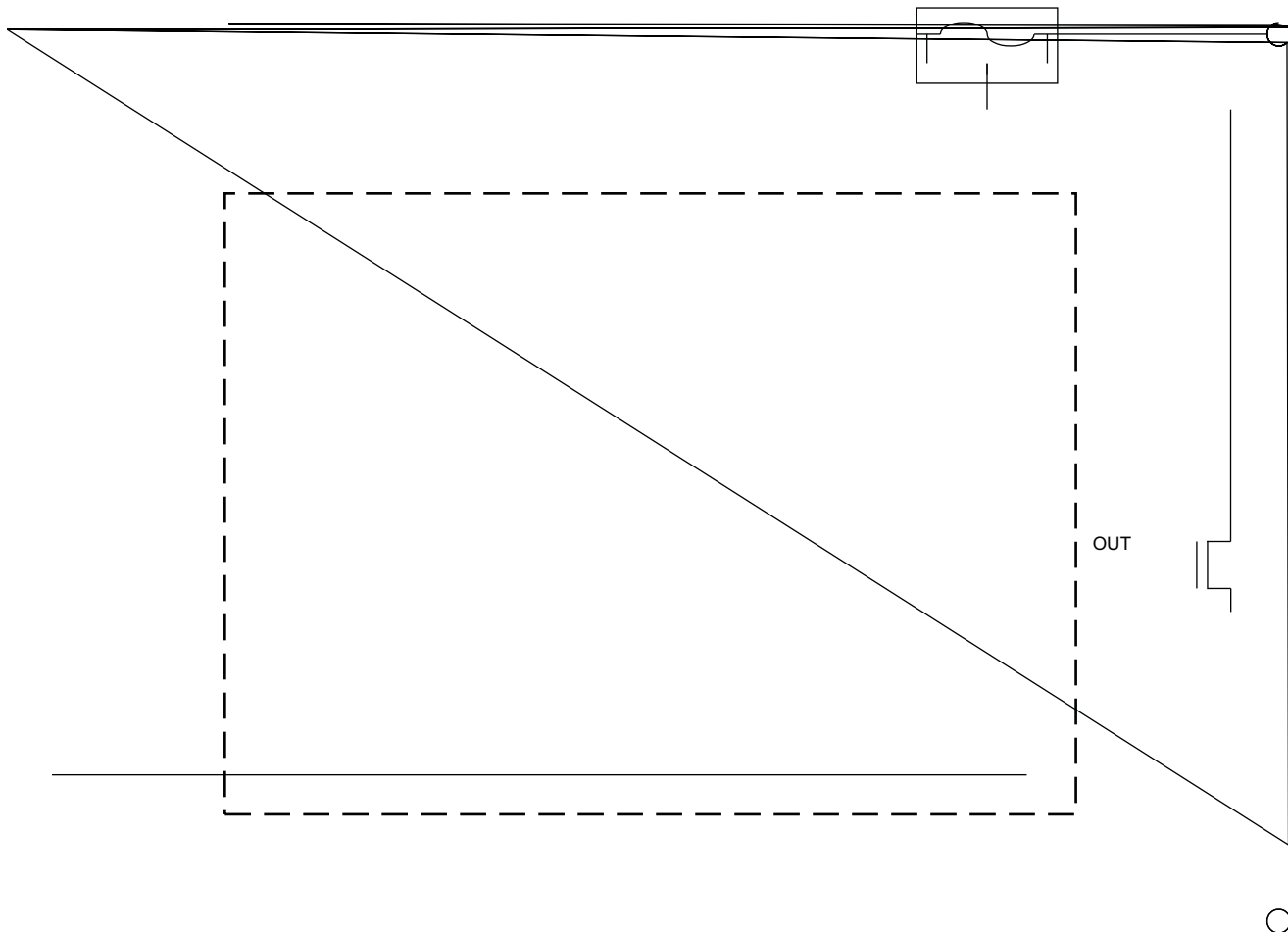
(3) Large tape and reel quantity is 3,000 units.

(4) Small tape and reel quantity is 250 units.

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		bq2944x	UNITS
		DRB	
		8 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	50.5	°C/W
θ <sub>JC(top)</sub>	Junction-to-case(top) thermal resistance <sup>(3)</sup>	25.1	
θ <sub>JB</sub>	Junction-to-board thermal resistance <sup>(4)</sup>	19.3	
ψ <sub>JT</sub>	Junction-to-top characterization		


## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		VALUE/UNIT
Supply voltage range, $V_{MAX}$	VDD–GND	–0.3 to 28 V
Input voltage range, $V_{IN}$	VC1–GND, VC2–GND, VC3–GND	–0.3 to 28 V
	VC1–VC2, VC2–VC3, VC3–VC4, VC4–GND	–0.3 to 8 V
	CD–GND	–0.3 to 8 V
Output voltage range, $V_{OUT}$	OUT–GND	–0.3 to 28 V
Storage temperature range, $T_{stg}$		–65°C to 150°C

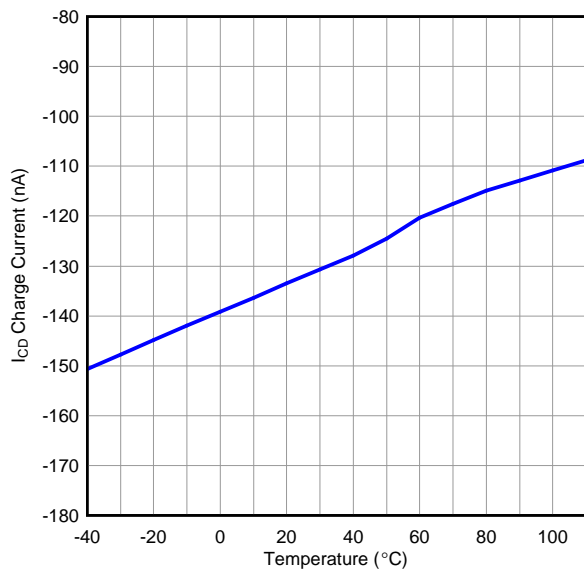
- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4		25	V
Input voltage range	VC1–VC2, VC2–VC3, VC3–VC4, VC4–GND	0		5	V
$t_{d(CD)}$ delay-time capacitance	$C_{CD}$ (See <a href="#">Figure 7.</a> )		0.1		$\mu$ F
Voltage monitor filter resistance	$R_{IN}$ (See <a href="#">Figure 7.</a> )	0.1	1		k

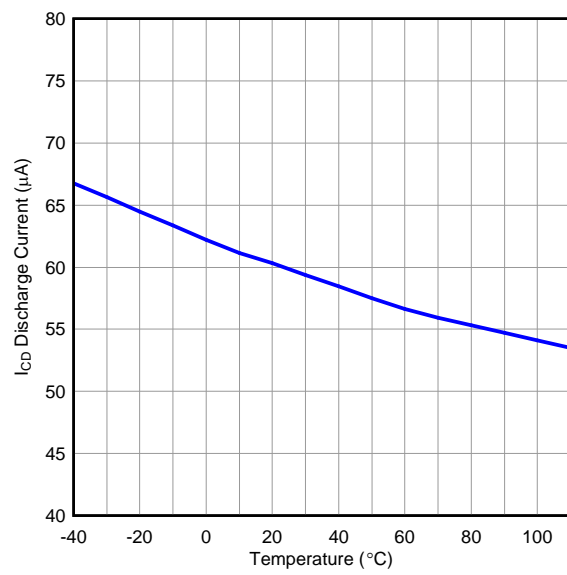



**I<sub>CD</sub> CHARGE CURRENT  
VS  
TEMPERATURE**

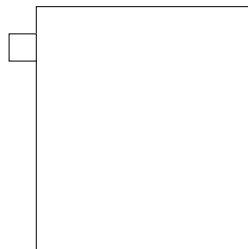


G001

**I<sub>CD</sub> DISCHARGE CURRENT  
VS  
TEMPERATURE**



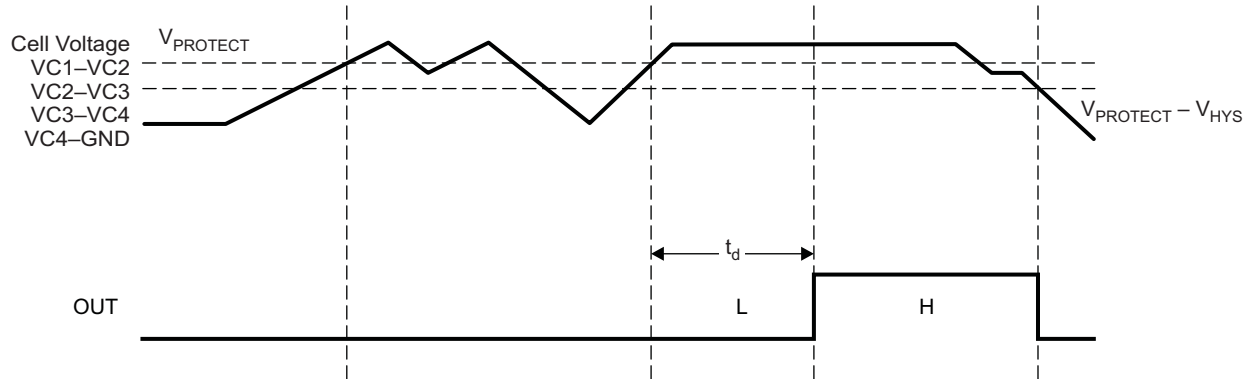
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## APPLICATIONS INFORMATION

### PROTECTION (OUT) TIMING AND DELAY TIME CAPACITOR SIZING

The bq2944x uses an external capacitor to set delay timing during an overvoltage condition. When any of the cells exceed the overvoltage threshold, the bq2944x activates an internal current source of nominally 140 nA, which charges the external capacitor. When the external capacitor charges up to a voltage of nominally 1.2 V, the OUT pin transitions from a low state to a high state, by means of an internal pull-up network, to a regulated voltage of no more than 9.5 V when  $I_{OH} = 0$  mA.



T0461-01

**Figure 4. Timing for Overvoltage Sensing**

Sizing the external capacitor is based on the desired delay time as follows:

$$C_{CD} = \frac{t_d}{X_{DELAY}}$$

Where  $t_d$  is the desired delay time and  $X_{DELAY}$  is the overvoltage delay time scale factor, expressed in seconds per microFarad.  $X_{DELAY}$  is nominally 9.0 s/ $\mu$ F. For example, if a nominal delay of 3 seconds is desired, the customer should use a  $C_{CD}$  capacitor that is 3 s/9.0 s/ $\mu$ F = 0.33  $\mu$ F.

The delay time is calculated as follows:

$$t_d = C_{CD} \times X_{DELAY}$$

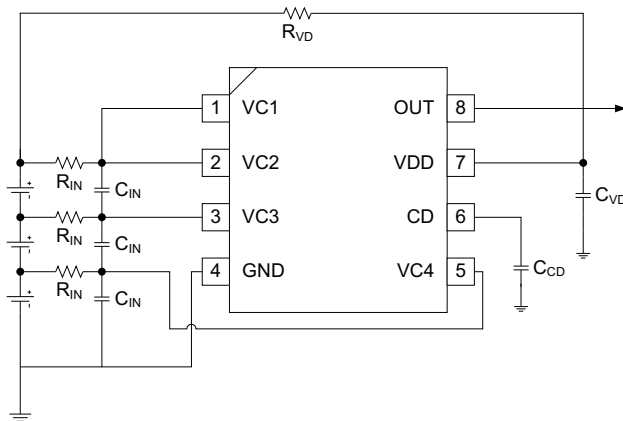
If the cell overvoltage condition is removed before the external capacitoras

the cell is in the network, 3 of 100 Tze (s) (10/910) 83

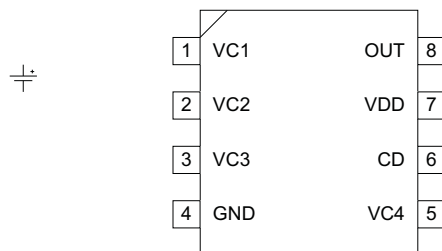
**BATTERY CONNECTION FOR 2-SERIES, 3-SERIES, AND 4-SERIES CELL CONFIGURATIONS**

Figure 5, Figure 6, and Figure 7 show the 2-series, 3-series, and 4-series cell configurations.

**Figure 5. 2-Series Cell Configuration**



**Figure 6. 3-Series Cell Configuration**



**Figure 7. 4-Series Cell Configuration**

## CELL CONNECTION SEQUENCE

### NOTE

Before connecting the cells, propagate the overvoltage delay timing capacitor,  $C_{CD}$ .

The recommended cell connection sequence begins from the bottom of the stack, as follows:

1. GND
2. VC4
3. VC3
4. VC2
5. VC1

While not advised, connecting the cells in a sequence other than that described above does not result in errant activity on the OUT pin. For example:

1. GND
2. VC4, VC3, VC2, or VC1
3. Remaining VCx pin
4. Remaining VCx pin
5. Remaining VCx pin

## CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to greatly reduce the overvoltage detection delay time and enable quicker customer production testing. This mode is intended for quick-pass board-level verification tests, and, as such, individual cell overvoltage levels may deviate slightly from the specifications ( $V_{PROTECT}$ ,  $V_{OA}$ ). If accurate overvoltage thresholds are to be tested, use the standard delay settings that are intended for normal use.

To enter CTM, VDD should be set to approximately 9.5 V higher than VC1. When CTM is entered, the device switches from the normal overvoltage delay time scale factor,  $X_{DELAY}$ , to a significantly reduced factor,  $X_{DELAY\_CTM}$ , thereby reducing the delay time during an overvoltage condition. The CTM overvoltage delay time is similar to the equation presented in [PROTECTION \(OUT\) TIMING AND DELAY TIME CAPACITOR SIZING](#) with the substitution of  $X_{DELAY\_CTM}$  in place of  $X_{DELAY}$ :

$$t_{d\_CTM} = C_{CD} \times X_{DELAY\_CTM}$$

### CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also, avoid exceeding Absolute Maximum Voltages for the individual cell voltages (VC1–VC2), (VC2–VC3), (VC3–VC4), and (VC4–GND). Stressing the pins beyond the rated limits may cause permanent damage to the device.

To exit CTM, power off the device and then power it back on.











For latched versions of the bq2944x, the external  $C_{CD}$  capacitor must be externally discharged if any overvoltage functionality is exercised during protection testing. This can be accomplished by shorting the CD pin to GND. If the  $C_{CD}$  capacitor is not explicitly discharged, a residual charge may cause the overvoltage delay time to be inaccurate.



## REVISION HISTORY

Changes from Revision B (June 2010) to Revision C	Page
• Added new protection thresholds .....	1
• Changed occurrences of $V_{DD}$ to VDD throughout document .....	1
• Added part numbers .....	2
• Changed the Functional Block Diagram .....	3
• Changed the Electrical Characteristics .....	4
• Deleted 3.5 from one of the maximum values from the $V_{OUT}$ specification .....	4
• Changed nominal delay time .....	6

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ29440DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	440	
BQ29440DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	440	
BQ29441DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	441	
BQ29441DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	441	
BQ29442DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	442	
BQ29442DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	442	
BQ29443DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	443	
BQ29443DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	443	
BQ29449DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	449	
BQ29449DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	449	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

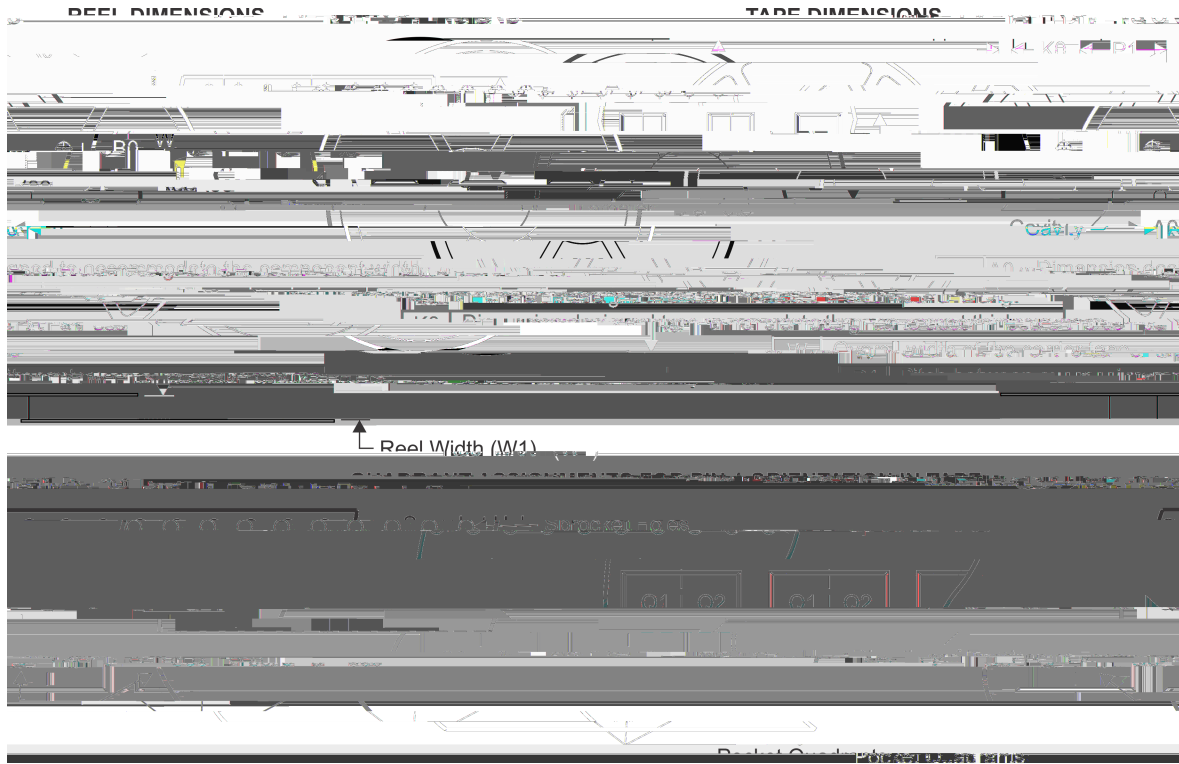
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

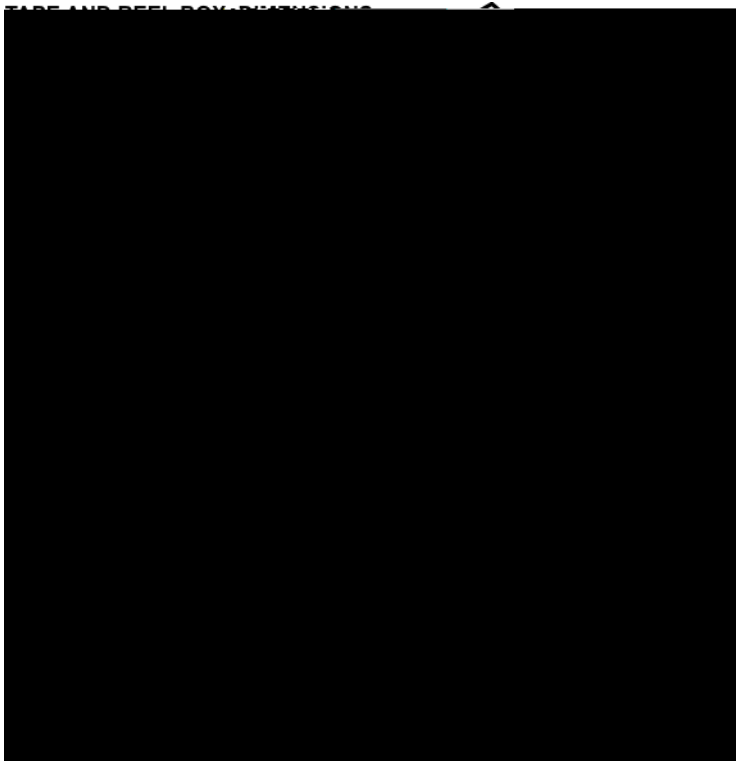
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29440DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29440DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29441DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29441DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29442DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29442DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29443DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29443DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29449DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ29449DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



# PACKAGE MATERIALS INFORMATION

www.ti.com

8-Apr-2013



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29440DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29440DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29441DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29441DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29442DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29442DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29443DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29443DRBT	SON	DRB	8	250	210.0	185.0	35.0
BQ29449DRBR	SON	DRB	8	3000	367.0	367.0	35.0
BQ29449DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



SEATING PLANE

4203482-2/1

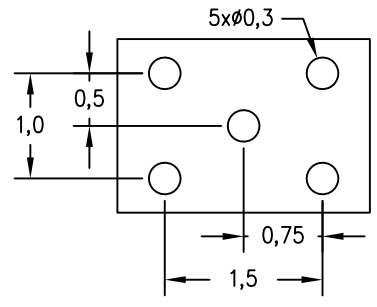
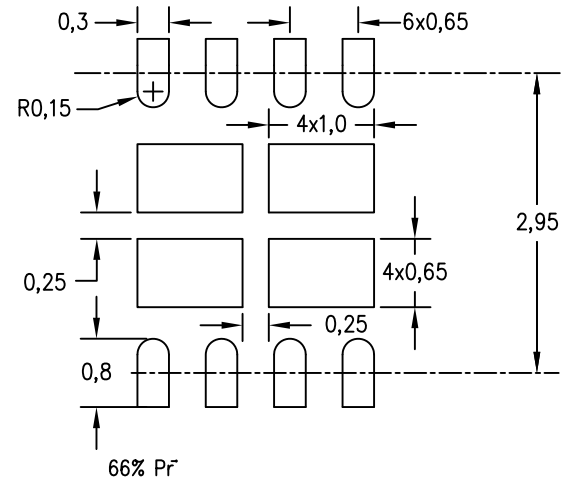
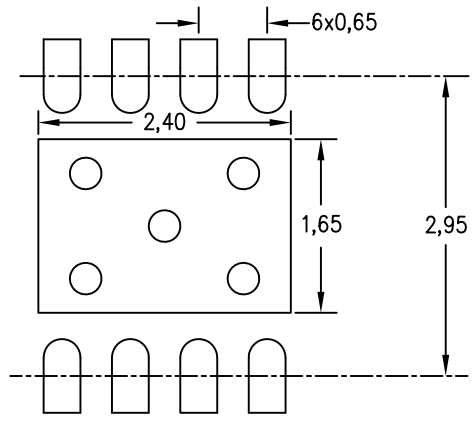
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.

## THERMAL PAD MECHANICAL DATA

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This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached  
designed into the PCB. This design optimizes the heat transfer from the

The exposed thermal pad dimensions for this package are shown in the following illustration.





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