Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

Check for Samples: bq294700, bq294701, bq294702, bq294703, bq294704, bq294705

FEATURES

- **2-, 3-, and 4-Series Cell Overvoltage Protection**
- **External Capacitor-Programmed Delay Timer**
- **Factory Programmed OVP Threshold (Threshold Range 3.85 V to 4.6 V)**
- **Output Options: Active High or Open Drain Active Low**
- **High-Accuracy Overvoltage Protection: ±10 mV**
- **Low Power Consumption I_{CC} 1 µA ($V_{CELL(ALL)} < V_{PROTECT}$)**
- **Low Leakage Current Per Cell Input < 100 nA**
- **Small Package Footprint**
  - **8-Pin SON (2 mm x 2 mm)**

APPLICATIONS

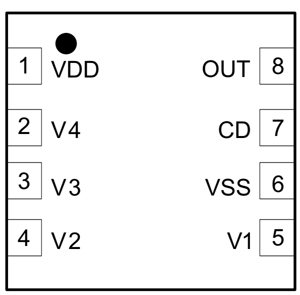
- **Notebook**
- **UPS Battery Backup**

DESCRIPTION

The bq2947xy family of products is an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition.

In the bq2947xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

For quicker production-line testing, the bq2947xy device provides a Customer Test Mode with reduced delay time.



PIN

bq2	Description
	ve voltage of the fourth cell from the bottom of the stack
Sense inpu	ve voltage of the third cell from the bottom of the stack
	ve voltage of the second cell from the bottom of the stack
	ve voltage of the lowest cell in the stack
	d to IC ground and negative terminal of the lowest cell in the stack
	nnection for delay timer
	for overvoltage fault signal. Active High or Open Drain Active Low
	ecting the exposed pad to VSS on PCB.

PIN

In th endently. Overvoltage is detected by comparing the actual cell v ny cell voltage exceeds the programmed OV value, a timer circu n to a nominal value, then slowly discharges it with a fixed curre w a nominal threshold near VSS, the OUT terminal goes from t detection circuit checks to ensure that the CD pin succe quently drops back down to VSS, and if a timeout error is detec UT pin to become active. See Figure 2 for details on CD and O

For an UT pin pulls down to VSS when active (OV present) and is high

4.11C5Tdq(pa3ow)Tj 51.9e1l Td (eTj 2ir Tdq6.1 18

theVSS

Figure 2 shows the behavior of CD pin during an OV sequence.

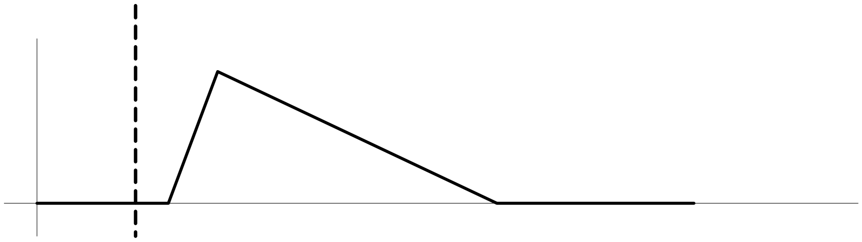


Figure 2. CD Pin Mechanism

NOTE

In the case of an Open Drain Active Low version, the V_{OUT} signal will be high and transition to low state when the voltage on the V_{CD} capacitor discharges to the set level based on the t_{CD} timer.

Input Sense Voltage, Vx

These inputs sense each battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either Active High or Open Drain Active Low options.

Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and Td (VDD) 2j 4 3.41 0 .69 0 T10 Tf 100 Tz 0 0 0 rg 54 2Td (Supply468 0 Td (Tdm Oconnected)Tj 49.5)Tj 18.81 0 5w3pc

is

isCD

when dis4nevior

To calculate the delay, use the following equation:

t_{CD} (sec) = K * C_{CD} (µF), where K = 10 to 20 range. (1)

Example: If C_{CD}= 0.1 µF (typical), then the delay timer range is

t_{CD} (sec) = 10 * 0.1 = 1 s (Minimum)

t_{CD} (sec) = 20 * 0.1 = 2 s (Maximum)

NOTE

The tolerance on the capacitor used for C_{CD} increases the range of the t_{CD} timer.

FUNCTIONAL BLOCK DIAGRAM

Figure 3 shows a CMOS Active High configuration.

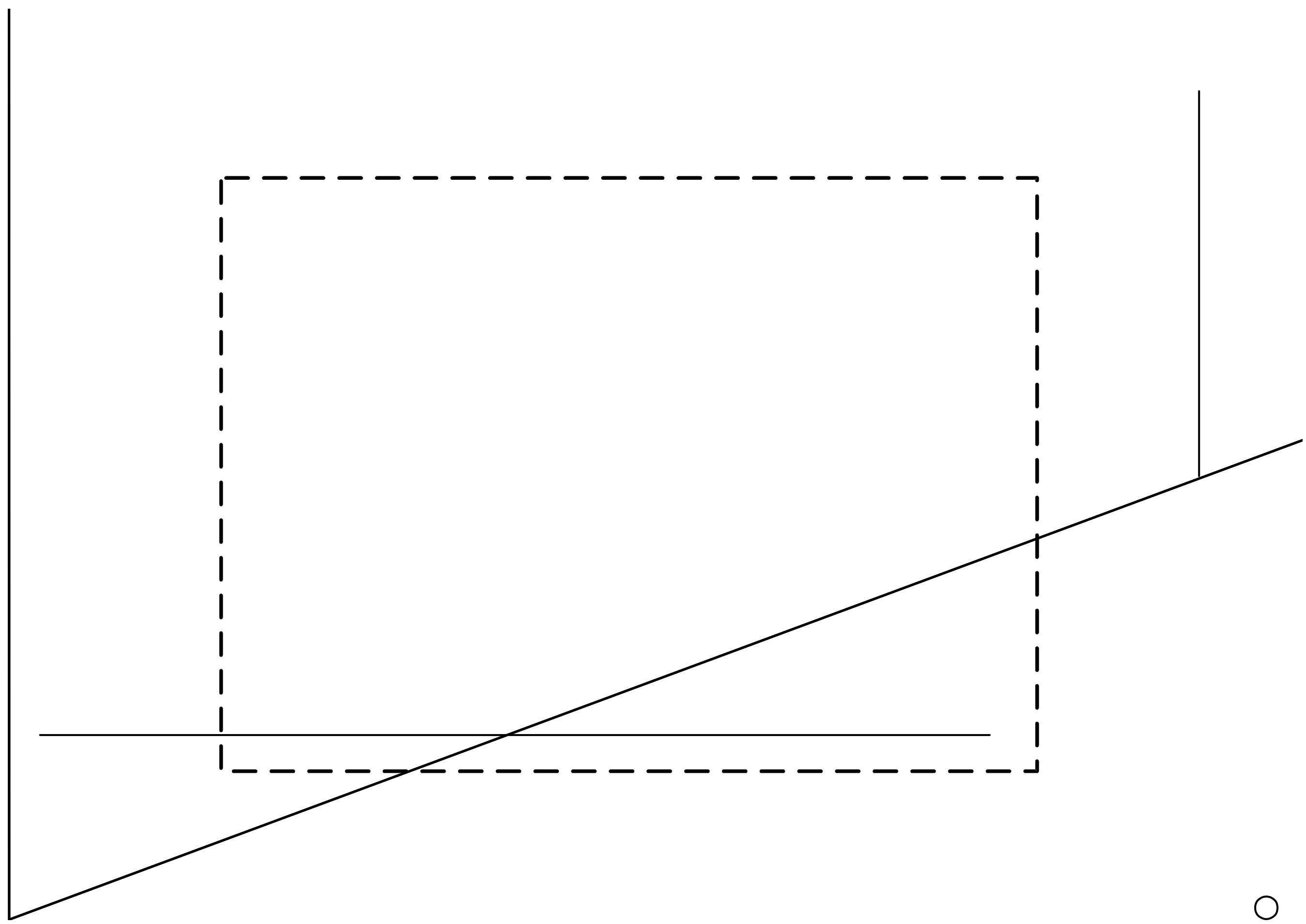


Figure 3. Block Diagram

NOTE

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	–0.3 to 30 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P_{TOT}		See package dissipation rating.
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (1)		3		20	V
Input voltage range	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	0		5	V
Operating ambient temperature range, T_A		–40		110	°C

(1) See APPLICATION SCHEMATIC.

DC CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Protection Thresholds						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	bq294700, R_{IN} = 1 kΩ		4.350		V
		bq294701, R_{IN} = 1 kΩ		4.250		V
		bq294702, R_{IN} = 1 kΩ		4.300		V
		bq294703, R_{IN} = 1 kΩ		4.325		V
		bq294704, R_{IN} = 1 kΩ		4.400		V
		bq294705, R_{IN} = 1 kΩ		4.450		V
V_{HYS}	OV Detection Hysteresis	bq2947xy(1)	250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		40	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
Supply and Leakage Current						
I_{DD}	Supply Current	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V at T_A = 25°C (See Figure 14.)		1	2	µA
I_{IN}	Input Current at Vx Pins	(V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 4.0 V at T_A = 25°C (See Figure 14.)	–0.1		0.1	µA
I_{CELL}	Input Current (ALL Vx and VDD Input Pins)	Current Consumption at Power down, (V4–V3) = (V3–V2) = (V2–V1) = (V1–VSS) = 2.30 V at T_A = 25°C		1.1		µA
Output Drive OUT, CMOS Active High Versions Only						

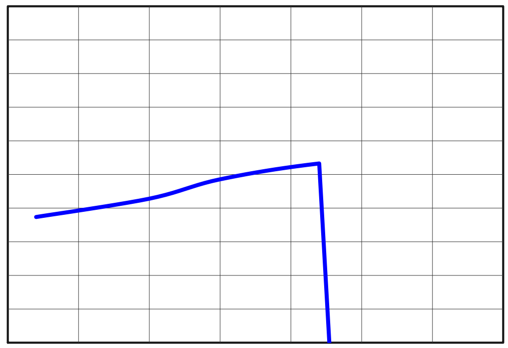
(1) Future option, contact TI.

DC CHARACTERISTICS (continued)

Typical values stated where T_A = 25°C and VDD = 14.4 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 20 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
		(V4Td/(=)TTz 0 0 0 rg 486.6 670.2 Td (MAX)Tj d (otherwise)Tj 41.21 0 Td (noted).)Tj7.8				se333

TYPICAL CHARACTERISTICS



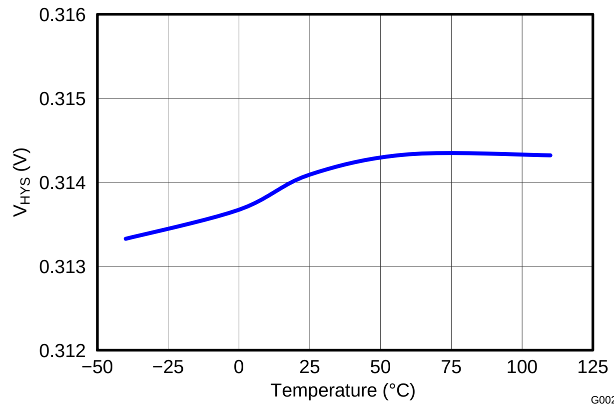
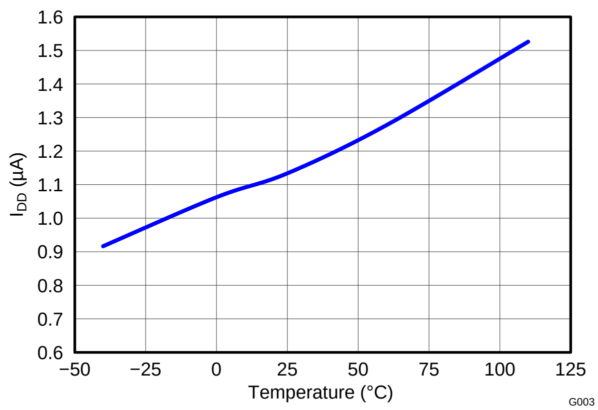
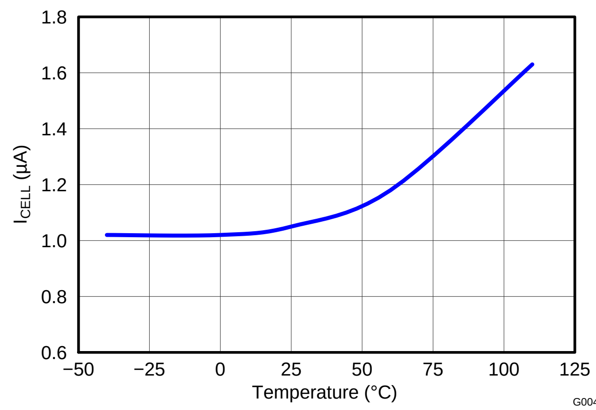
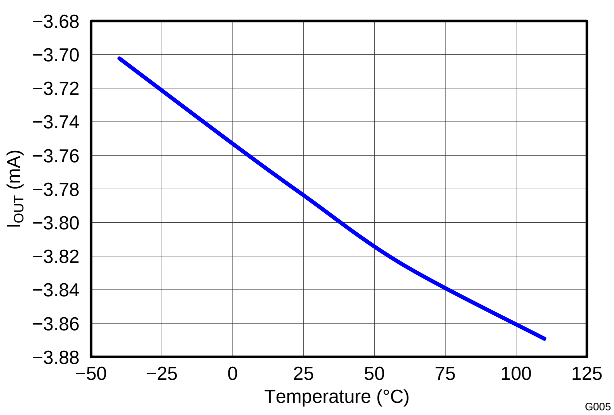


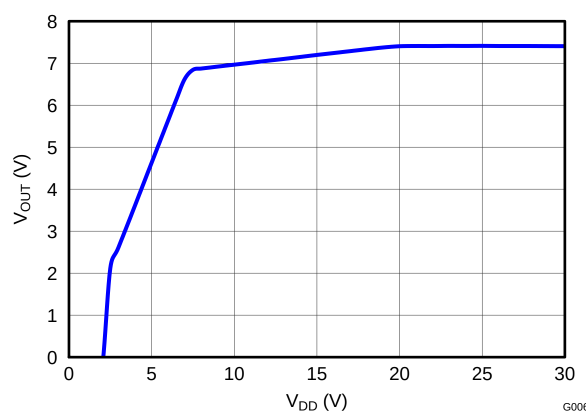
Figure 4. Overvoltage Threshold (OVT) vs.

Figure 5. Hysteresis V_{HYS}









APPLICATION INFORMATION

Figure 10 shows the recommended reference design components.

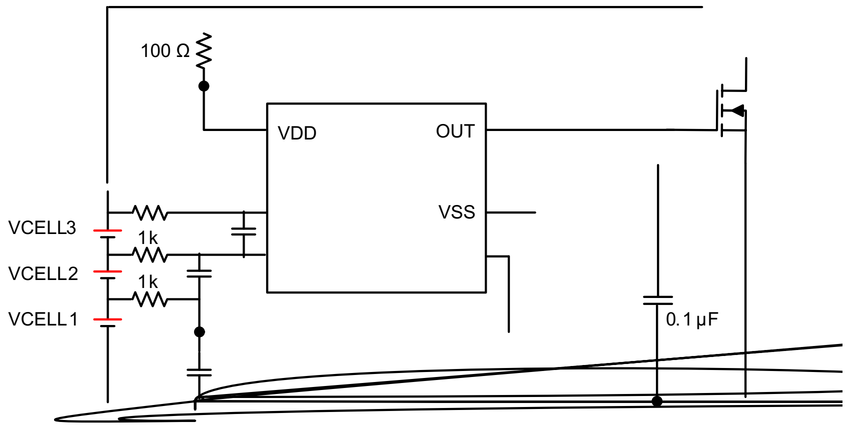


Figure 10. Application Configuration for Active High

NOTE

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements.

Table 1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	4700	Ω
Voltage monitor filter capacitance	C_{IN}	0.01	0.1	1.0	µF
Supply voltage filter resistance	R_{VD}	100		1	KΩ
Supply voltage filter capacitance	C_{VD}		0.1	1.0	µF
CD external delay capacitance	C_{CD}		0.1	1.0	µF

NOTE

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

APPLICATION SCHEMATIC

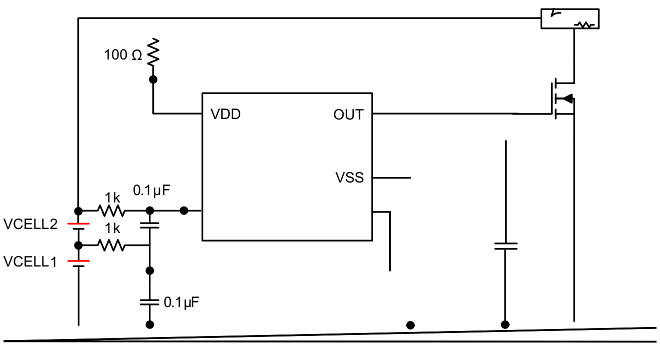


Figure 11. 2-Series Cell Configuration Active High with Capacitor-Programmed Delay

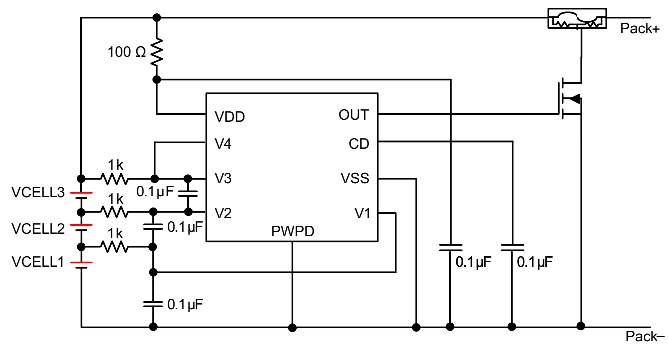


Figure 12. 3-Series Cell Configuration Active High with Capacitor-Programmed Delay

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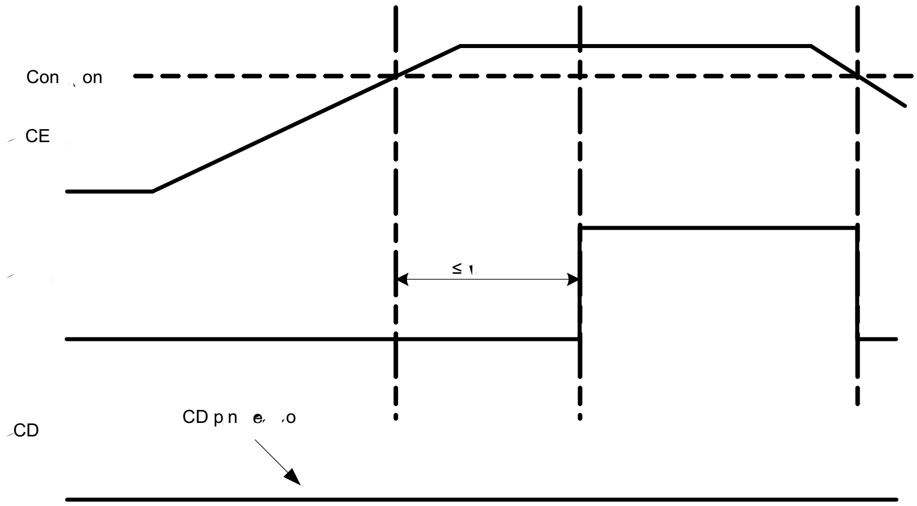
NOTE

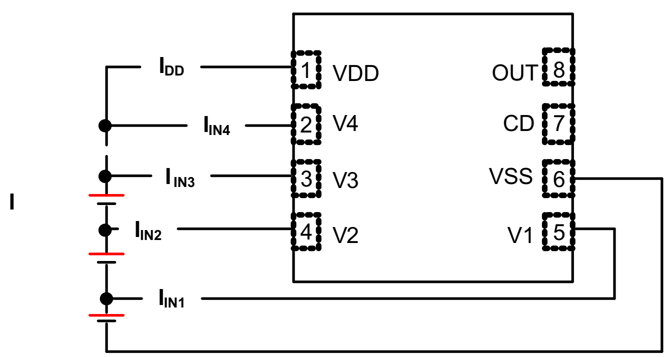
In these application examples of 2s and 3s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

CUSTOMER TEST MODE

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the $t_{(CD\_GND)}$ value, which has a maximum of 170 ms.

Figure 13 shows the timing for the Customer Test





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ294700DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	700	Samples
BQ294700DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	700	Samples
BQ294701DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	701	Samples
BQ294701DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	701	Samples
BQ294702DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	702	Samples
BQ294702DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	702	Samples
BQ294703DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	703	Samples
BQ294703DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	705 -40 to 85	703 [redacted]	Samples
BQ294704DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	704	Samples
BQ294704DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	704	Samples
BQ294705DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	705	Samples
BQ294705DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	705	Samples

(1) The marke(ACTIVE)] TJ ET Q q 1 0 0 1 162.254 303.503 cm q 0 0.25 m 56.692001 0

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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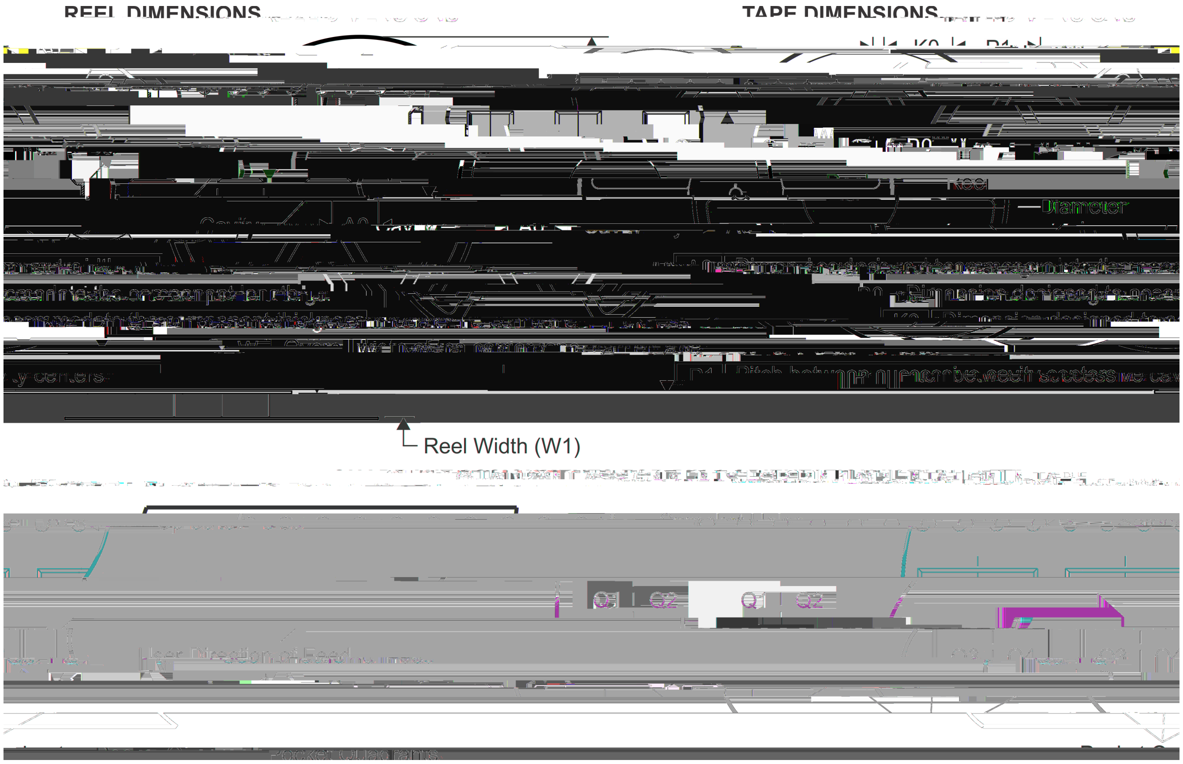
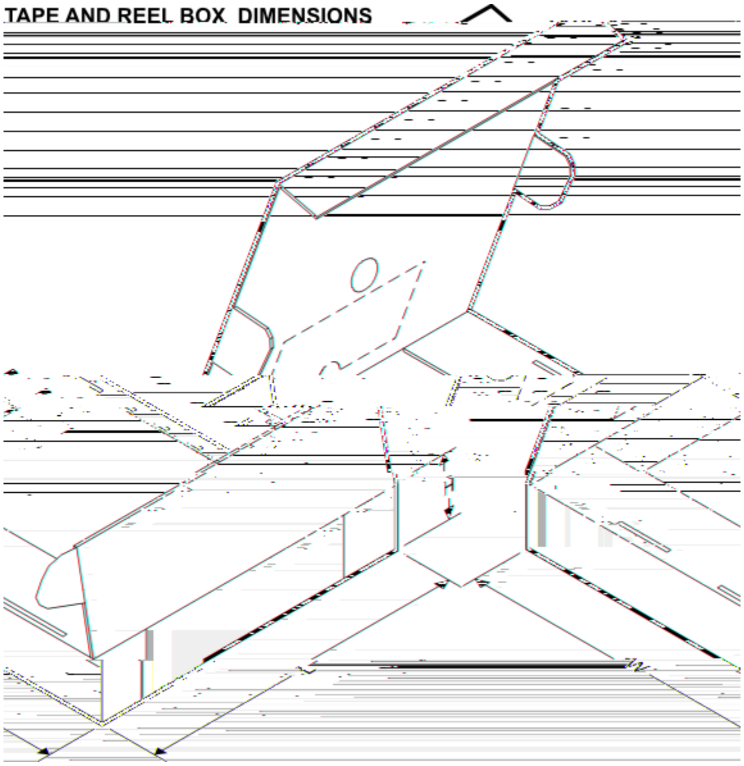


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294700DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294700DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294701DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294702DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294703DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294703DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294704DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294705DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

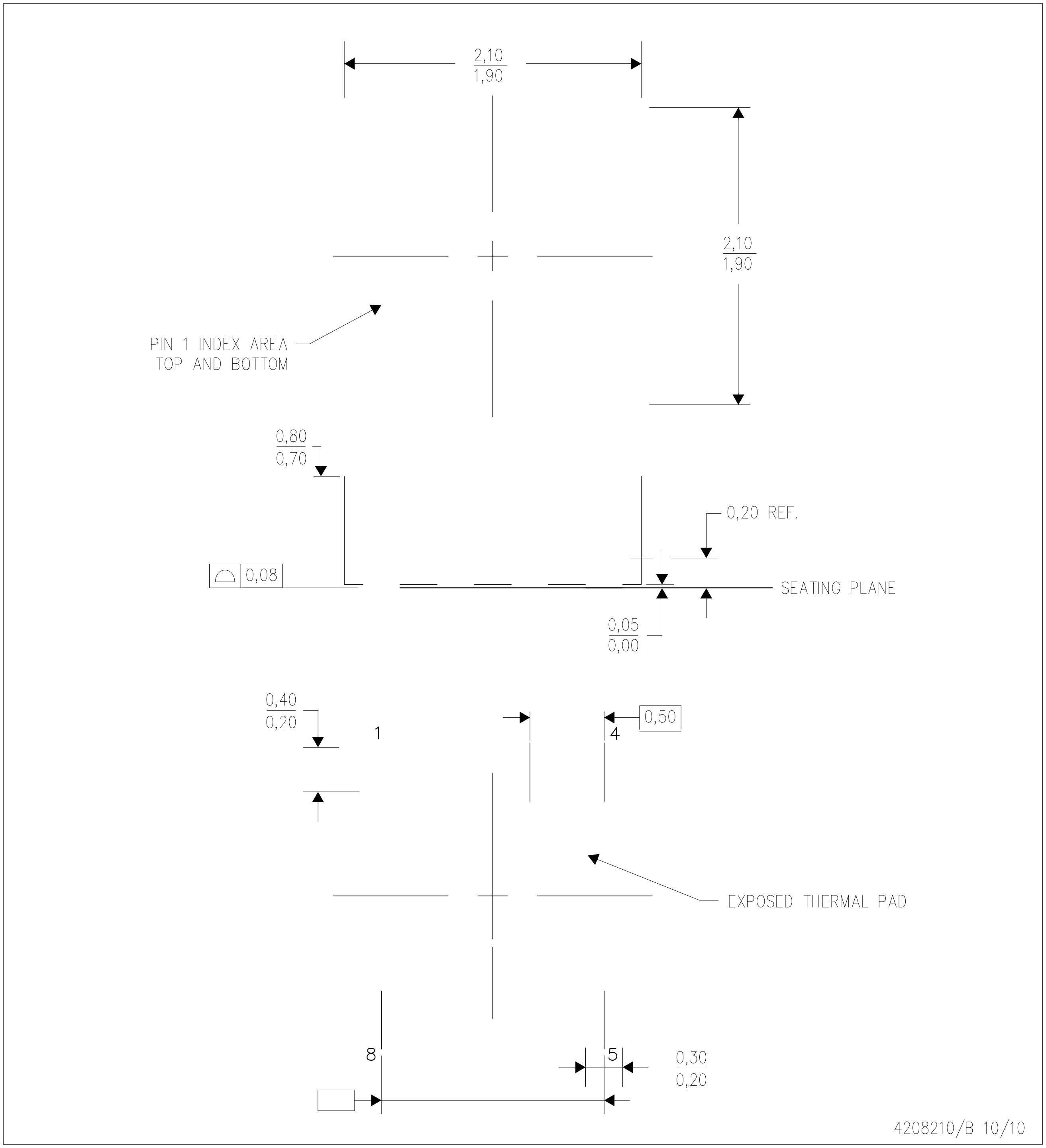


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294700DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294700DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294701DSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ294701DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ294702DSGR	WSON	DSG	8	3000	367.0	367.0	35.0

35.953 Tm [(35.0)] TJ ET q 0 T q 0 q 185.0

DSG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.

E. Falls within JEDEC MO—229.

DSG (S-PWSON-N8)

THERMAL INFORMATION

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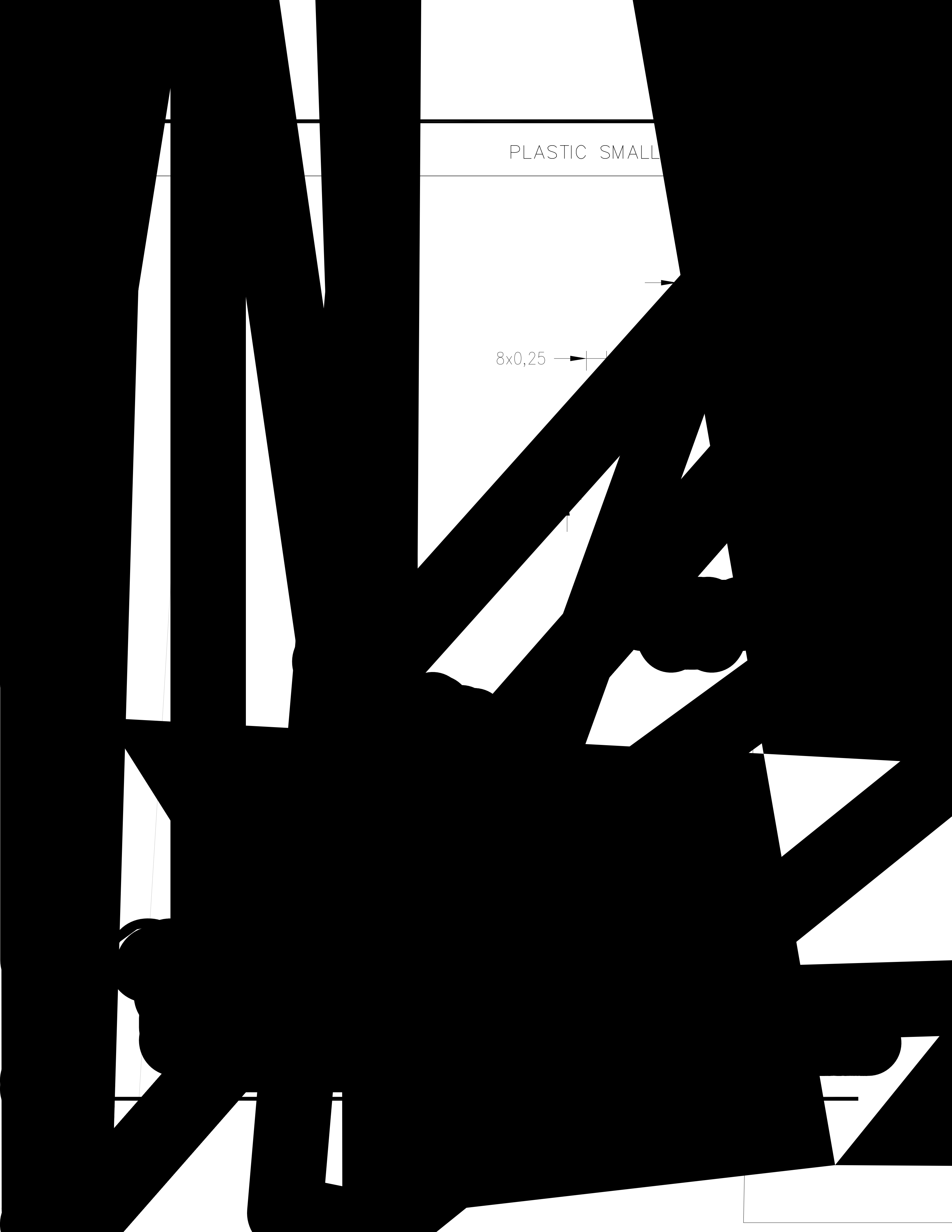
dditic

per plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink stru integrated circuit (IC).

QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

own in the following illustration.

4208347/E



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8x0,25

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