

## Low-Power Bidirectional I<sup>2</sup>C Isolators

Check for Samples: [ISO1540](#), [ISO1541](#)

### FEATURES

- Isolated Bidirectional, I<sup>2</sup>C Compatible, Communications
- Supports up to 1 MHz Operation
- 3-V to 5.5-V Supply Range
- Open Drain Outputs with 3.5-mA Side 1 and 35-mA Side 2 Sink Current Capability
- -40°C to 125°C Operating Temperature
- ±50 kV/μs Transient Immunity (Typical)
- HBM ESD Protection of 4 kV on All Pins; 8 kV on Bus Pins

### APPLICATIONS

- Isolated I<sup>2</sup>C Bus
- SMBus and PMBus Interfaces
- Open-drain Networks
- Motor Control Systems
- Battery Management
- I<sup>2</sup>C Level Shifting

### DESCRIPTION

The ISO1540 and ISO1541 are low-power, bidirectional isolators that are compatible with I<sup>2</sup>C interfaces. These devices have their logic input and output buffers separated by TI's Capacitive Isolation technology using a silicon dioxide (SiO<sub>2</sub>) barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

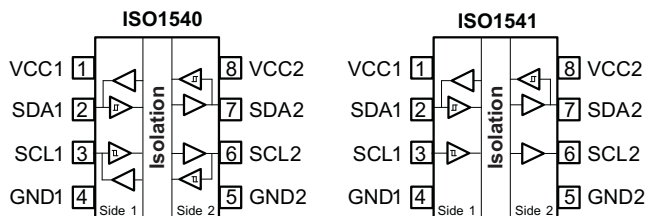
This isolation technology provides for function, performance, size, and power consumption advantages when compared to opto-couplers. The ISO1540 and ISO1541 enable a complete isolated I<sup>2</sup>C interface to be implemented within a small form factor.

The ISO1540 has two isolated bidirectional channels for clock and data lines while the ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single Master while the ISO1540 is ideally fit for multi-master applications.

Isolated bidirectional communications is accomplished within these devices by offsetting the Side 1 Low-Level Output Voltage to a value greater than the Side 1 High-Level Input Voltage thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

### SAFETY AND REGULATORY APPROVALS

- 4000-V<sub>PK</sub> Isolation per DIN EN 60747-5-2 (VDE 0884 Part 2) (Approved)
- 2500-V<sub>RMS</sub> Isolation for 1 minute per UL 1577 (Approved)
- CSA Component Acceptance Notice 5A (Approved)
- IEC 60950-1 and IEC 61010-1 End Equipment Standards (Approved)



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I<sup>2</sup>C is a trademark of NXP B.V. Corporation.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## PIN FUNCTIONS

| ISO1540 and ISO1541 | I / O      | DESCRIPTION |         |                                   |                                  |
|---------------------|------------|-------------|---------|-----------------------------------|----------------------------------|
|                     |            | ISO1540     | ISO1541 | ISO1540                           | ISO1541                          |
| <b>NAME</b>         | <b>PIN</b> |             |         |                                   |                                  |
| VCC1                | 1          | -           | -       | Supply Voltage, Side 1            | Supply Voltage, Side 1           |
| SDA1                | 2          | I / O       | I / O   | Serial Data, Side 1 Input/Output  | Serial Data, Side 1 Input/Output |
| SCL1                | 3          | I / O       | I       | Serial Clock Input/Output, Side 1 | Serial Clock Input, Side 1       |
| GND1                | 4          | -           | -       | Ground, Side 1                    | Ground, Side 1                   |
| GND2                | 5          | -           | -       | Ground, Side 2                    | Ground, Side 2                   |
| SCL2                | 6          | I / O       | O       | Serial Clock Input/Output, Side 2 | Serial Clock Output, Side 2      |
| SDA2                | 7          | I / O       | I / O   | Serial Data Input/Output, Side 2  | Serial Data Input/Output, Side 2 |
| VCC2                | 8          | -           | -       | Supply Voltage, Side 2            | Supply Voltage, Side 2           |

## AVAILABLE OPTIONS

| PRODUCT | RATED ISOLATION   | PACKAGE | CHANNEL DIRECTION                             | MARKED AS | ORDERING NUMBER                     |
|---------|---|---------|---|-----------|-------------------------------------|
| ISO1540 | 4000-V <sub>PK</sub> and 2500-V <sub>RMS</sub> <sup>(1)</sup> | D-8     | Both SDA and SCL are Bidirectional            | IS1540    | ISO1540D (rail)<br>ISO1540DR (reel) |
| ISO1541 |   |         | SDA is Bidirectional<br>SCL is Unidirectional | IS1541    | ISO1541D (rail)<br>ISO1541DR (reel) |

(1) See the Regulatory Information table for detailed Isolation specifications.

**Table 1. FUNCTION TABLE<sup>(1)</sup>**

| POWER STATE           | INPUT            | OUTPUT |
|-----------------------|------------------|--------|
| VCC1 or VCC2 < 2.1 V  | X                | Z      |
| VCC1 and VCC2 > 2.8 V | L                | L      |
| VCC1 and VCC2 > 2.8 V | H                | Z      |
| VCC1 and VCC2 > 2.8 V | Z <sup>(2)</sup> | ?      |

(1) H = High Level; L = Low Level; Z = High Impedance or Float; X = Irrelevant; ? = Indeterminate

(2) Invalid input condition as an I<sup>2</sup>C system requires that a pull-up resistor to VCC is connected.

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)(2)</sup>

|                         |                                    | VALUES                  |            | UNIT |    |
|-------------------------|------------------------------------|-------------------------|------------|------|----|
|                         |                                    | MIN                     | MAX        |      |    |
| Supply voltage          | VCC1, VCC2                         | -0.5                    | 6          | V    |    |
|                         | SDA1, SCL1                         | -0.5                    | VCC1 + 0.5 | V    |    |
|                         | SDA2, SCL2                         | -0.5                    | VCC2 + 0.5 | V    |    |
| Output current          | SDA1, SCL1                         |                         | ±20        | mA   |    |
|                         | SDA2, SCL2                         |                         | ±100       | mA   |    |
| Electrostatic Discharge | Human Body Model                   | ESDA, JEDEC JS-001-2012 | Bus Pins   | ±8   | kV |
|                         |                                    |                         | All Pins   | ±4   |    |
|                         | Field-Induced-Charged Device Model | JEDEC JESD22-C101E      | All Pins   | ±1.5 | kV |
|                         | Machine Model                      | JEDEC JESD22-A115-A     |            | ±200 | V  |
| T <sub>J(MAX)</sub>     | Maximum junction temperature       |                         |            | 150  | °C |
| T <sub>STG</sub>        | Storage temperature range          |                         | -65        | 150  | °C |

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute-maximum-rated conditions for extended periods affects device reliability.
- All voltage values here within are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

**THERMAL INFORMATION**

| THERMAL METRIC <sup>(1)</sup> |  | ISO1540<br>ISO1541 | UNITS |
|-------------------------------|--|--------------------|-------|
|                               |  | D (8 PINS)         |       |
| θ <sub>JA</sub>               | Junction-to-ambient thermal resistance       | 114.6              | °C/W  |
| θ <sub>JCtop</sub>            | Junction-to-case (top) thermal resistance    | 69.6               |       |
| θ <sub>JB</sub>               | Junction-to-board thermal resistance         | 55.3               |       |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 27.2               |       |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 54.7               |       |
| θ <sub>JCbot</sub>            | Junction-to-case (bottom) thermal resistance | n/a                |       |

- For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

**RECOMMENDED OPERATING CONDITIONS**

|                                       |  | MIN        | NOM | MAX        | UNIT |
|---------------------------------------|--|------------|-----|------------|------|
| VCC1, VCC2                            | Supply Voltage                             | 3          |     | 5.5        | V    |
| V <sub>SDA1</sub> , V <sub>SCL1</sub> | Input/Output Signal Voltages, Side 1       | 0          |     | VCC1       |      |
| V <sub>SDA2</sub> , V <sub>SCL2</sub> | Input/Output Signal Voltages, Side 2       | 0          |     | VCC2       |      |
| V <sub>IL1</sub>                      | Low-Level Input Voltage, Side 1            | 0          |     | 0.5        |      |
| V <sub>IH1</sub>                      | High-Level Input Voltage, Side 1           | 0.7 x VCC1 |     | VCC1       |      |
| V <sub>IL2</sub>                      | Low-Level Input Voltage, Side 2            | 0          |     | 0.3 x VCC2 |      |
| V <sub>IH2</sub>                      | High-Level Input Voltage, Side 2           | 0.7 x VCC2 |     | VCC2       |      |
| I <sub>OL1</sub>                      | Output Current, Side 1                     | 0.5        |     | 3.5        | mA   |
| I <sub>OL2</sub>                      | Output Current, Side 2                     | 0.5        |     | 35         |      |
| C <sub>b1</sub>                       | Maximum Capacitive Load, Side 1            |            |     | 40         | pF   |
| C <sub>b2</sub>                       | Maximum Capacitive Load, Side 2            |            |     | 400        |      |
| f <sub>MAX</sub>                      | Maximum Operating Frequency <sup>(1)</sup> |            |     | 1          | MHz  |
| T <sub>A</sub>                        | Ambient Temperature                        | -40        |     | 125        | °C   |
| T <sub>J</sub>                        | Junction Temperature                       | -40        |     | 136        | °C   |
| T <sub>SD</sub>                       | Thermal Shutdown                           | 139        |     | 171        | °C   |

- This represents the maximum frequency with the maximum bus load (C<sub>b</sub>) and the maximum current sink (I<sub>O</sub>). If the system has less bus capacitance, then higher frequencies can be achieved.

## ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted

| PARAMETER  |  | TEST CONDITIONS        |   | MIN   | TYP | MAX           | UNIT  |    |
|--|--|------------------------|---|---|-----|---------------|-------|----|
| <b>SUPPLY CURRENT (3V ≤ VCC1, VCC2 ≤ 3.6V)</b>     |  |                        |   |   |     |               |       |    |
| I <sub>CC1</sub>                                   | Supply Current, Side 1   | ISO1540                | V <sub>SDA1</sub> ,<br>V <sub>SCL1</sub> = GND1;  | See <a href="#">Figure 1</a> ;<br>R <sub>1</sub> , R <sub>2</sub> = Open,<br>C <sub>1</sub> , C <sub>2</sub> = Open | 2.4 | 3.6           | mA    |    |
|  |  | ISO1541                |   |   | 2.1 | 3.3           |       |    |
| I <sub>CC2</sub>                                   | Supply Current, Side 2   | ISO1540 and<br>ISO1541 | V <sub>SDA2</sub> ,<br>V <sub>SCL2</sub> = GND2   | 1.7   | 2.7 |               |       |    |
| I <sub>CC1</sub>                                   | Supply Current, Side 1   | ISO1540                | V <sub>SDA1</sub> ,<br>V <sub>SCL1</sub> = VCC1;  | 2.5   | 3.8 |               |       |    |
|  |  | ISO1541                |   | 2.3   | 3.6 |               |       |    |
| I <sub>CC2</sub>                                   | Supply Current, Side 2   | ISO1540 and<br>ISO1541 | V <sub>SDA2</sub> ,<br>V <sub>SCL2</sub> = VCC2   | 1.9   | 3.1 |               |       |    |
| <b>SUPPLY CURRENT (4.5 V ≤ VCC1, VCC2 ≤ 5.5 V)</b> |  |                        |   |   |     |               |       |    |
| I <sub>CC1</sub>                                   | Supply Current, Side 1   | ISO1540                | V <sub>SDA1</sub> ,<br>V <sub>SCL1</sub> = GND1;  | See <a href="#">Figure 1</a> ;<br>R <sub>1</sub> , R <sub>2</sub> = Open,<br>C <sub>1</sub> , C <sub>2</sub> = Open | 3.1 | 4.7           |       | mA |
|  |  | ISO1541                |   |   | 2.8 | 4.4           |       |    |
| I <sub>CC2</sub>                                   | Supply Current, Side 2   | ISO1540 and<br>ISO1541 | V <sub>SDA2</sub> ,<br>V <sub>SCL2</sub> = GND2   | 2.3   | 3.7 |               |       |    |
| I <sub>CC1</sub>                                   | Supply Current, Side 1   | ISO1540                | V <sub>SDA1</sub> ,<br>V <sub>SCL1</sub> = VCC1;  | 3.1   | 4.7 |               |       |    |
|  |  | ISO1541                |   | 2.9   | 4.5 |               |       |    |
| I <sub>CC2</sub>                                   | Supply Current, Side 2   | ISO1540 and<br>ISO1541 | V <sub>SDA2</sub> ,<br>V <sub>SCL2</sub> = VCC2   | 2.5   | 4   |               |       |    |
| PARAMETER  |  | TEST CONDITIONS        |   | MIN   | TYP | MAX           | UNIT  |    |
| <b>SIDE 1 (Only)</b>                               |  |                        |   |   |     |               |       |    |
| V <sub>ILT1</sub>                                  | Voltage Input Threshold “Low”,<br>Side 1 (SDA1, SCL1)  |                        |   | 500   | 550 | 660           | mV    |    |
| V <sub>IHT1</sub>                                  | Voltage Input Threshold “High”,<br>Side 1 (SDA1, SCL1)   |                        |   | 540   | 610 | 700           |       |    |
| V <sub>HYST1</sub>                                 | Voltage Input Hysteresis,<br>Side 1 V <sub>IHT1</sub> - V <sub>ILT1</sub>                            |                        |   | 40  | 60  |               |       |    |
| V <sub>OL1</sub> <sup>(1)</sup>                    | Low-Level Output Voltage,<br>Side 1 (SDA1, SCL1)   |                        | 0.5 mA ≤ (I <sub>SDA1</sub> and<br>I <sub>SCL1</sub> ) ≤ 3.5 mA                               | 650   |     | 800           |       |    |
| ΔV <sub>OIT1</sub> <sup>(1)(2)</sup>               | Low-Level Output Voltage to High-Level Input Voltage<br>Threshold Difference,<br>Side 1 (SDA1, SCL1) |                        |   | 50  |     |               |       |    |
| <b>SIDE 2 (Only)</b>                               |  |                        |   |   |     |               |       |    |
| V <sub>ILT2</sub>                                  | Voltage Input Threshold “Low”,<br>Side 2 (SDA2, SCL2)  |                        |   | 0.3 x<br>VCC2   |     | 0.4 x<br>VCC2 | mV    |    |
| V <sub>IHT2</sub>                                  | Voltage Input Threshold “High”,<br>Side 2 (SDA2, SCL2)   |                        |   | 0.4 x<br>VCC2   |     | 0.5 x<br>VCC2 |       |    |
| V <sub>HYST2</sub>                                 | Voltage Input Hysteresis,<br>Side 2 V <sub>IHT2</sub> - V <sub>ILT2</sub>                            |                        |   | 0.05 x<br>VCC2  |     |               |       |    |
| V <sub>OL2</sub>                                   | Low-Level Output Voltage,<br>Side 2 (SDA2, SCL2)   |                        | 0.5 mA ≤ (I <sub>SDA2</sub> and<br>I <sub>SCL2</sub> ) ≤ 35 mA                                |   |     | 400           |       |    |
| <b>BOTH SIDES</b>                                  |  |                        |   |   |     |               |       |    |
| I <sub>l</sub>                                     | Input Leakage Currents<br>(SDA1, SCL1, SDA2, SCL2)   |                        | V <sub>SDA1</sub> , V <sub>SCL1</sub> = VCC1;<br>V <sub>SDA2</sub> , V <sub>SCL2</sub> = VCC2 | 0.01  |     | 10            | μA    |    |
| C <sub>1</sub>                                     | Input Capacitance to Local Ground<br>(SDA1, SCL1, SDA2, SCL2)  |                        | V <sub>l</sub> = 0.4 x sin(2E6πt) +<br>2.5 V  |   | 7   |               | pF    |    |
| CMTI   | Common-Mode Transient Immunity   |                        | See <a href="#">Figure 3</a>  | 25  | 50  |               | kV/μs |    |
| V <sub>CCUV</sub> <sup>(3)</sup>                   | V <sub>CC</sub> Undervoltage Lockout Threshold<br>(Side 1 and Side 2)                                |                        |   | 2.1   | 2.5 | 2.8           | V     |    |

(1) This parameter does not apply to the ISO1541 SCL1 line as it is uni-directional.

(2) ΔV<sub>OIT1</sub> = V<sub>OL1</sub> - V<sub>IHT1</sub>. This represents the minimum difference between a Low-Level Output Voltage and a High-Level Input Voltage Threshold to prevent a permanent latch condition that would otherwise exist with bi-directional communication.

(3) Any V<sub>CC</sub> voltages, on either side, less than the minimum will ensure device lockout. Both V<sub>CC</sub> voltages above the maximum will prevent device lockout.

## SWITCHING CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted

| PARAMETER                          |   | TEST CONDITIONS  | MIN  | TYP                 | MAX | UNIT |     |    |
|------------------------------------|---|--|--|---------------------|-----|------|-----|----|
| <b>3 V ≤ VCC1, VCC2 ≤ 3.6 V</b>    |   |  |  |                     |     |      |     |    |
| t <sub>f1</sub>                    | Output Signal Fall Time (SDA1, SCL1)                              | See <a href="#">Figure 1</a><br>R <sub>1</sub> = 953 Ω,<br>C <sub>1</sub> = 40 pF  | 0.7 x VCC1 to 0.3 x VCC1   |                     | 8   | 17   | 29  | ns |
|                                    |   |  | 0.9 x VCC1 to 900 mV   |                     | 16  | 29   | 48  |    |
| t <sub>f2</sub>                    | Output Signal Fall Time (SDA2, SCL2)                              | See <a href="#">Figure 1</a><br>R <sub>2</sub> = 95.3 Ω,<br>C <sub>2</sub> = 400 pF  | 0.7 x VCC2 to 0.3 x VCC2   |                     | 14  | 23   | 47  | ns |
|                                    |   |  | 0.9 x VCC2 to 400 mV   |                     | 35  | 50   | 100 |    |
| t <sub>pLH1-2</sub>                | Low-to-High Propagation Delay, Side 1 to Side 2                   | See <a href="#">Figure 1</a><br>R <sub>1</sub> = 953 Ω,<br>R <sub>2</sub> = 95.3 Ω,<br>C <sub>1</sub> , C <sub>2</sub> = 10 pF | 0.55 V to 0.7 x VCC2   |                     | 33  | 65   | ns  |    |
| t <sub>pHL1-2</sub>                | High-to-Low Propagation Delay, Side 1 to Side 2                   |  | 0.7 V to 0.4 V   |                     | 90  | 181  | ns  |    |
| PWD <sub>1-2</sub>                 | Pulse Width Distortion  t <sub>pHL1-2</sub> - t <sub>pLH1-2</sub> |  |  |                     | 55  | 123  | ns  |    |
| t <sub>PLH2-1</sub> <sup>(1)</sup> | Low-to-High Propagation Delay, Side 2 to Side 1                   |  | 0.4 x VCC2 to 0.7 x VCC1   |                     | 47  | 68   | ns  |    |
| t <sub>PHL2-1</sub> <sup>(1)</sup> | High-to-Low Propagation Delay, Side 2 to Side 1                   |  | 0.4 x VCC2 to 0.9 V  |                     | 67  | 109  | ns  |    |
| PWD <sub>2-1</sub> <sup>(1)</sup>  | Pulse Width Distortion  t <sub>pHL2-1</sub> - t <sub>pLH2-1</sub> |  |  |                     | 20  | 49   | ns  |    |
| t <sub>LOOP1</sub> <sup>(1)</sup>  | Round-trip propagation delay on Side 1                            |  | See <a href="#">Figure 2</a> ;<br>R <sub>1</sub> = 953 Ω, C <sub>1</sub> = 40 pF<br>R <sub>2</sub> = 95.3 Ω, C <sub>2</sub> = 400 pF | 0.4 V to 0.3 x VCC1 |     | 100  | 165 | ns |
| <b>4.5V ≤ VCC1, VCC2 ≤ 5.5V</b>    |   |  |  |                     |     |      |     |    |
| t <sub>f1</sub>                    | Output Signal Fall Time (SDA1, SCL1)                              | See <a href="#">Figure 1</a><br>R <sub>1</sub> = 1430 Ω,<br>C <sub>1</sub> = 40 pF   | 0.7 x VCC1 to 0.3 x VCC1   |                     | 6   | 11   | 20  | ns |
|                                    |   |  | 0.9 x VCC1 to 900 mV   |                     | 13  | 21   | 39  |    |
| t <sub>f2</sub>                    | Output Signal Fall Time (SDA2, SCL2)                              | See <a href="#">Figure 1</a><br>R <sub>2</sub> = 143 Ω,<br>C <sub>2</sub> = 400 pF   | 0.7 x VCC2 to 0.3 x VCC2   |                     | 10  | 18   | 35  | ns |
|                                    |   |  | 0.9 x VCC2 to 400 mV   |                     | 28  | 41   | 76  |    |
| t <sub>pLH1-2</sub>                | Low-to-High Propagation Delay, Side 1 to Side 2                   | See <a href="#">Figure 1</a><br>R <sub>1</sub> = 1430 Ω,<br>R <sub>2</sub> = 143 Ω,<br>C <sub>1</sub> , C <sub>2</sub> = 10 pF | 0.55 V to 0.7 x VCC2   |                     | 31  | 62   | ns  |    |
| t <sub>pHL1-2</sub>                | High-to-Low Propagation Delay, Side 1 to Side 2                   |  | 0.7 V to 0.4 V   |                     | 70  | 139  | ns  |    |
| PWD <sub>1-2</sub>                 | Pulse Width Distortion  t <sub>pHL1-2</sub> - t <sub>pLH1-2</sub> |  |  |                     | 38  | 80   | ns  |    |
| t <sub>PLH2-1</sub> <sup>(1)</sup> | Low-to-High Propagation Delay, Side 2 to Side 1                   |  | 0.4 x VCC2 to 0.7 x VCC1   |                     | 55  | 80   | ns  |    |
| t <sub>PHL2-1</sub> <sup>(1)</sup> | High-to-Low Propagation Delay, Side 2 to Side 1                   |  | 0.4 x VCC2 to 0.9 V  |                     | 47  | 85   | ns  |    |
| PWD <sub>2-1</sub> <sup>(1)</sup>  | Pulse Width Distortion  t <sub>pHL2-1</sub> - t <sub>pLH2-1</sub> |  |  |                     | 8   | 21   | ns  |    |
| t <sub>LOOP1</sub> <sup>(1)</sup>  | Round-trip propagation delay on Side 1                            |  | See <a href="#">Figure 2</a> ;<br>R <sub>1</sub> = 1430 Ω, C <sub>1</sub> = 40 pF<br>R <sub>2</sub> = 143 Ω, C <sub>2</sub> = 400 pF | 0.4 V to 0.3 x VCC1 |     | 110  | 180 | ns |

(1) This parameter does not apply to the ISO1541 SCL1 line as it is uni-directional.

## TIMING CHARACTERISTICS

| PARAMETER         |   | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----|-----|-----|------|
| t <sub>SP</sub>   | Input Noise Filter                                |  | 5   | 12  |     | ns   |
| t <sub>UVLO</sub> | Time to recover from <i>Undervoltage Lock-out</i> | See <a href="#">Figure 4</a><br>2.7 V to 0.9 V | 30  | 50  | 110 | μs   |

PARAMETER MEASUREMENT INFORMATION

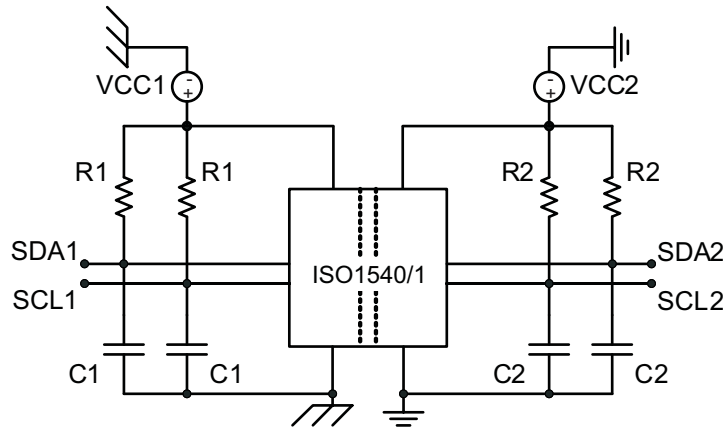


Figure 1. Test Diagram

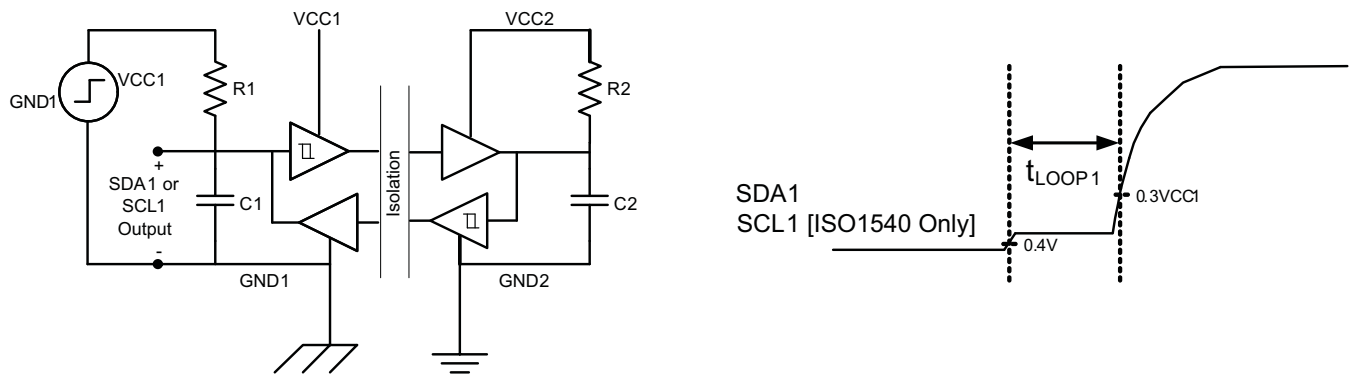


Figure 2.  $t_{Loop1}$  Setup and Timing Diagram

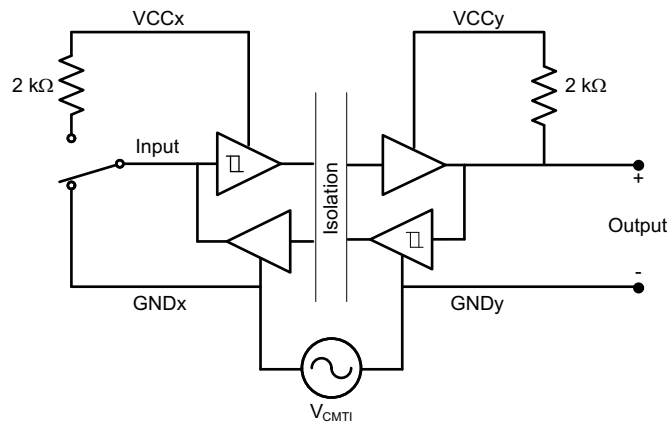
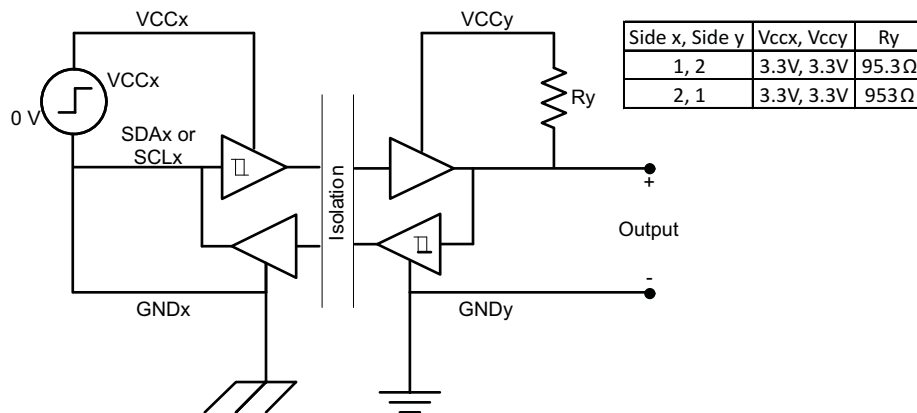


Figure 3. Common-Mode Transient Immunity Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



or

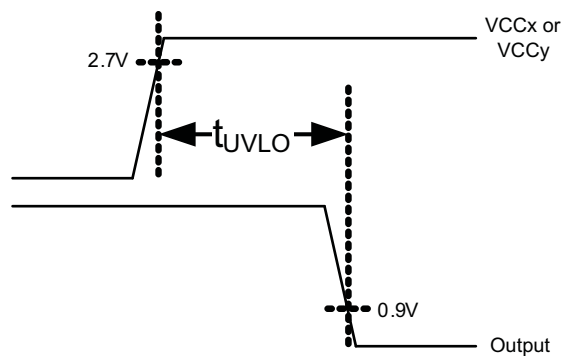
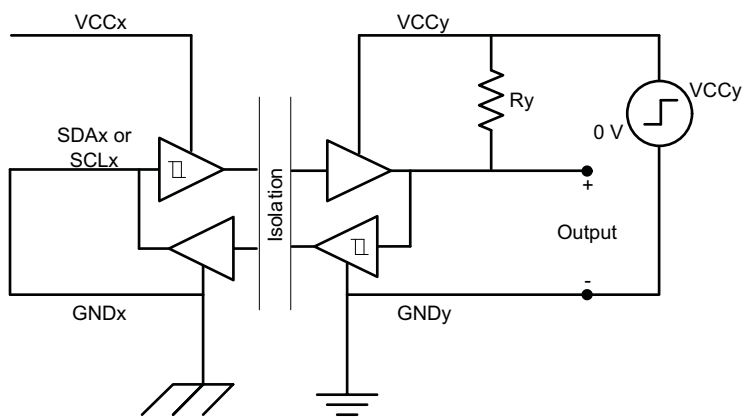


Figure 4.  $t_{UVLO}$  Test Circuit and Timing Diagrams

**DEVICE INFORMATION**

**Table 2. IEC INSULATION AND SAFETY-RELATED SPECIFICATION FOR D-8 PACKAGE  
Over recommended operating conditions, unless otherwise noted**

| PARAMETER       |  | TEST CONDITIONS   | MIN                            | TYP               | MAX | UNIT |
|-----------------|--|---|--------------------------------|-------------------|-----|------|
| L(I01)          | Minimum air gap (Clearance)                          | Shortest terminal-to-terminal distance through air                | 4.8                            |                   |     | mm   |
| L(I02)          | Minimum external tracking (Creepage)                 | Shortest terminal-to-terminal distance across the package surface | 4.3                            |                   |     | mm   |
| CTI             | Tracking resistance (comparative tracking index)     | DIN IEC 60112 / VDE 0303 Part 1                                   | >400                           |                   |     | V    |
|                 | Minimum internal gap (internal clearance)            | Distance through the insulation                                   | 0.014                          |                   |     | mm   |
| R <sub>IO</sub> | Isolation resistance, input to output <sup>(1)</sup> | V <sub>IO</sub> = 500 V, T <sub>A</sub> < 100°C                   |                                | >10 <sup>12</sup> |     | Ω    |
|                 |  | V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub>                   |                                | >10 <sup>11</sup> |     | Ω    |
| C <sub>IO</sub> | Barrier capacitance, input to output <sup>(1)</sup>  | V <sub>IO</sub> = 0.4 x sin(2E6πt)                                |                                | 1                 |     | pF   |
| C <sub>I</sub>  | Input capacitance <sup>(2)</sup>                     |   | See Electrical Characteristics |                   |     | pF   |

- (1) All pins on each side of the barrier tied together creating a two-terminal device.
- (2) Measured from input pin to ground.

**NOTE**

Creepage and clearance requirements should be applied according to the specific application isolation standards. Care should be taken to maintain these distances on a board design to ensure that the mounting pads for the isolator do not reduce this distance.

Creepage and clearance on the printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on the printed circuit board are used to help increase these specifications.

**Table 3. IEC 60747-5-2 INSULATION CHARACTERISTICS<sup>(1)</sup>  
Over recommended operating conditions, unless otherwise noted**

| PARAMETER         | TEST CONDITIONS                                | SPECIFICATION   | UNIT              |      |
|-------------------|--|---|-------------------|------|
| V <sub>IORM</sub> | Maximum working insulation voltage             | 566   | V <sub>PEAK</sub> |      |
| V <sub>PR</sub>   | Input-to-Output test voltage per IEC 60747-5-2 | Method a, After environmental tests subgroup 1, V <sub>PR</sub> = V <sub>IORM</sub> x 1.6, t = 10 sec, Partial Discharge < 5 pC                     |                   | 906  |
|                   |  | Method b1, After environmental tests subgroup 1, V <sub>PR</sub> = V <sub>IORM</sub> x 1.875, t = 1 sec (100% production), Partial Discharge < 5 pC |                   | 1062 |
|                   |  | After Input/Output safety test subgroup 2/3, V <sub>PR</sub> = V <sub>IORM</sub> x 1.2, t = 10 sec, Partial Discharge < 5 pC                        |                   | 680  |
| V <sub>IOTM</sub> | Transient overvoltage per IEC 60747-5-2        | V <sub>TEST</sub> = V <sub>OITM</sub><br>t = 60 sec (qualification)<br>t = 1 sec (100% production)  | 4000              |      |
| R <sub>S</sub>    | Insulation resistance                          | V <sub>IO</sub> = 500 V at T <sub>S</sub>   | >10 <sup>9</sup>  | Ω    |
|                   | Pollution degree                               |   | 2                 |      |

- (1) Climatic Classification 40/125/21



**Table 4. IEC 60664-1 RATINGS TABLE**

| PARAMETER                   | TEST CONDITIONS                        | SPECIFICATION |
|-----------------------------|--|---------------|
| Basic isolation group       | Material group                         | II            |
| Installation classification | Rated mains voltage $\leq 150 V_{RMS}$ | I–IV          |
|                             | Rated mains voltage $\leq 300 V_{RMS}$ | I–III         |
|                             | Rated mains voltage $\leq 400 V_{RMS}$ | I–II          |

**Table 5. REGULATORY INFORMATION**

| VDE   | CSA  | UL   |
|---|--|--|
| Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2) and EN 61010-1  | Approved under CSA Component Acceptance Notice 5A, CSA/IEC 60950-1 and CSA/IEC 61010-1   | Recognized under UL 1577 Component Recognition Program             |
| Basic Insulation<br>Maximum Transient Overvoltage, 4000 $V_{PK}$<br>Maximum Surge Voltage, 4000 $V_{PK}$<br>Maximum Working Voltage, 566 $V_{PK}$ | Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 390 $V_{RMS}$ maximum working voltage<br>Basic insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Ed), 300 $V_{RMS}$ maximum working voltage<br>Reinforced insulation per CSA 61010-1-04 and IEC 61010-1 (2nd Ed), 150 $V_{RMS}$ maximum working voltage | Single Protection Isolation Voltage, 2500 $V_{RMS}$ <sup>(1)</sup> |
| File number: 40016131   | File number: 220991  | File number: E181974   |

(1) Production tested  $\geq 3000 V_{RMS}$  for 1 second in accordance with UL 1577.

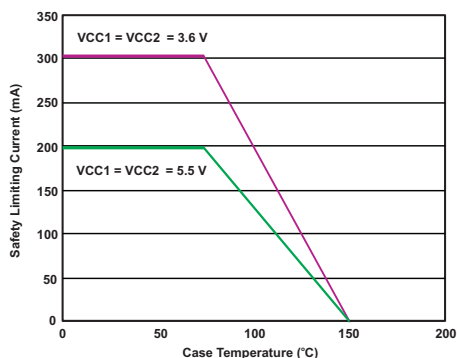
**IEC SAFETY LIMITING VALUES**

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER                                     | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |                  |
|---|---|-----|-----|-----|------|------------------|
| $I_S$ Safety input, output, or supply current | D-8<br>$\theta_{JA} = 114.6^\circ\text{C/W}$ , $V_I = 5.5\text{V}$ , $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$ |     |     |     | 198  | mA               |
|   |   |     |     |     | 303  |                  |
| $T_S$ Maximum case temperature                |   |     |     |     | 150  | $^\circ\text{C}$ |

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

**ISO154x THERMAL DERATING**



**Figure 5.**

## APPLICATION INFORMATION

### I<sup>2</sup>C™ Bus Overview

The I<sup>2</sup>C (Inter-Integrated Circuit) bus is a single-ended, multi-master, 2-wire bus for efficient inter-IC communication in half-duplex mode.

I<sup>2</sup>C uses open-drain technology, requiring two lines, Serial Data (SDA) and Serial Clock (SCL), to be connected to VDD by resistors (see Figure 6). Pulling the line to ground is considered a logic Zero while letting the line float is a logic One. This is used as a channel access method. Transitions of logic states must occur while SCL is Low, transitions while SCL is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are permitted.

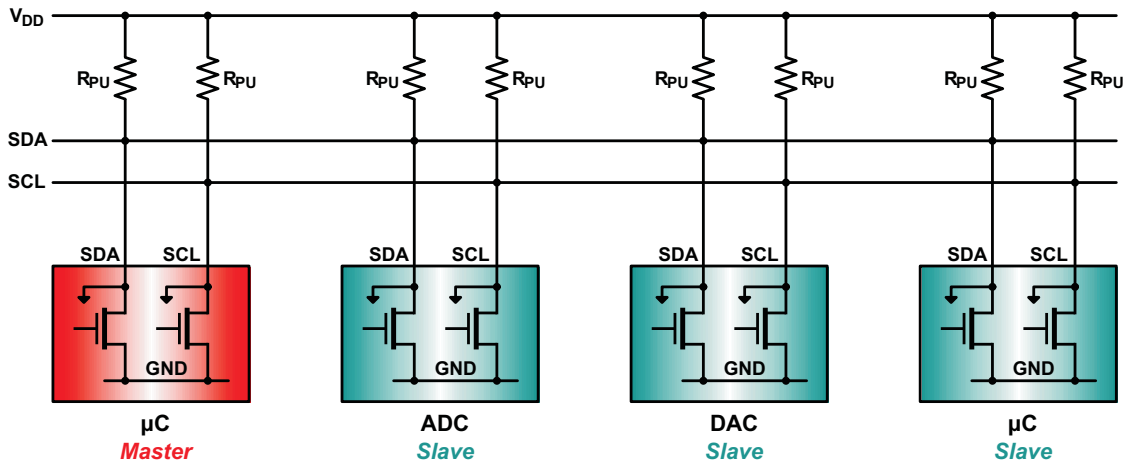


Figure 6. I<sup>2</sup>C BUS

I<sup>2</sup>C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified, total bus capacitance of 400 pF, which restricts communication distances to a few meters.

The specified signaling rates for the ISO1540 and ISO1541 are 100 kbps (Standard mode), 400 kbps (Fast mode), 1 Mbps (Fast mode plus).

The bus has two roles for nodes: master and slave. A master node issues the clock, slave addresses, and also initiates and ends data transactions. A slave node receives the clock and addresses and responds to requests from the master. Figure 7 shows a typical data transfer between master and slave.

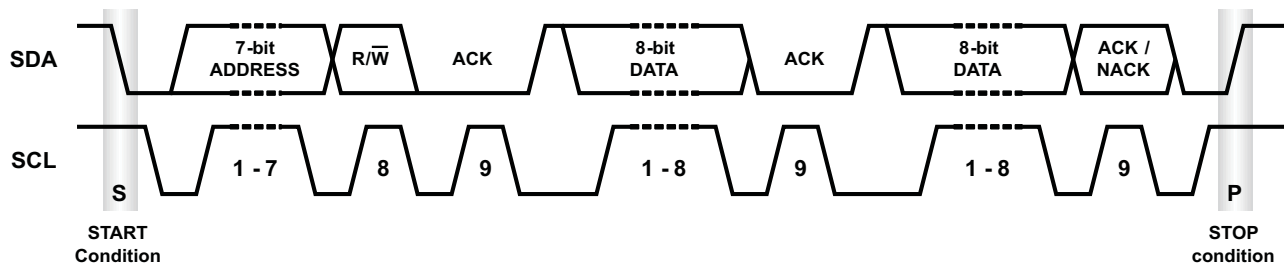


Figure 7. Timing Diagram of a Complete Data Transfer

The master initiates a transaction by creating a START condition, following by the 7-bit address of the slave it wishes to communicate with. This is followed by a single Read/Write bit, representing whether the master wishes to write to (0), or to read from (1) the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge bit (ACK) by pulling SDA low during the entire high time of the 9th clock pulse on SCL, after which the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and the 8-bit data bytes are sent most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte with the slave sending an ACK bit. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave, while acknowledging (ACK) the receipt of every byte but the last one (see Figure 8). In this situation the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit, or may send another START bit to maintain bus control for further transfers.

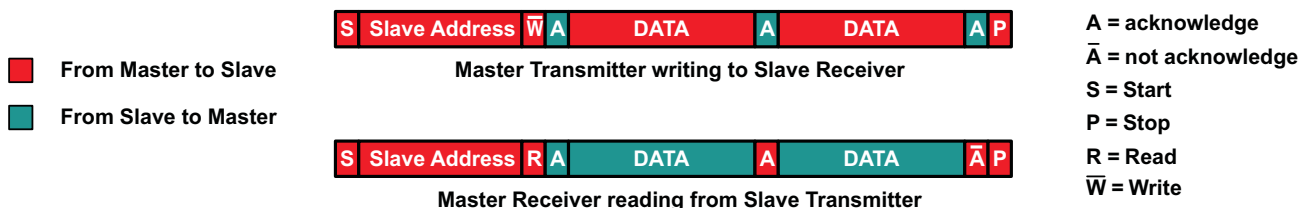


Figure 8. Transmit or Receive Mode Changes During a Data Transfer

When writing to a slave, a master mainly operates in transmit-mode and only changes to receive-mode when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit-mode and then changes to receive-mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note, that the master ends a reading sequence by not acknowledging (NACK) the last byte received. This procedure resets the slave state machine and allows the master to send the STOP command.

### Isolator Functional Principle

To isolate a bidirectional signal path (SDA or SCL), the ISO1540 internally splits a bidirectional line into two unidirectional signal lines, each of which is isolated via a single-channel digital isolator. Each channel output is made open-drain to comply with the open-drain technology of I<sup>2</sup>C. Side 1 of the ISO1540 connects to a low-capacitance I<sup>2</sup>C node, while Side 2 is designed for connecting to a fully loaded I<sup>2</sup>C bus with up to 400 pF capacitance.

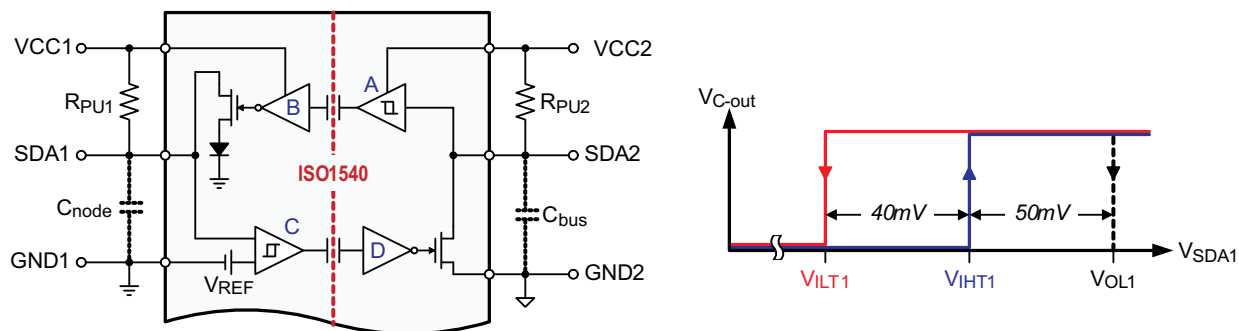


Figure 9. SDA Channel Design and Voltage Levels at SDA1

At first sight, the arrangement of the internal buffers suggests a closed signal loop that is prone to latch-up. However, this loop is broken by implementing an output buffer (B) whose output low-level is raised by a diode drop to approximately 0.75 V, and the input buffer (C) that consists of a comparator with defined hysteresis. The comparator's upper and lower input thresholds then distinguish between the proper low-potential of 0.4 V maximum driven directly by SDA1 and the buffered output low-level of B.

Figure 10 demonstrate the switching behavior of the I<sup>2</sup>C isolator, ISO1540, between a master node at SDA1 and a heavy loaded bus at SDA2

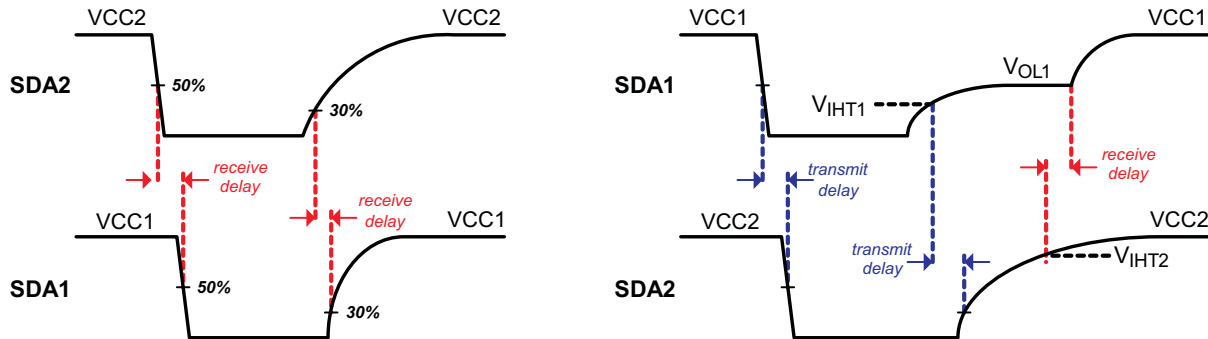


Figure 10. SDA Channel Timing in Receive and Transmit Directions

### Receive Direction (left diagram)

When the I<sup>2</sup>C bus drives SDA2 low, SDA1 follows after a certain delay in the receive path. Its output low will be the buffered output of  $V_{OL1} = 0.75\text{ V}$ , which is sufficiently low to be detected by Schmitt-trigger inputs with a minimum input-low voltage of  $V_{IL} = 0.9\text{ V}$  at 3 V supply levels.

Once SDA2 is released, its voltage potential increases towards  $V_{CC2}$  following the time-constant formed by  $R_{PU2}$  and  $C_{bus}$ . After the receive delay, SDA1 is released and also rises towards  $V_{CC1}$ , following the time-constant  $R_{PU1} \times C_{node}$ . Because of the significant lower time-constant, SDA1 may reach  $V_{CC1}$  before SDA2 reaches  $V_{CC2}$  potential.

### Transmit Direction (right diagram)

When a master drives SDA1 low, SDA2 follows after a certain delay in the transmit direction. When SDA2 turns low it also causes the output of buffer B to turn low but at a higher 0.75 V level. This level cannot be observed immediately as it is overwritten by the master's lower low-level.

However, when the master releases SDA1, its voltage potential increases and first must pass the upper input threshold of the comparator,  $V_{IHT1}$ , to release SDA2. SDA1 then increases further until it reaches the buffered output level of  $V_{OL1} = 0.75\text{ V}$ , maintained by the receive path. Once comparator C turns high, SDA2 is released after the delay in transmit direction. It takes another receive delay until B's output turns high and fully releases SDA1 to move towards  $V_{CC1}$  potential.

### Typical Application Circuit

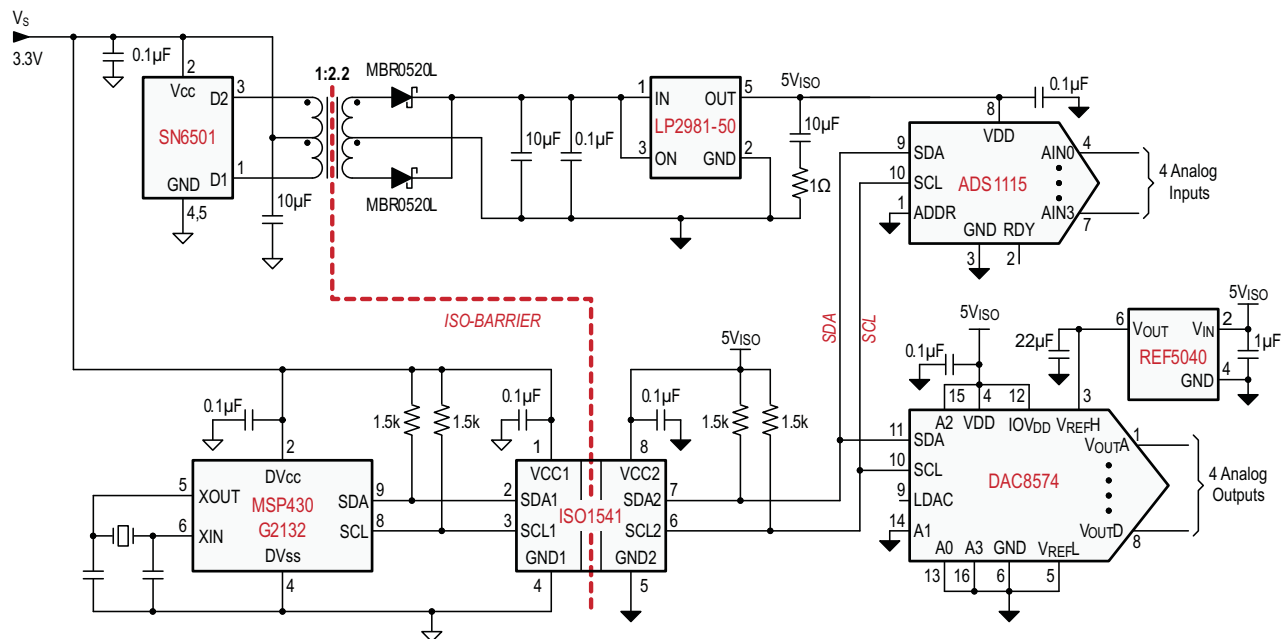


Figure 11. Isolated I<sup>2</sup>C Data Acquisition System

In Figure 11, the ultra low-power micro controller, MSP430G2132, controls the I<sup>2</sup>C data traffic of configuration data and conversion results for the analog inputs and outputs. Low-power data converters build the analog interface to sensors and actuators. The ISO1541 provides the necessary isolation between different ground potentials of the system controller, remote sensor, and actuator circuitry to prevent ground loop currents that otherwise may falsify the acquired data.

The entire circuit operates from a single 3.3 V supply. A low-power push-pull converter, SN6501, drives a center-tapped transformer whose output is rectified and linearly regulated to provide a stable 5 V supply for the data converters.

TYPICAL CHARACTERISTICS

SIDE 1 OUTPUT LOW VOLTAGE vs FREE-AIR TEMPERATURE

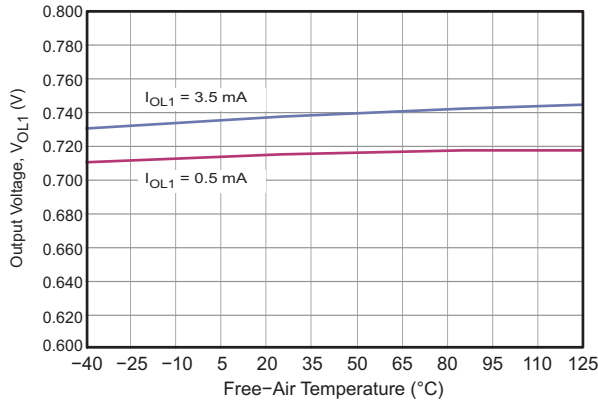


Figure 12.

SIDE 1 OUTPUT LOW CURRENT vs  $S_{DA1}$  or  $S_{CL1}$  APPLIED VOLTAGE

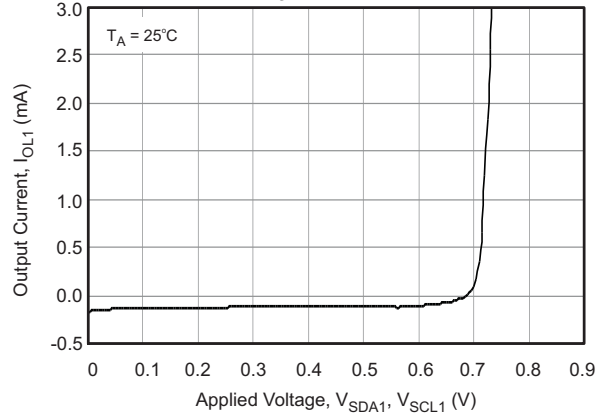


Figure 13.

SIDE 1 OUTPUT FALL TIME vs FREE-AIR TEMPERATURE

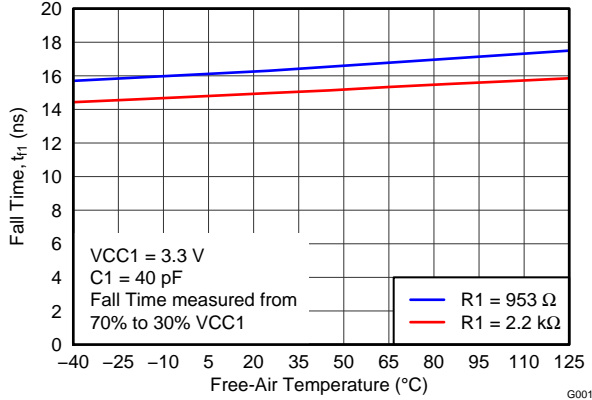


Figure 14.

SIDE 1 OUTPUT FALL TIME vs FREE-AIR TEMPERATURE

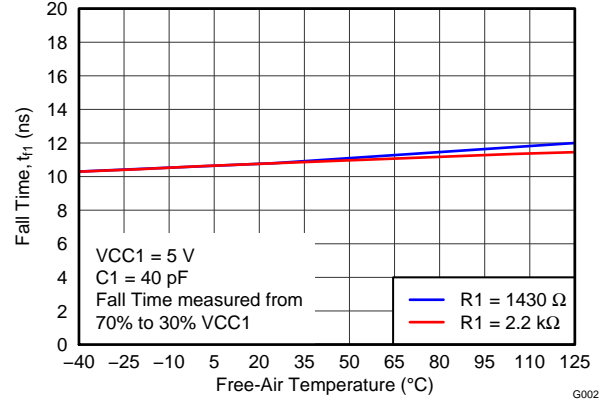


Figure 15.

SIDE 2 OUTPUT FALL TIME vs FREE-AIR TEMPERATURE

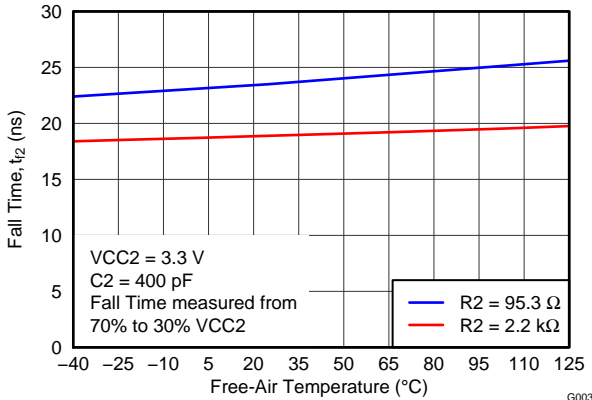


Figure 16.

SIDE 2 OUTPUT FALL TIME vs FREE-AIR TEMPERATURE

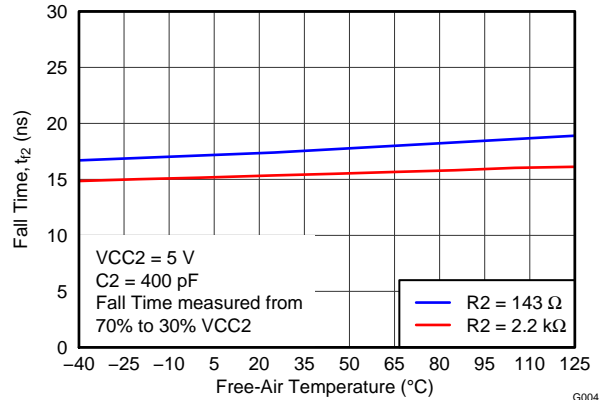


Figure 17.

TYPICAL CHARACTERISTICS (continued)

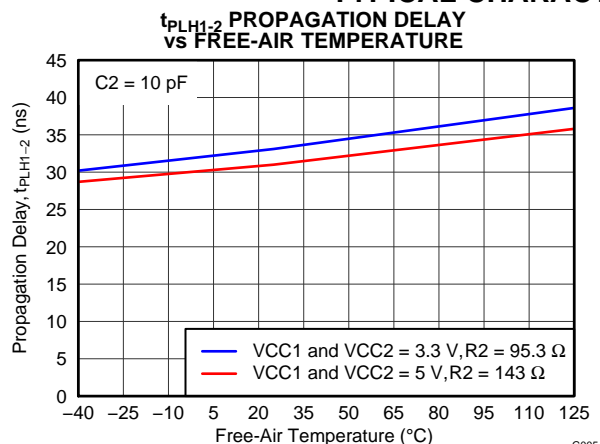


Figure 18.

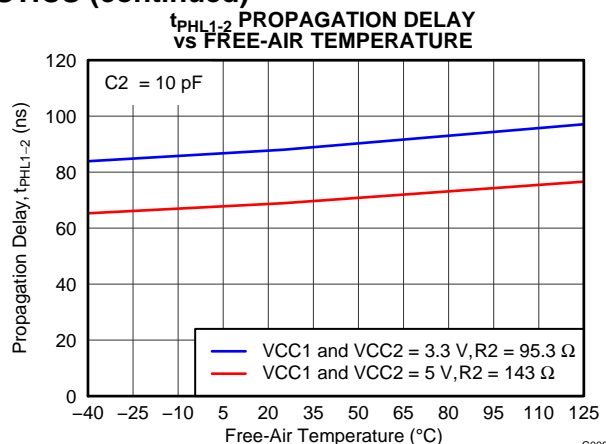


Figure 19.

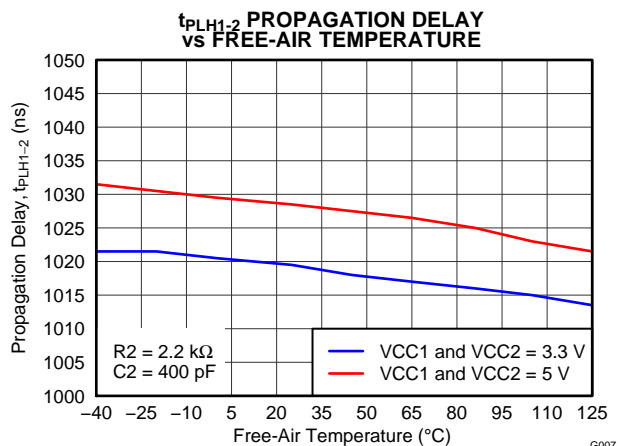


Figure 20.

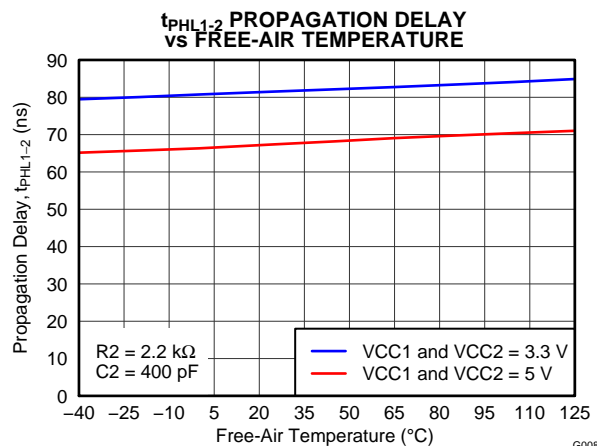


Figure 21.

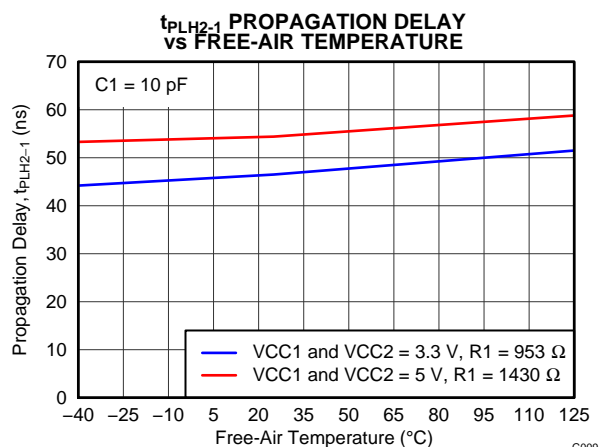


Figure 22.

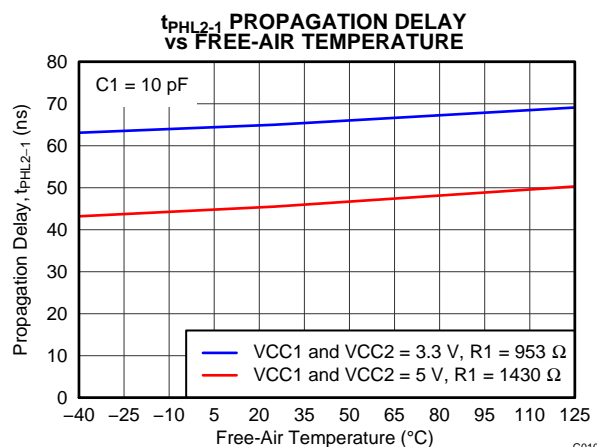


Figure 23.

**TYPICAL CHARACTERISTICS (continued)**

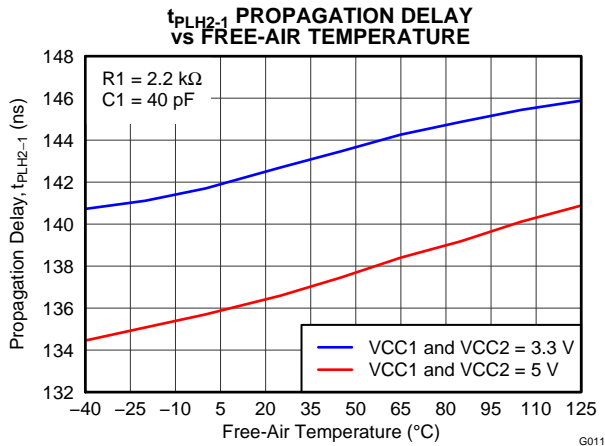


Figure 24.

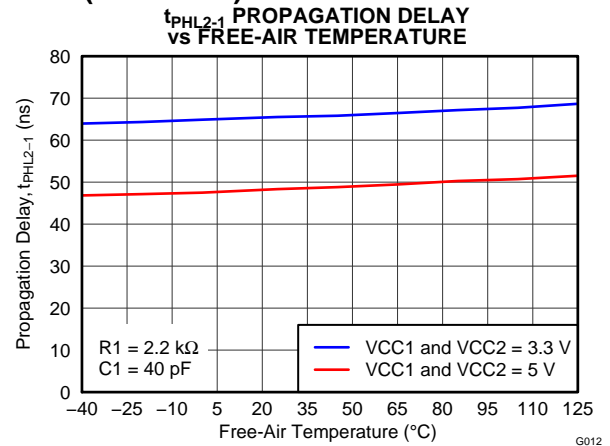


Figure 25.

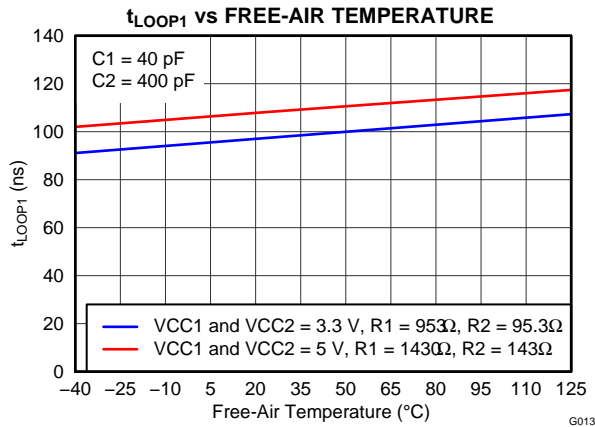


Figure 26.

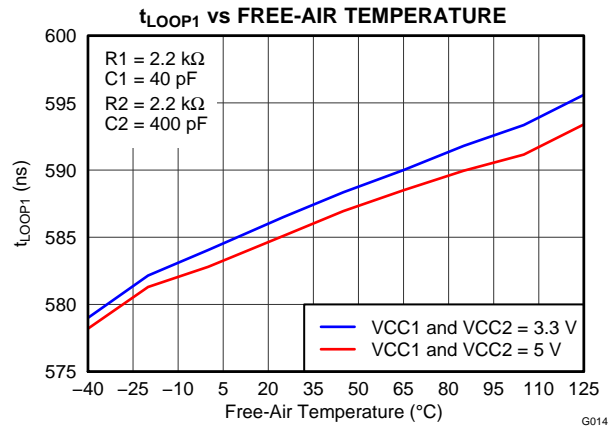


Figure 27.

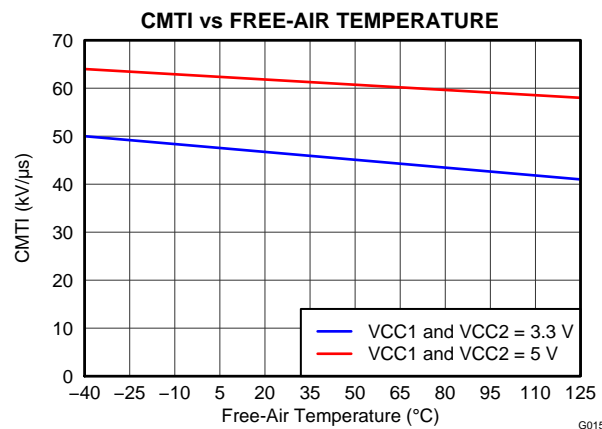
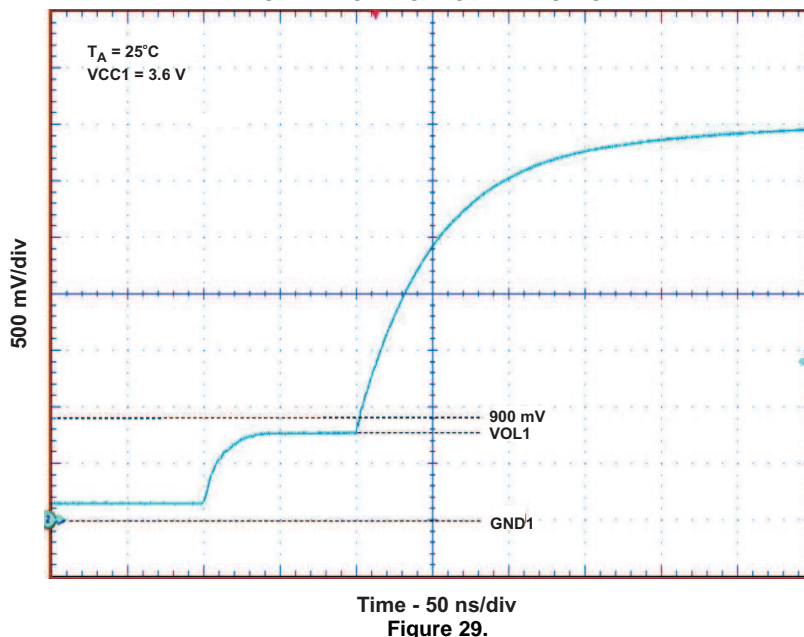


Figure 28.



**TYPICAL CHARACTERISTICS (continued)**  
**SIDE 1 LOW-TO-HIGH TRANSITION**



**REVISION HISTORY**

| Changes from Original (July 2012) to Revision A   | Page |
|---|------|
| <ul style="list-style-type: none"> <li>Changed From: CSA Component Acceptance Notice 5A (Pending) To: CSA Component Acceptance Notice 5A (Approved) ..... 1</li> <li>Changed From: IEC 60950-1 and IEC 61010-1 End Equipment Standards (Pending) To: IEC 60950-1 and IEC 61010-1 End Equipment Standards (Approved) ..... 1</li> <li>Changed Table 5, CSA column From: File number: 220991 (pending) To: File number: 220991 ..... 9</li> </ul> |      |
| Changes from Original (October 2012) to Revision B  | Page |
| <ul style="list-style-type: none"> <li>Change Safety Feature From: (VDE 0884 Part 2) (Pending) To: (VDE 0884 Part 2) (Approved) ..... 1</li> <li>Changed, VDE column From: File number: 40016131 (pending) To: File number: 40016131 ..... 9</li> </ul>   |      |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| ISO1540D         | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 125   | IS1540                   | <a href="#">Samples</a> |
| ISO1540DR        | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 125   | IS1540                   | <a href="#">Samples</a> |
| ISO1541D         | ACTIVE        | SOIC         | D               | 8    | 75          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 125   | IS1541                   | <a href="#">Samples</a> |
| ISO1541DR        | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 125   | IS1541                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

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