

# TLP2160

## 1. Applications

- Factory Networking
- High-Speed Digital Interfacing for Instrumentation and Control Devices
- Plasma Display Panels (PDPs)

## 2. General

The Toshiba TLP2160 consists of a high-output GaAs light-emitting diode coupled with a high-speed photo-diode-transistor chip. TLP2160 guarantees operation at up to 125°C and on supplies from 2.7 V to 5.5 V. It is offered in the SO8 package. It has a totem-pole output that can both sink and source current. With two LED-photoreceptor pairs, the TLP2160 helps save board space. An internal noise shield provides a guaranteed common-mode transient immunity of 20 kV/μs.

## 3. Features

- (1) Inverter logic type (Totem pole output)
- (2) Package: SO8
- (3) Operating temperature: -40 to 125°C
- (4) Supply voltage: 2.7 to 5.5 V
- (5) Data transfer rate: 20 MBd (typ.) (NRZ)
- (6) Threshold input current: 3.5 mA (max)
- (7) Supply current: 5 mA (max)
- (8) Common-mode transient immunity: ±20 kV/μs (min)
- (9) Isolation voltage: 2500 Vrms (min)
- (10) Safety standards

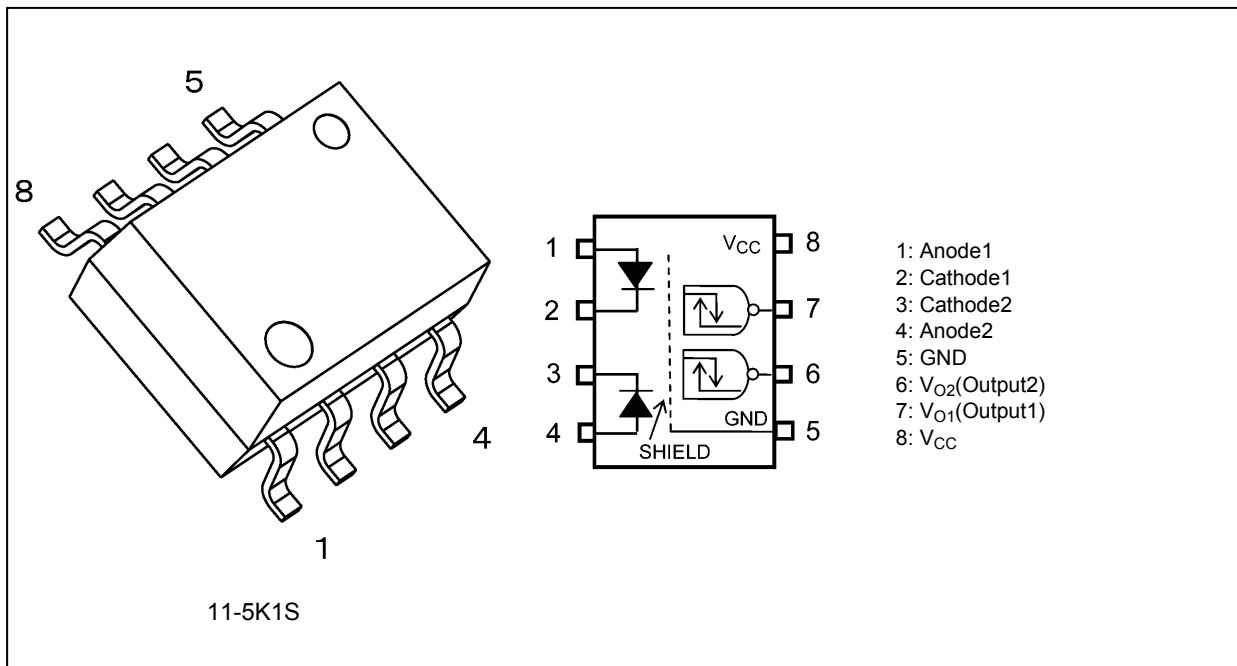
UL-approved: UL1577 File No.E67349

cUL-approved: CSA Component Acceptance Service No.5A, File No.E67349

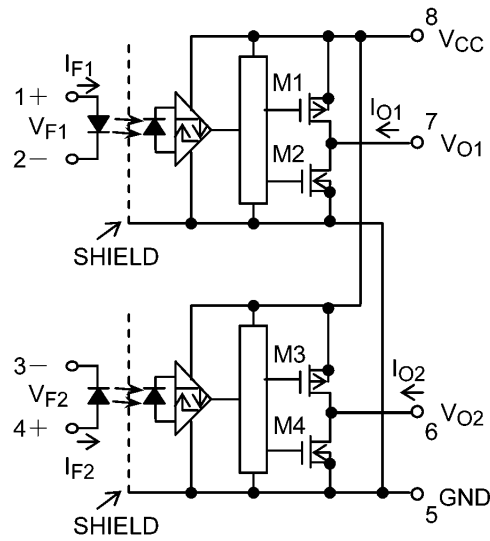
VDE-approved: Option (V4) EN60747-5-5 (Note)

Note: When an EN60747-5-5 approved type is needed, please designate the **Option (V4)**.

## 4. Packaging and Pin Configuration



**5. Internal Circuit (Note)**



**Fig. 5.1 Internal Circuit**

Note: A 0.1 $\mu$ F bypass capacitor must be connected between pin 8 and pin 5.

**6. Principle of Operation**

**6.1. Truth Table**

Input	LED1 (2)	M1 (3)	M2 (4)	Output1 (2)
H	ON	OFF	ON	L
L	OFF	ON	OFF	H

**6.2. Mechanical Parameters**

Characteristics	Min	Unit
Creepage distances	4.2	mm
Clearance distances	4.2	
Internal isolation thickness	—	

## 7. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^\circ\text{C}$ )

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	$I_F$	(Note 1)	25	mA
	Input forward current derating ( $T_a \geq 110^\circ\text{C}$ )	$\Delta I_F/\Delta T_a$	(Note 1)	-0.67	mA/ $^\circ\text{C}$
	Input forward current (pulsed)	$I_{FP}$	(Note 1), (Note 2)	40	mA
	Input forward current derating (pulsed) ( $T_a \geq 110^\circ\text{C}$ )	$\Delta I_{FP}/\Delta T_a$	(Note 1)	-1.0	mA/ $^\circ\text{C}$
	Input power dissipation	$P_D$	(Note 1)	40	mW
	Input power dissipation derating ( $T_a \geq 110^\circ\text{C}$ )	$\Delta P_D/\Delta T_a$	(Note 1)	-1.0	mW/ $^\circ\text{C}$
	Input reverse voltage	$V_R$	(Note 1)	5	V
Detector	Output current	$I_O$	(Note 1)	10	mA
	Output voltage	$V_O$	(Note 1)	6	V
	Supply voltage	$V_{CC}$		6	
	Output power dissipation	$P_O$	(Note 1)	60	mW
	Output power dissipation derating ( $T_a \geq 110^\circ\text{C}$ )	$\Delta P_O/\Delta T_a$	(Note 1)	-1.5	mW/ $^\circ\text{C}$
Common	Operating temperature	$T_{opr}$		-40 to 125	$^\circ\text{C}$
	Storage temperature	$T_{stg}$		-55 to 150	
	Lead soldering temperature (10 s)	$T_{sol}$		260	
	Isolation voltage AC, 1 min, R.H. $\leq 60\%$	$BV_S$	(Note 3)	2500	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Each channel

Note 2: Pulse width (PW)  $\leq 1$  ms, duty = 50 %

Note 3: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

## 8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1), (Note 2)	4.5	—	15	mA
Input off-state voltage	$V_{F(OFF)}$	(Note 1)	0	—	0.8	V
Supply voltage	$V_{CC}$	(Note 3)	2.7	3.3/5.0	5.5	
Operating temperature	$T_{opr}$	(Note 3)	-40	—	125	$^\circ\text{C}$

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (0.1  $\mu\text{F}$ ) should be connected between pin 8 and pin 5 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: Each channel

Note 2: The rise and fall times of the input on-current should be less than 0.5  $\mu\text{s}$ .

Note 3: Denotes the operating range, not the recommended operating condition.

**9. Electrical Characteristics (Note)**  
 (Unless otherwise specified,  $T_a = -40$  to  $125^\circ\text{C}$ ,  $V_{CC} = 2.7$  to  $5.5$  V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	$V_F$	(Note 1)	—	$I_F = 10$ mA, $T_a = 25^\circ\text{C}$	1.45	1.55	1.7	V
Input forward voltage temperature coefficient	$\Delta V_F/\Delta T_a$	(Note 1)	—	$I_F = 10$ mA	—	-2.0	—	mV/ $^\circ\text{C}$
Input reverse current	$I_R$	(Note 1)	—	$V_R = 5$ V, $T_a = 25^\circ\text{C}$	—	—	10	$\mu\text{A}$
Input capacitance	$C_t$	(Note 1)	—	$V = 0$ V, $f = 1$ MHz, $T_a = 25^\circ\text{C}$	—	60	—	pF
Low-level output voltage	$V_{OL}$	(Note 1)	Fig. 12.1.1	$I_F = 14$ mA, $I_O = 4$ mA	—	—	0.4	V
High-level output voltage	$V_{OH}$	(Note 1)	Fig. 12.1.2	$V_F = 1.05$ V, $I_O = -4$ mA, $V_{CC} = 3.3$ V	2.3	—	—	V
		(Note 1)		$V_F = 1.05$ V, $I_O = -4$ mA, $V_{CC} = 5$ V	4	—	—	
Low-level supply current	$I_{CCL}$		Fig. 12.1.3	$I_F = 14$ mA	—	—	5	mA
High-level supply current	$I_{CCH}$		Fig. 12.1.4	$I_F = 0$ mA	—	—	5	
Threshold input current (H/L)	$I_{FHL}$	(Note 1)	—	$I_O = 1.6$ mA, $V_O < 0.4$ V	—	—	3.5	

Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note 1: Each channel

**10. Isolation Characteristics (Unless otherwise specified,  $T_a = 25^\circ\text{C}$ )**

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	$C_S$	(Note 1)	$V_S = 0$ V, $f = 1$ MHz	—	0.8	—	pF
Isolation resistance	$R_S$	(Note 1)	$V_S = 500$ V, R.H. $\leq 60\%$	$1 \times 10^{12}$	$10^{14}$	—	$\Omega$
Isolation voltage	$BV_S$	(Note 1)	AC, 1 min	2500	—	—	Vrms
			AC, 1 s in oil	—	5000	—	
			DC, 1 min in oil	—	5000	—	Vdc

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

**11. Switching Characteristics (Note)**

**11.1. Switching Characteristics (1) (Each Channel)**  
 (Unless otherwise specified,  $T_a = -40$  to  $125^\circ\text{C}$ ,  $V_{CC} = 2.7$  to  $3.6$  V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)	Fig. 12.1.5	$I_F = 0 \rightarrow 14$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	30	40	ns
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)		$I_F = 14 \rightarrow 0$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	25	40	
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)		$I_F = 14$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	5	25	
Propagation delay skew (device to device)	$t_{psk}$	(Note 1), (Note 2)			-30	—	30	
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)	Fig. 12.1.5	$I_F = 0 \rightarrow 6$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	36	55	
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)		$I_F = 6 \rightarrow 0$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	26	55	
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)		$I_F = 6$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	10	30	
Propagation delay skew (device to device)	$t_{psk}$	(Note 1), (Note 2)			-30	—	30	
Fall time	$t_f$	(Note 1)	Fig. 12.1.5	$I_F = 0 \rightarrow 14$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	15	—	
Rise time	$t_r$	(Note 1)		$I_F = 14 \rightarrow 0$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	15	—	
Common-mode transient immunity at output high	$CM_H$		Fig. 12.1.6	$V_{CM} = 1000$ V <sub>p-p</sub> , $I_F = 0$ mA, $V_{O(min)} = 2$ V, $V_{CC} = 3.3$ V, $T_a = 25^\circ\text{C}$	$\pm 20$	$\pm 25$	—	kV/ $\mu\text{s}$
Common-mode transient immunity at output low	$CM_L$			$V_{CM} = 1000$ V <sub>p-p</sub> , $I_F = 14$ mA, $V_{O(max)} = 0.4$ V, $V_{CC} = 3.3$ V, $T_a = 25^\circ\text{C}$	$\pm 20$	$\pm 25$	—	

Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note 1:  $f = 5$  MHz, duty = 50 %, input current  $t_r = t_f = 5$  ns,  $C_L$  is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: The propagation delay skew,  $t_{psk}$ , is equal to the magnitude of the worst-case difference in  $t_{pHL}$  and/or  $t_{pLH}$  that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

**11.2. Switching Characteristics (2) (Each Channel)**  
 (Unless otherwise specified,  $T_a = -40$  to  $125^\circ\text{C}$ ,  $V_{CC} = 4.5$  to  $5.5$  V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit	
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)	Fig. 12.1.5	$I_F = 0 \rightarrow 14$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	33	45	ns	
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)			$I_F = 14 \rightarrow 0$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	25		45
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)			$I_F = 14$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	8		25
Propagation delay skew (device to device)	$t_{psk}$	(Note 1), (Note 2)				-30	—		30
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)	Fig. 12.1.5	$I_F = 0 \rightarrow 6$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	40	55		
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)			$I_F = 6 \rightarrow 0$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	28		55
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)			$I_F = 6$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	12		30
Propagation delay skew (device to device)	$t_{psk}$	(Note 1), (Note 2)				-30	—		30
Fall time	$t_f$	(Note 1)	Fig. 12.1.5	$I_F = 0 \rightarrow 14$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	15	—		
Rise time	$t_r$	(Note 1)			$I_F = 14 \rightarrow 0$ mA, $R_{IN} = 100 \Omega$ , $C_L = 15$ pF	—	15		—
Common-mode transient immunity at output high	$CM_H$		Fig. 12.1.6	$V_{CM} = 1000$ V <sub>p-p</sub> , $I_F = 0$ mA, $V_{O(min)} = 4$ V, $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$	$\pm 20$	$\pm 25$	—	kV/ $\mu\text{s}$	
Common-mode transient immunity at output low	$CM_L$				$V_{CM} = 1000$ V <sub>p-p</sub> , $I_F = 14$ mA, $V_{O(max)} = 0.4$ V, $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$	$\pm 20$	$\pm 25$		—

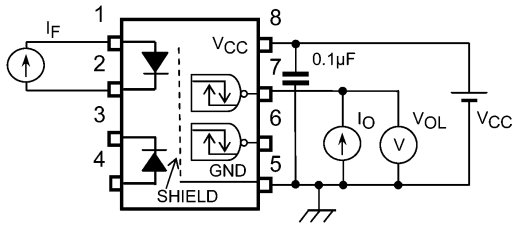
Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note 1:  $f = 5$  MHz, duty = 50 %, input current  $t_r = t_f = 5$  ns,  $C_L$  is approximately 15 pF which includes probe and stray wiring capacitance.

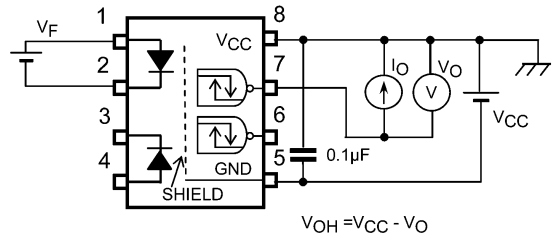
Note 2: The propagation delay skew,  $t_{psk}$ , is equal to the magnitude of the worst-case difference in  $t_{pHL}$  and/or  $t_{pLH}$  that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

**12. Test Circuits and Characteristics Curves**

**12.1. Test Circuits**

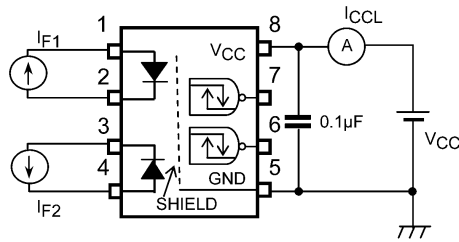


**Fig. 12.1.1 VOL Test Circuit**

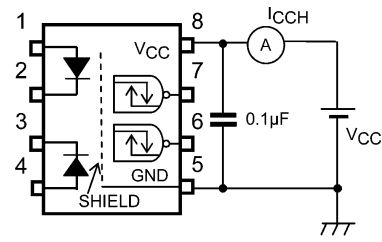


**Fig. 12.1.2 VOH Test Circuit**

$V_{OH} = V_{CC} - V_O$

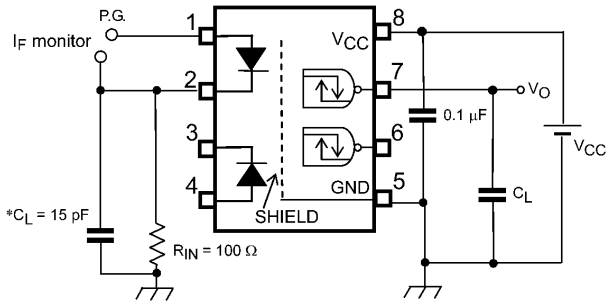


**Fig. 12.1.3 ICCL Test Circuit**

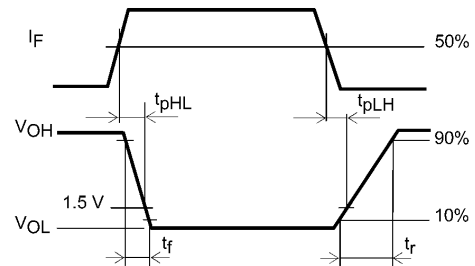


**Fig. 12.1.4 ICCH Test Circuit**

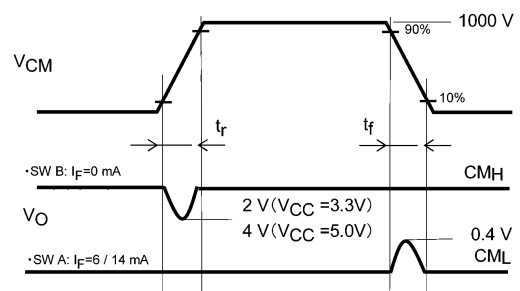
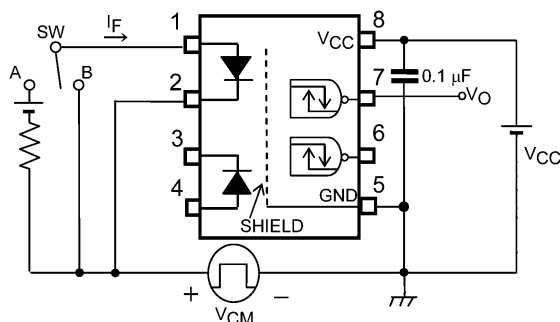
$I_F = 6/14 \text{ mA (P.G.)}$   
 $(f = 5 \text{ MHz, duty} = 50\%, \text{ less than } t_r = t_f = 5 \text{ ns})$



\* $C_L$  includes probe and stray capacitance.  
 P.G.: Pulse generator



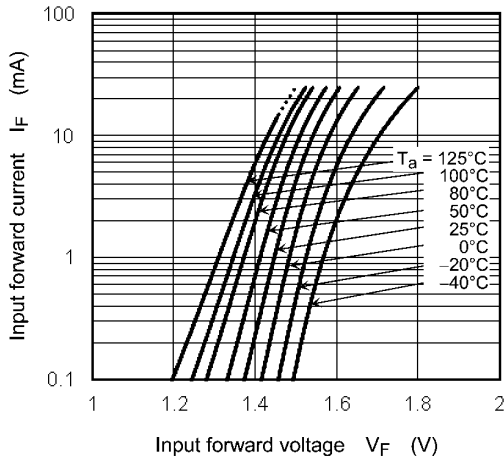
**Fig. 12.1.5 Switching Time Test Circuit**



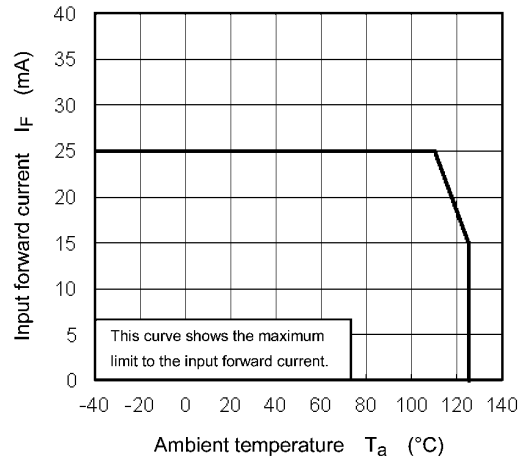
$$CML = \frac{800(V)}{t_f (\mu s)} \quad CMH = -\frac{800(V)}{t_r (\mu s)}$$

**Fig. 12.1.6 Common-Mode Transient Immunity**

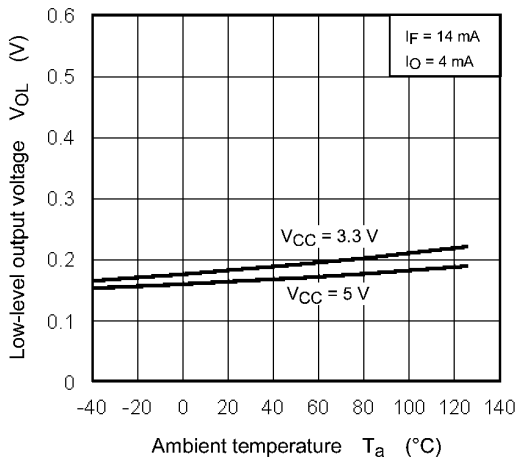
**12.2. Characteristics Curves (Note)**



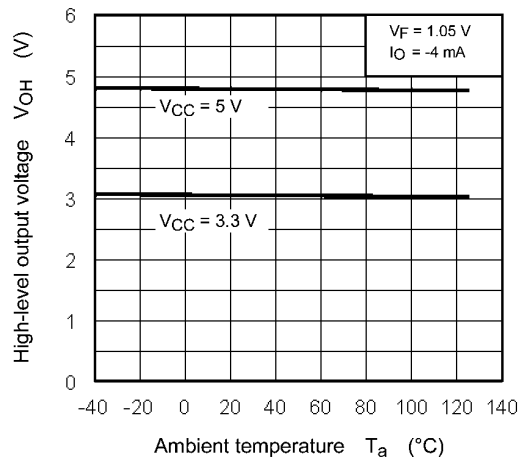
**Fig. 12.2.1  $I_F - V_F$**



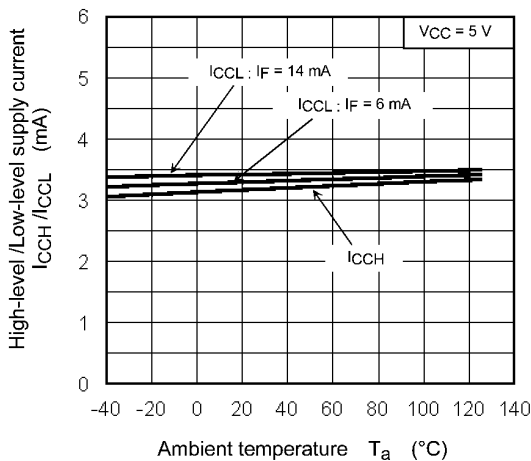
**Fig. 12.2.2  $I_F - T_a$**



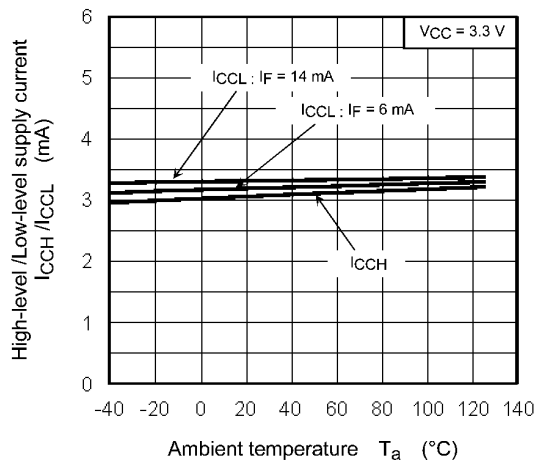
**Fig. 12.2.3  $V_{OL} - T_a$**



**Fig. 12.2.4  $V_{OH} - T_a$**



**Fig. 12.2.5  $I_{CCH} / I_{CCL} - T_a$**



**Fig. 12.2.6  $I_{CCH} / I_{CCL} - T_a$**



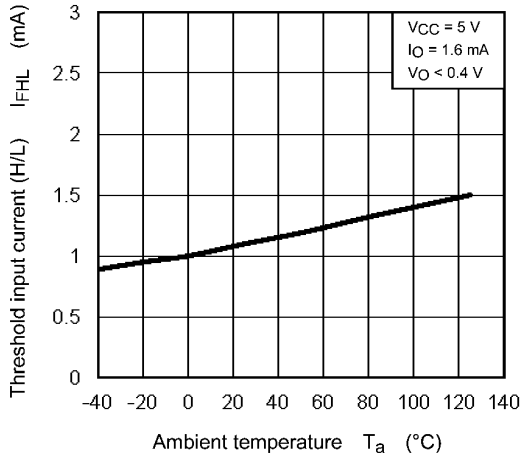


Fig. 12.2.7  $I_{FHL} - T_a$

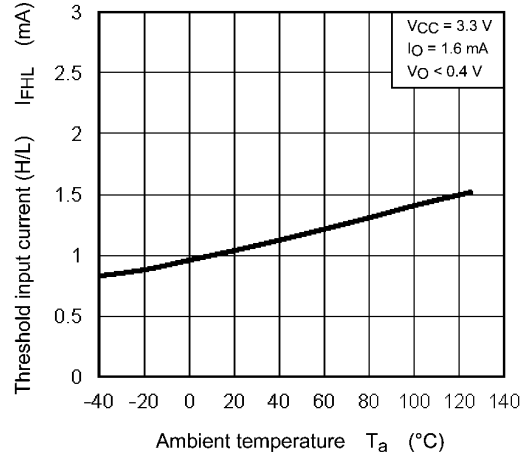


Fig. 12.2.8  $I_{FHL} - T_a$

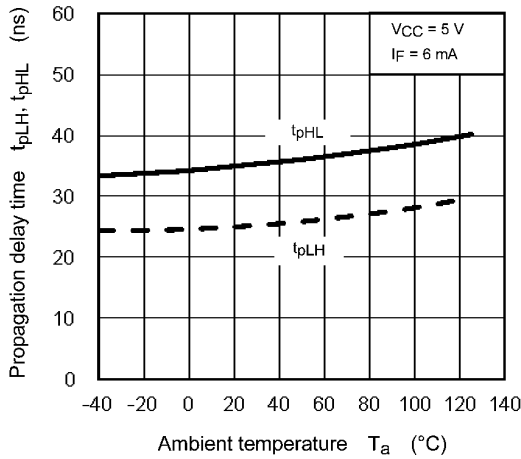


Fig. 12.2.9  $t_{pLH} / t_{pHL} - T_a$

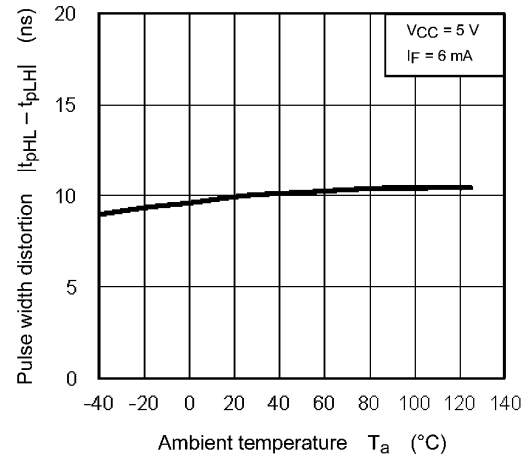


Fig. 12.2.10  $|t_{pHL} - t_{pLH}| - T_a$

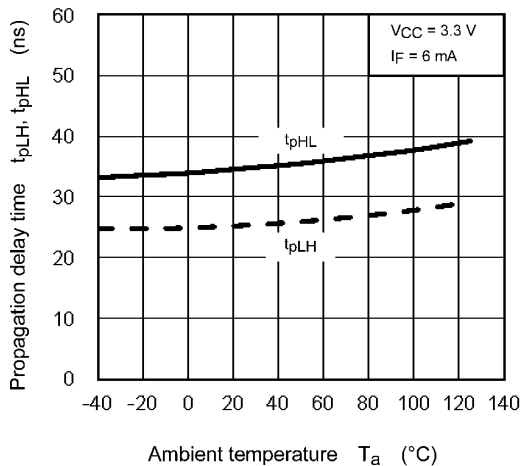


Fig. 12.2.11  $t_{pLH} / t_{pHL} - T_a$

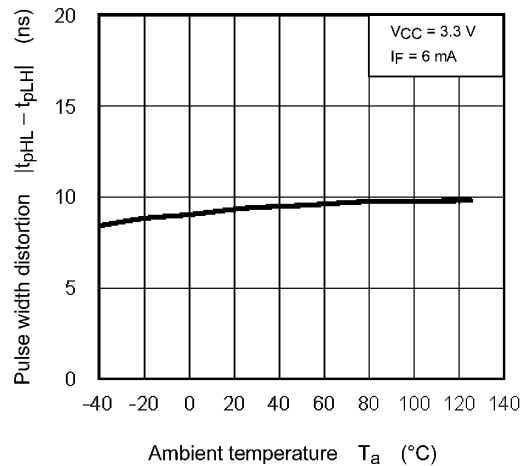
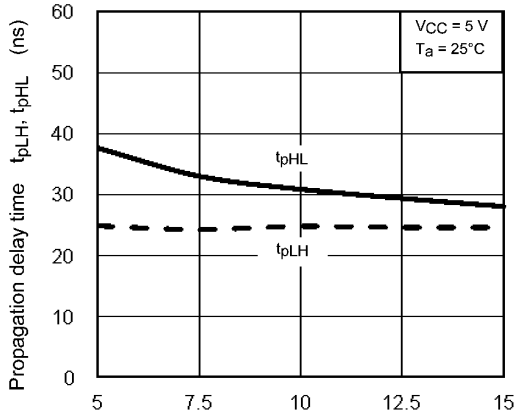
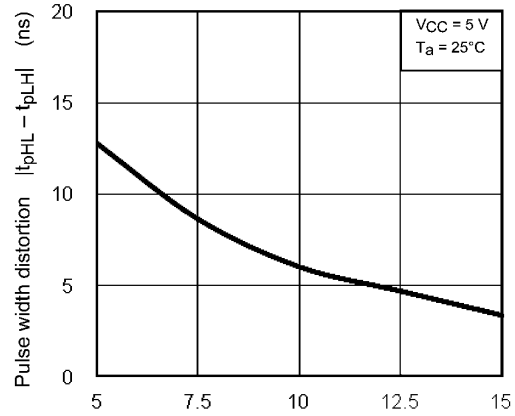


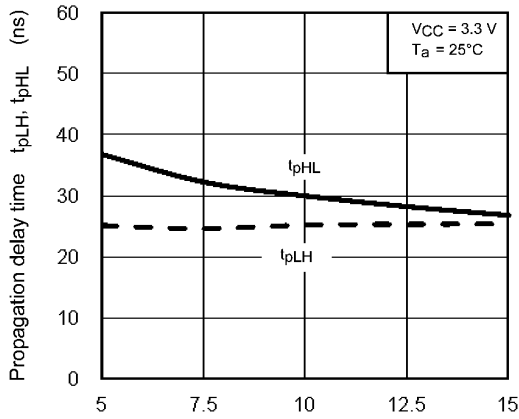
Fig. 12.2.12  $|t_{pHL} - t_{pLH}| - T_a$



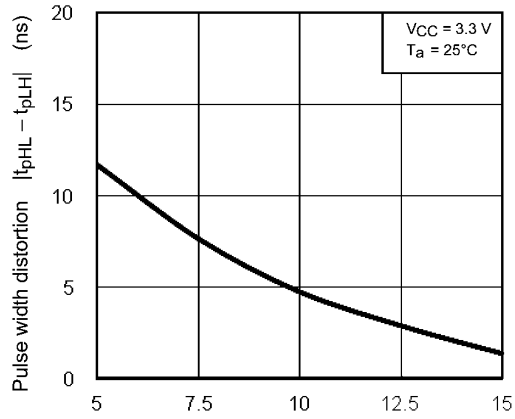
**Fig. 12.2.13**  $t_{pLH} / t_{pHL} - I_F$



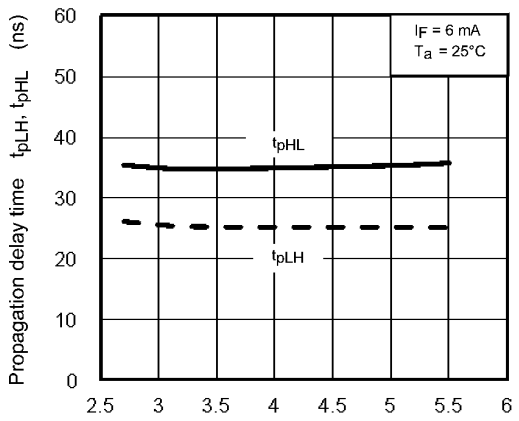
**Fig. 12.2.14**  $|t_{pHL} - t_{pLH}| - I_F$



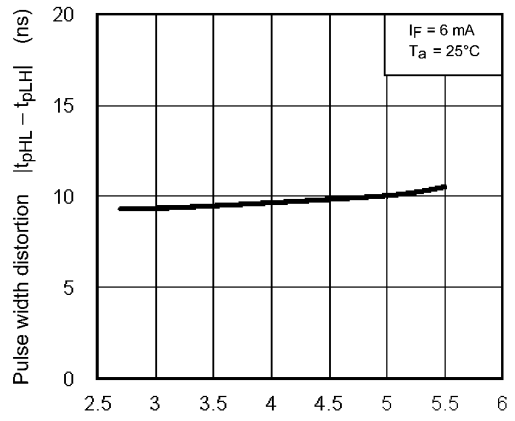
**Fig. 12.2.15**  $t_{pLH} / t_{pHL} - I_F$



**Fig. 12.2.16**  $|t_{pHL} - t_{pLH}| - I_F$



**Fig. 12.2.17**  $t_{pLH} / t_{pHL} - V_{CC}$



**Fig. 12.2.18**  $|t_{pHL} - t_{pLH}| - V_{CC}$

NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

**13. Soldering and Storage**

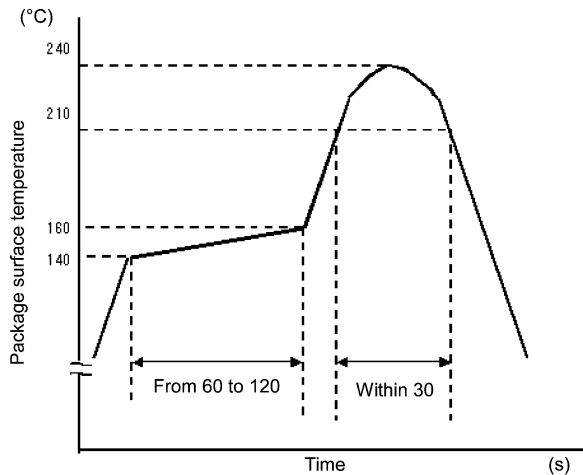
**13.1. Precautions for Soldering**

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

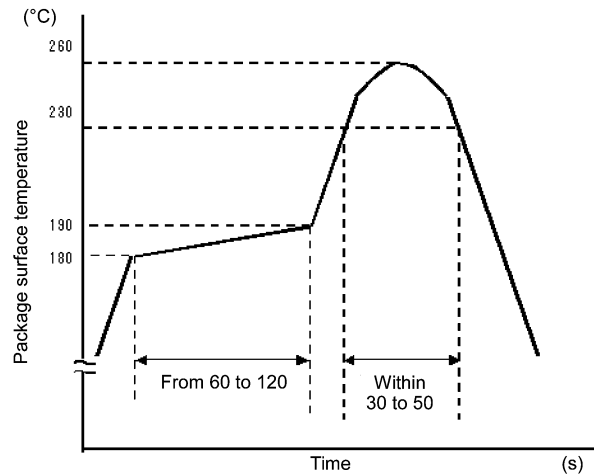
- When using soldering reflow (See Fig. 13.1.1 and 13.1.2)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



**Fig. 13.1.1 An Example of A Temperature Profile when Sn-Pb Eutectic Solder Is Used**



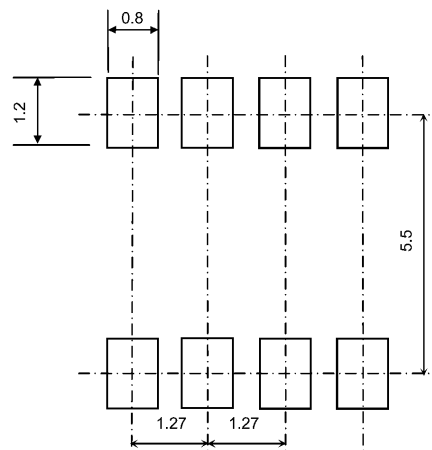
**Fig. 13.1.2 An Example of A Temperature Profile when Lead(Pb)-Free Solder Is Used**

- When using soldering flow (Applicable to both eutectic solder and Lead(Pb)-Free solder)  
Apply preheating of 150°C for 60 to 120 seconds.  
Mounting condition of 260°C within 10 seconds is recommended.  
Flow soldering must be performed once.
- When using soldering Iron (Applicable to both eutectic solder and Lead(Pb)-Free solder)  
Complete soldering within 10 seconds for lead temperature not exceeding 260°C or within 3 seconds not exceeding 350°C  
Heating by soldering iron must be done only once per lead.

**13.2. Precautions for General Storage**

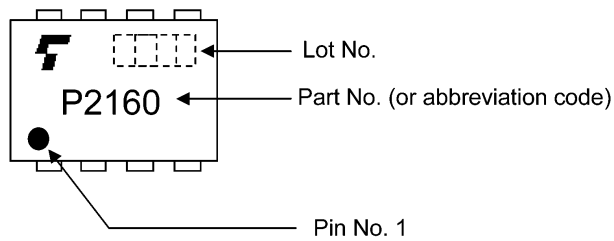
- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5°C to 35°C and 45% to 75%, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

**14. Land Pattern Dimensions for Reference Only**



**Fig. 14.1 Land Pattern Dimensions for Reference Only (unit: mm)**

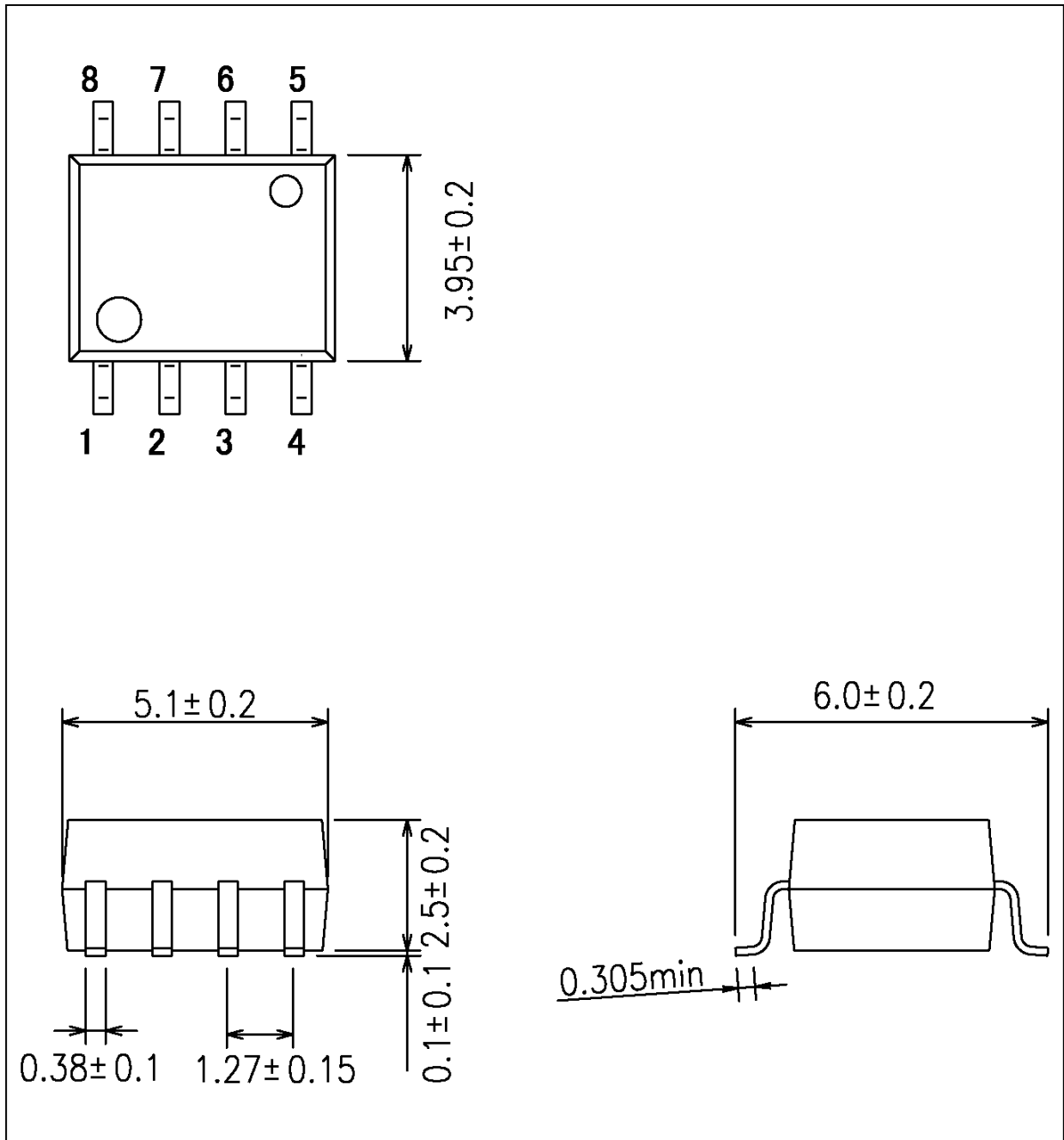
**15. Marking**



**Fig. 15.1 Marking**

Package Dimensions

Unit: mm



Weight: 0.11 g (typ.)

Package Name(s)
TOSHIBA: 11-5K1S

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